iC-TW3 SENSOR SIGNAL CONDITIONER WITH TEMPERATURE COMPENSATION AND LINE DRIVER

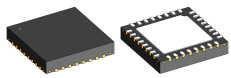
FEATURES

- Fully differential 3-channel signal conditioning
- PGS inputs for differential and single-ended signals
- Overall gain of -3 to 57 dB, adjustable in steps of 0.08 dB
- Output referred offset range of ±1.2 V, adjustable in steps of 2 mV
- Signal bandwidth to 1 MHz and in/out latency below 1 µs
- Selectable automatic gain and offset control for encoder applications
- On-chip or off-chip temperature sensing
- Temperature drift compensation for gain and offset via programmable look-up-tables
- Short-circuit-proof outputs: 1 Vpp to 100 Ω, 2 Vpp to 1 kΩ
- I^2C interface to restore device setup from serial EEPROM
- Bidirectional 1-wire interface for direct RAM and EEPROM access
- Optical setup link via 1-wire interface operating a photo receiver
- Single 3.0 V to 5.5 V supply
- Operating temperature range of -40 to +125 °C

APPLICATIONS

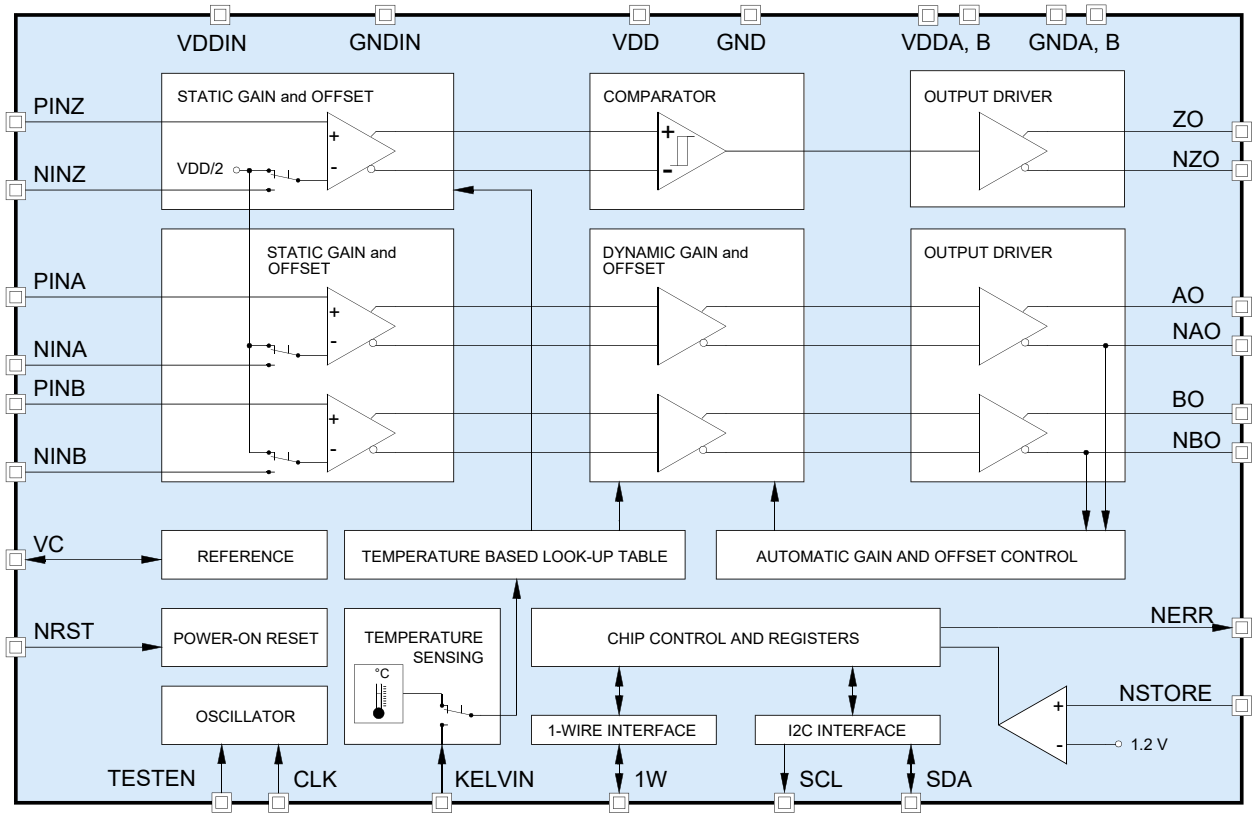
- Programmable general purpose sensor interface
- Optical position sensors
- Magnetic position sensors
- Incremental position sensors
- Linear scales

PACKAGES



QFN32
5 mm x 5 mm
RoHS compliant

BLOCK DIAGRAM



DESCRIPTION

The general purpose sensor signal conditioner iC-TW3 provides highly accurate non contact trimming of three independent sine/cosine sensor signals. The differential output signals can be calibrated to 1 Vpp or to 2 Vpp, alternatively.

The internal or an external temperature sensor linked to the chip can influence the gain and offset correction by arbitrary temperature-dependent compensation parameters sourced from a look-up table.

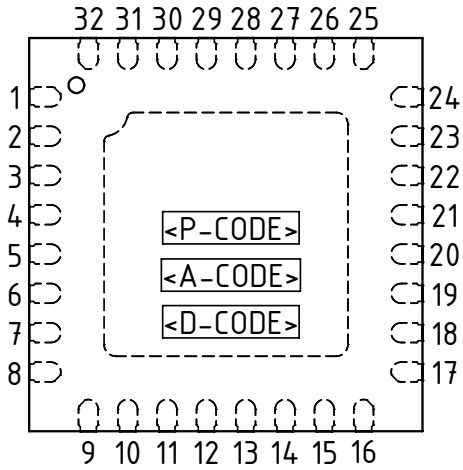
For encoder applications an automatic gain and offset control compensates sensor offset voltages and stabilizes the output signal level.

The direct connection of sine/cosine encoders, MR sensor bridges or photosensor arrays is possible and supported by a selectable input impedance.

PACKAGING INFORMATION

PIN CONFIGURATION QFN32 (5 mm x 5 mm)

(top view)



PIN FUNCTIONS

No.	Name	Function
1	PINZ	Signal Input Z+
2	NINZ	Signal Input Z-
3	TESTEN[4]	Test Mode Enable Input
4	CLK[5]	External Clock Input (optional)
5	NZO	Signal Output Z-
6	ZO	Signal Output Z+
7	GNDB	Driver Ground
8	VDDB	+3...+5.5 V Driver Supply Voltage
9	NBO	Signal Output B-
10	BO	Signal Output B+
11	GND	Digital Ground
12	SCL	I2C Interface, clock line
13	SDA	I2C interface, data line
14	VDD	+3...+5.5 V Digital Supply Voltage
15	GNDA	Driver Ground
16	n.c.[1]	
17	AO	Signal Output A+
18	NAO	Signal Output A-
19	VDDA	+3...+5.5 V Driver Supply Voltage
20	1W	1-Wire Interface, bidirectional port
21	NERR	Error Message Output (active low)
22	NRST	External Reset Input (active low)
23	NSTORE[2]	Coefficient Store Input (active low)
24	n.c.[1]	
25	NINA	Signal Input A-
26	PINA	Signal Input A+
27	KELVIN[5]	External Temperature Sensor Input
28	GNDIN	Input Ground
29	VDDIN	+3...+5.5 V Input Supply Voltage
30	PINB	Signal Input B+
31	NINB	Signal Input B-
32	VC	1.21 V Reference Voltage Output, Reference Voltage Input (optional)
TP	TP[3]	Thermal Pad

IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes), <D-CODE> = date code (subject to changes);

[1] Pin is not connected.

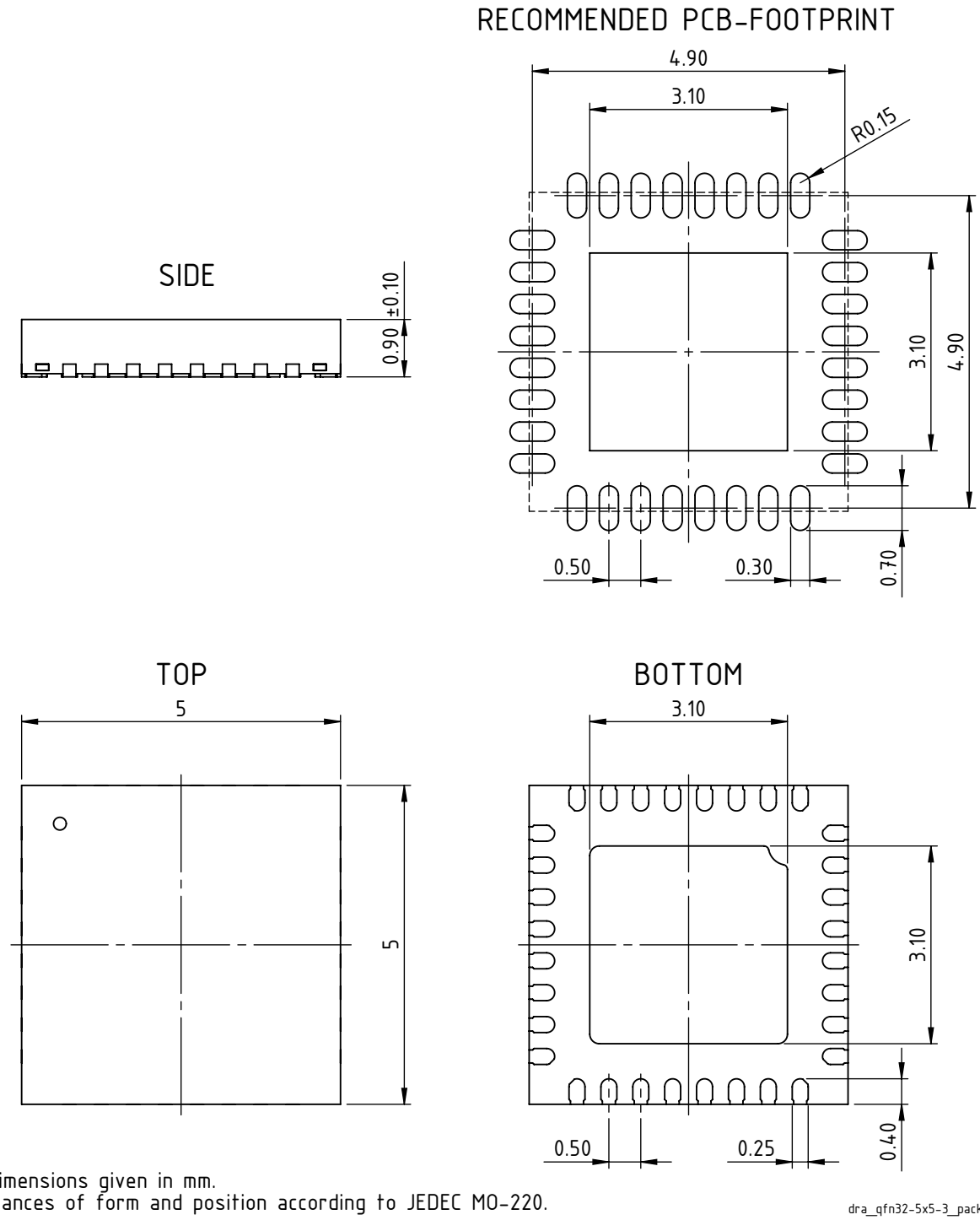
[2] Pin NSTORE should be wired to VDD.

[3] The Thermal Pad of the QFN package (bottom side) is to be connected to a ground plane on the PCB which must have GND potential.

[4] Pin features an internal pull-down. Connect to GND if there is no need to enable chip test functions for verification.

[5] Pin can remain open when not in use.

PACKAGE DIMENSIONS



All dimensions given in mm.
Tolerances of form and position according to JEDEC MO-220.

dra_qfn32-5x5-3_pack_1, 10:1

ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these ratings device damage may occur.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VDDx()	Voltage at VDD, VDDA, VDDB, VDDIN	referenced to GND, GNDA, GNDB, GNDIN	-0.3	6.0	V
G002	V()	Voltage applied to any other pin	referenced to GND	-0.3	VDD + 0.5	V
G003	V()	Voltage Difference VDDA, VDDB vs. VDD			0.5	V
G004	V()	Voltage Difference VDDIN vs. VDD			0.5	V
G005	V()	Voltage Difference GNDA, GNDB vs. GND			0.5	V
G006	V()	Voltage Difference GNDIN vs. GND			0.5	V
G007	Vd	ESD Susceptibility Of Signal Outputs: AO, NAO, BO, NBO, ZO, NZO	HBM, 100 pF discharged through 1.5 kΩ		2	kV
G008	Vd	ESD Susceptibility (remaining pins)	HBM, 100 pF discharged through 1.5 kΩ		2	kV
G009	Ptot	Permissible Power Dissipation			500	mW
G010	Tj	Junction Temperature		-40	150	°C

THERMAL DATA

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range		-40		125	°C
T02	Rthja	Thermal Resistance Chip To Ambient	surface mounted to PCB according to JEDEC 51		40		K/W
T03	Ts	Storage Temperature		-40		150	°C

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD, VDDA, VDDB, VDDIN = 3.0...5.5 V, Tj = -40...125 °C, reference point GND unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VDDx	Permissible Supply Voltage at VDD, VDDA, VDDB, VDDIN		3.0		5.5	V
002	I(VDDx)	Total Supply Current	VDDx = 3.3 V VDDx = 5.5 V			15 25	mA mA
003	Vc()hi	Clamp-Voltage hi at all pins	Vc()hi = V() - VDD; I() = 10 mA	0.3		1.4	V
004	Vc()lo	Clamp-Voltage lo at all pins	I() = -10 mA	-1.2		-0.3	V
Analog Signal Inputs PINA, NINA, PINB, NINB, PINZ, NINZ							
101	Vin()sig	Permissible Input Voltage Range		1.4		VDD – 1.2	V
102	Vin()os	Input Offset Voltage			±5	±15	mV
103	Iin()	Input Current	ENSIGAB = 0, ENSIGZ = 0	-35		35	nA
104	Rpu()	Input Pull-Up Resistor	ENSIGAB = 1, ENSIGZ = 1	2.0	2.5	3	MΩ
105	fg	-3 dB Bandwidth	PGA gain of 36 dB	1.2			MHz
106	CMRR	Common Mode Rejection Ratio	fc < 1 MHz fc < 1 kHz		40 60		dB dB
107	PSRR	Power Supply Rejection Ratio	fc < 1 MHz fc < 1 kHz		40 60		dB dB
108	e_n	Input Voltage Noise	f = 1 kHz f = 100 Hz f = 0.1 to 10 Hz		20 n 25 n 2 µ		V/√Hz V/√Hz V/√Hz
109	ΔDGAIN	Dynamic Gain Step Width			0.08		dB
110	ΔDOFFS	Dynamic Offset Step Width			2		mV
Temperature Sensor and Analog Input KELVIN							
201	Tor	Int. Temperature Sensor Operating Range	after calibration of ADC;	-50		150	°C
202	Tacc	Device-To-Device Temp. Sensor Variation	after calibration of ADC, Tj = -40 °C to 125 °C		± 10		°C
203	Vin()low	Temperature Input Voltage	CELSIUS(7:0) = 10 CELSIUS(7:0) = 245		1.7 0.9		V V
204	Iin()	Input Current at KELVIN	V(KELVIN) = 0 .. VDD	-50		50	nA
205	T()lo	Lo-Temperature ADC Reading, via Register CELSIUS(7:0)	after calibration of ADC; XCELSIUS = 0, internal sensor: Tj = -40 °C XCELSIUS = 1, ext. sensor: V(KELVIN) = 1.7 V		19 10		
206	T()hi	Hi-Temperature ADC Reading, via Register CELSIUS(7:0)	after calibration of ADC; XCELSIUS = 0, internal sensor: Tj = 125 °C XCELSIUS = 1, ext. sensor: V(KELVIN) = 0.9 V		224 245		
Reference Voltage Input/Output VC							
301	Vout(VC)	Reference Voltage Output	VEXT = 0; CL = 100 nF, I() = 0 mA	1.10	1.21	1.35	V
302	Vin(VC)	Permissible Input Voltage Range at VC	VEXT = 1	0		2.21	V
303	Iin(VC)	Input Current at VC	VEXT = 1	-0.1		1	µA
Power-On Reset and Input NRST							
401	VDDon	Turn-On Threshold (power-on release)	increasing voltage at VDD			3.0	V
402	VDDoff	Turn-Off Threshold (power-down reset)	decreasing voltage at VDD		2.6		V
403	Vt()hi	Input Threshold Voltage hi	VDD = 3.3 V +/- 10 % VDD = 5.0 V +/- 10 %	1.5 3.3			V V
404	Vt()lo	Input Threshold Voltage lo	VDD = 3.3 V +/- 10 % VDD = 5.0 V +/- 10 %			0.8 1.0	V V
405	Ipu()	Input Pull-Up Current	V() = 0...VDD - 1 V			-3	µA
406	Vpu()	Input Pull-Up Voltage	Vpu() = VDD - V(), I() = -3 µA			700	mV

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD, VDDA, VDDB, VDDIN = 3.0...5.5 V, Tj = -40...125 °C, reference point GND unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Oscillator CLK, TESTEN							
501	Vt()hi	Input Threshold Voltage hi	VDD = 3.3 V +/- 10 % VDD = 5.0 V +/- 10 %	1.5 3.3			V V
502	Vt()lo	Input Threshold Voltage lo	VDD = 3.3 V +/- 10 % VDD = 5.0 V +/- 10 %			0.8 1.0	V V
503	Ipd()	Input Pull-Down Current	V() = 1 V...VDD	3			µA
504	Vpd()	Input Pull-Down Voltage	I() = 3 µA			700	mV
505	fosc	Oscillator Frequency	TEST_CLK = 1, measured at NERR; CLKDIV = 0 (low active) CLKDIV = 1			 2 4	 MHz MHz
506	fin()	Permissible External Clock Frequency at CLK				4	MHz
1-Wire Interface 1W							
601	Vs()lo	Saturation Voltage lo	I() = 1 mA			300	mV
602	Isc()lo	Short-Circuit Current lo		2			mA
603	Ipu()	Input Pull-Up Current	V() = 0...VDD - 1 V			-3	µA
604	Vpu()	Input Pull-Up Voltage	Vpu() = VDD - V(), I() = -3 µA			700	mV
605	tr(), tf()	Rise and Fall Time (10/90%)	VDD = 3.3 V, CL = 10 pF			32	ns
606	Vt()hi	Input Threshold Voltage hi	VDD = 3.3 V +/- 10 % VDD = 5.0 V +/- 10 %	1.5 3.3			V V
607	Vt()lo	Input Threshold Voltage lo	VDD = 3.3 V +/- 10 % VDD = 5.0 V +/- 10 %			0.8 1.0	V V
I2C Interface SDA, SCL							
701	Vs()lo	Saturation Voltage lo	I() = 1 mA			400	mV
702	Isc()lo	Short-Circuit Current lo	V() = 1V...VDD	3			mA
703	Ipu()	Pull-Up Current	V() = 0...VDD - 1 V			-3	µA
704	Vpu()	Input Pull-Up Voltage	Vpu() = VDD - V(), I() = -3 µA			700	mV
705	Vt()hi	Input Threshold Voltage hi at SDA	VDD = 3.3 V +/- 10 % VDD = 5.0 V +/- 10 %	1.5 3.3			V V
706	Vt()lo	Input Threshold Voltage lo at SDA	VDD = 3.3 V +/- 10 % VDD = 5.0 V +/- 10 %			0.8 1.0	V V
707	fclk()	Write/Read Clock Frequency at SCL	CLKDIV = 0		100		kHz
708	tbusy()cfg	Duration Of Startup Configuration	CLKDIV = 0, 2 LUT blocks CLKDIV = 0, 16 LUT blocks			20 80	ms ms
Digital Output NERR							
901	Vs()lo	Saturation Voltage lo	I() = 1 mA			400	mV
902	Vs()hi	Saturation Voltage hi	Vs()hi = VDD - V(); I() = -1 mA			400	mV
903	Isc()lo	Short-Circuit Current lo		3			mA
904	Isc()hi	Short-Circuit Current hi				-2.5	mA

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD, VDDA, VDDB, VDDIN = 3.0...5.5 V, Tj = -40...125 °C, reference point GND unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Line Driver Outputs AO, NAO, BO, NBO, ZO, NZO							
B01	Vpk()max	Permissible Output Amplitude	VDD = 3 V, RL = 50 Ω vs. VDD/2			550	mV
B02	Vdc()	Output DC Voltage			VDD / 2		
B03	ΔVout()	Output Voltage Load Dependency	I() = 0...5 mA			50	mV
B04	Isc()lo	Short-Circuit Current lo	pin shorten to VDD/2	12		50	mA
B05	Isc()hi	Short-Circuit Current hi	pin shorten to VDD/2	-50		-12	mA
B06	Isc()	Output Current Limitation hi/lo	V() = 0...VDD		40	50	mA
B07	SR()hi, lo	Slew Rate hi/lo	CL() = 5 nF CL() = 50 pF	3 4			V / µs V / µs
B08	t_S	Settling Time	CL() = 5 nF, to 0.1% of final value			1	µs
B09	dbVlin	Output Linearity	100 kHz sine and diff. 1 Vpp output voltage; RL() > 1 kΩ RL() = 120 Ω	 80 60			 dB dB
B10	CLmax	Maximum Capacitive Output Load	no sustained oscillation		100		nF

PROGRAMMING

REGISTER MAP								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Configuration Registers [1]								
0x00	ROM Device ID[7:0]							
0x01	OGAIN[1:0]		SINGLEIN	FREQ[1:0]		GENTLE	DYNAMIC	TEMP
0x02	VEXT	XCELSIUS	OGAINZ[1:0]		MODEZ	BYPASSZ	SINGLEINZ	POLARITYZ
0x03	ERR_SIG	ERR_TEMP	ERR_EE	TALARM[2:0]			ENSIGZ	ENSIGAB
0x04	EN_NSTORE [2]			FILTER[1:0]		PDZ	PDB	PDA
0x05	CCELSIUS[3:0]				FCELSIUS[3:0]			
0x06	GAINZ[2]		OFSZ[5:0]					
0x07	GAINZ[1:0]		CGAINB[2:0]			CGAINA[2:0]		
0x08	COFSA[7:0]							
0x09	COFSB[7:0]							
0x0A	DGAINA[7:0]							
0x0B	DGAINB[7:0]							
0x0C	DOFSA[7:0]							
0x0D	DOFSB[7:0]							
0x0E	0	0	VC[1:0] [2]		CLKSLOW [2]	CLKDIV [2]	TEST_CLK [2]	PD_CELSIUS [2]
0x0F	Internal Checksum(7:0)							
0x10	0	TEST_ADC [2]	TEST_VGA [2]	TEST_PGA [2]	VTEST1 [2]	VTEST0 [2]	PD_BG [2]	TEST_BG [2]
0x11								
0x12	CELSIUS[7:0]							
0x13								
Internal State Machine Registers								
0x14	INTERNAL USE							
0x15	INTERNAL USE							
0x16	INTERNAL USE							
0x17	INTERNAL USE							
0x18	INTERNAL USE							
0x19	INTERNAL USE							
0x1A	INTERNAL USE							
0x1B	INTERNAL USE							
0x1C	INTERNAL USE							
0x1D	INTERNAL USE							
0x1E	INTERNAL USE							
0x1F	INTERNAL USE							
0x20	INTERNAL USE							
0x21	INTERNAL USE							
0x22	INTERNAL USE							
0x23	INTERNAL USE							
0x24	INTERNAL USE							
0x25	INTERNAL USE							
0x26	INTERNAL USE							
0x27	INTERNAL USE							
Peripheral Registers								
0x40	CELSIUSRAW[7:0]							
0x41				CHANNEL	OFS_P	OFS_N	GAIN_P	GAIN_N
0x42			EE_ERR	XERR_OUT	1OUTPUT	1INPUT	XSTORE	SIG_VALID

REGISTER MAP								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x43			EE_IRQ			1INPUT_IRQ	XS-TORE_IRQ	
Notes	[1] Only the configuration registers are user programmable. [2] Register bit for IC test only; must be kept on 0 for normal operation.							

Table 1: Register layout

I2C INTERFACE

Startup

An external I²C 1-kbit EEPROM (e.g. 24xx01 family) is used to store configuration parameters permanently. On power-up and after reset is released iC-TW3 accesses the external EEPROM and reads its device configuration according to Table 3.

EEPROM Checksum

The checksum at address 0x0F contains the 8-bit sum of registers 0x01 to 0x0E plus the 8-bit sum of all LUT bytes up to and including the final block with its breakpoint set to 255.

On startup iC-TW3 calculates the expected checksum and compares it with the value stored at EEPROM address 0x0F. If computed and stored address match normal operation begins. Otherwise, iC-TW3 asserts an error condition and pin NERR is pulled low.

It is the user's responsibility to store the correct checksum in the EEPROM during production programming.

CHECKSUM(7:0) Addr. 0x0F; bit 7:0		R/W
Code	Function	
...	Checksum of EEPROM contents: over 0x01 to 0x0E and 0x10 to 0x1B (minimum) over 0x01 to 0x0E and 0x10 to 0x6F (maximum)	

Table 2: Checksum

Note: As the checksum includes the LUT, breakpoint 255 must be assigned to the final block.

EEPROM Register Map

The 14 bytes of device configuration data are followed by a minimum of 2 to a maximum of 16 lock-up-table blocks (LUT). The LUT block size is 6 bytes each and the final block is indicated by its breakpoint value of 255.

Thus, a minimum of 28 bytes are read with 2 active LUT blocks and 112 bytes are read with 16 active LUT blocks during the configuration phase.

The last LUT block ist indicated by a breakpoint value of 255. Further descriptions on LUTs are given in section "Temperature Compensation" on page 22.

Note that the EEPROM address space maps to the 1-wire address 128. Accessing EEPROM address 0 is therefore equivalent to accessing memory location 128 via the 1-wire interface (see page 13).

EEPROM Address	**Description**	**Corresponding Configuration Register**
0x00	<reserved>	-
0x01	Config. 1	0x01
0x02	Config. 2	0x02
0x03	Config. 3	0x03
0x04	Config. 4	0x04
0x05	Temp. Sensing	0x05
0x06	Config. Index	0x06
0x07	Coarse Gain	0x07
0x08	COFSA	0x08
0x09	COFSB	0x09
0x0A	DGAINA	0x0A
0x0B	DGAINB	0x0B
0x0C	DOFSA	0x0C
0x0D	DOFSB	0x0D
0x0E	Test 1	0x0E
0x0F	CHECKSUM	0x0F
EEPROM Address	Description	LUT Block Number
0x10	Breakpoint 0	0
0x11	GAINA	0
0x12	GAINB	0
0x13	OFSA	0
0x14	OFSB	0
0x15	OFSZ	0
0x16	Breakpoint 1 (255)	1
0x17	GAINA	1
0x18	GAINB	1
0x19	OFSA	1
0x1A	OFSB	1
0x1B	OFSZ	1
. . .	. . .	. . .
0x6A	Breakpoint 255	15
0x6B	GAINA	15
0x6C	GAINB	15
0x6D	OFSA	15
0x6E	OFSB	15
0x6F	OFSZ	15

Table 3: EEPROM register map

1-WIRE INTERFACE

The 1-wire interface provides read and write access to the register bank and to the external EEPROM. When read access is not required an infrared phototransistor can be directly connected to the pin in order to build a cost effective wireless write-only port for in-field or production programming.

The communication bit stream is pulse-width modulated (PWM) as shown in Figure 1. A zero-bit is encoded as a short high followed by a long low. A one-bit is encoded as a long high followed by a short low.

The modulated signal is independent of the receiver or the transmitted clock frequency. Since iC-TW3 uses a free-running oscillator it is important to implement a robust, frequency insensitive protocol.

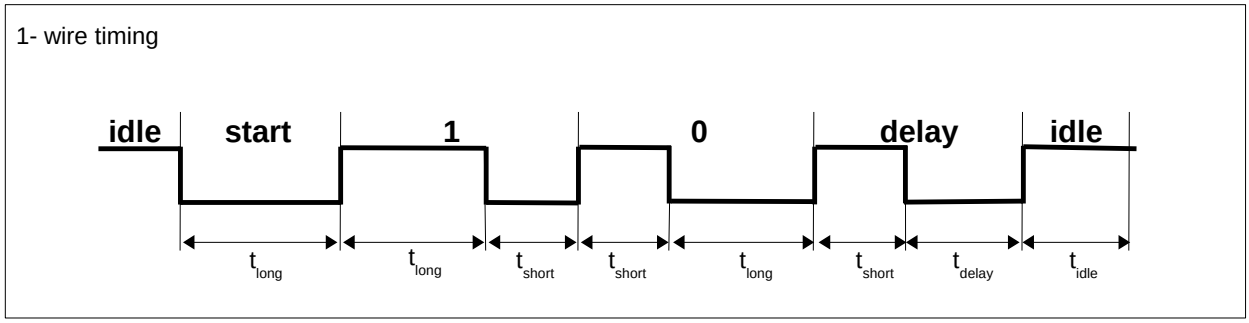


Figure 1: Pulse width modulation bit stream

Parameter	Description	min	max
t_{start}	Low time start condition (Master only)	1 ms	
t_{long}	Unit time long (Master and iC-TW3)	t_{short} + 10 µs	400 µs
t_{short}	Unit time short (Master and iC-TW3)	35 µs	t_{long} - 10 µs
t_{delay}	Delay on register read (iC-TW3 only)	35 µs	
t_{idle}	Interface idle before next access Access was write to external EEPROM Access was not write to external EEPROM	 8 ms 3 ms	

Table 4: 1-Wire interface timing

Addressing

The EEPROM address 0x00 maps to the 1-wire address 128. Accessing EEPROM address 0 is therefore equivalent to accessing memory location 128 through the 1-wire interface. All other 1-wire addresses are thus determined by adding 128 to the EEPROM address of interest.

Write Sequence

Figure 2 describes the write sequence of the 1-wire interface. On an idle wire, a write sequence is initiated by generating a start condition followed by the write command (000) and by the address and register data.

Read Sequence

A read sequence is depicted in Figure 3. After the start condition the read command (001) is followed by the register address. The master then releases the wire and iC-TW3 begins to pull low while internally accessing the data. When the data is ready it is produced while following the same PWM rules valid for the master.

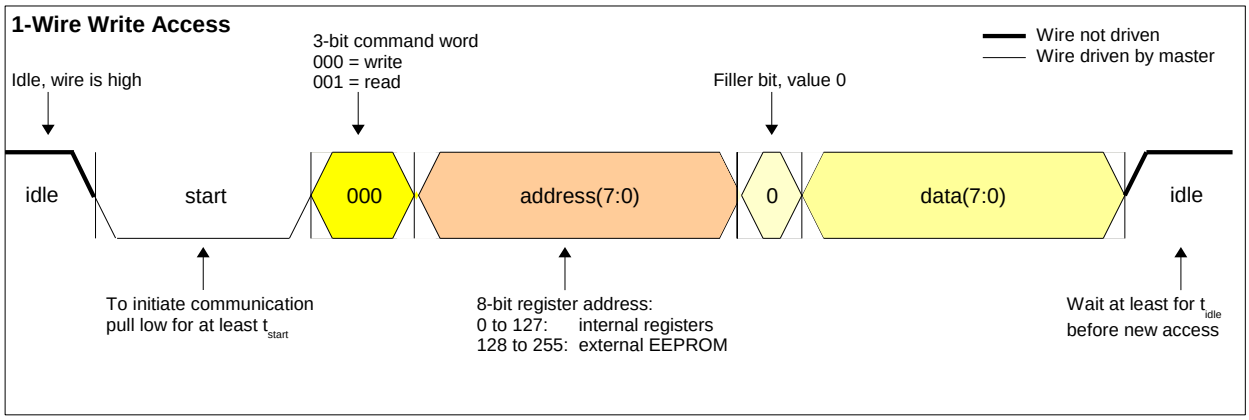


Figure 2: Register write sequence

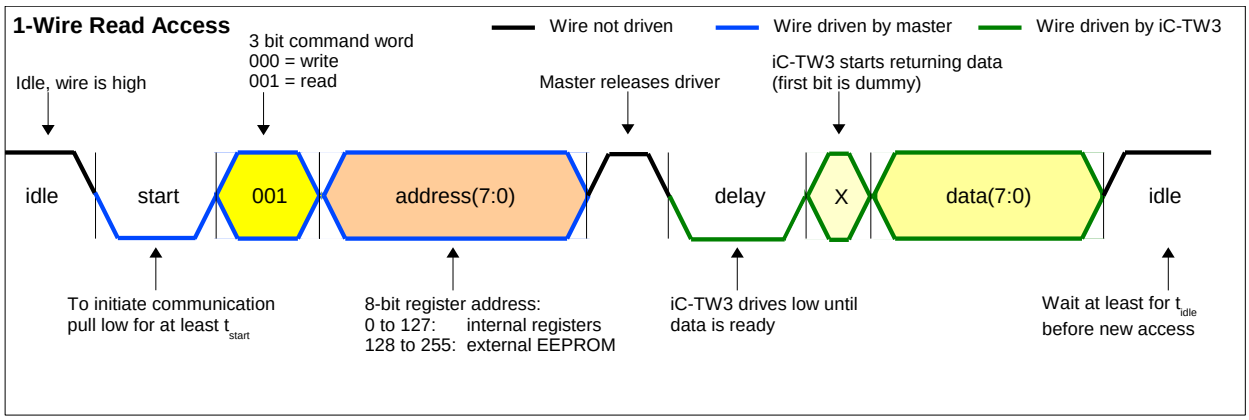


Figure 3: Register read sequence

A/B SIGNAL PATH

iC-TW3 incorporates two analog gain paths called channel A and B, respectively. Gain and offset of both paths are independently controlled and temperature compensated. Figure 4 depicts a diagram of a single signal path, Table 5 below summarizes gain and offset characteristics.

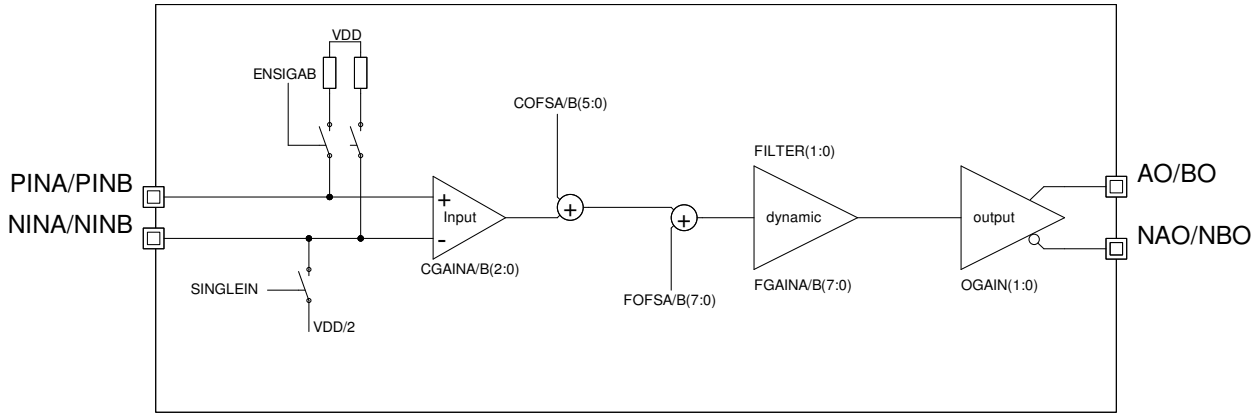


Figure 4: The A/B signal path

	Input Amplifier	Dynamic Amplifier	Output Amplifier	Composite
Gain range	0..36 dB	-2..18.4 dB	-3 dB, 0 dB, 6 dB	-5..60 dB
Gain step	6.0 dB	0.08 dB		
Offset range input referred	$\frac{\pm 1.24\ V}{gain_{input}}$	$\frac{\pm 0.25\ V}{gain_{input}}$		$\frac{\pm 1.49\ V}{gain_{input}}$
Offset step input referred	$\frac{40\ mV}{gain_{input}}$	$\frac{2\ mV}{gain_{input}}$		
	$gain_{input} = 10^{\frac{gain\_of\_input\_amplifier\_in\_dB}{20}}$			

Table 5: Overview of gain and offset characteristics

Single ended signals

Single ended input functionality is provided by connecting the negative input terminal (pins NINA and NINB) to an internally generated voltage of $V_{DD}/2$. This is enabled by setting the control bit *SINGLEIN* to 1. Alternatively, an externally generated reference voltage may be applied to the negative input terminals.

SINGLEIN	Addr. 0x01; bit 5	R/W
Code	Function	
0	A and B inputs are differential *(default)*	
1	A and B inputs are single ended	

Table 6: Single ended input functionality

Input error detection

Weak input pull-up resistors are enabled by setting control bit *ENSIGAB* to 1. The resistors are at minimum 2.0 MΩ. When driving the input with a high impedance source it might be necessary to disable the pull-up resistors to avoid excessive signal distortion. The pull-up resistors are used to sense floating or damaged sensor connections. Any input terminal left unconnected is pulled to V_{DD} and triggers a sensor error condition *err_sig*.

ENSIGAB	Addr. 0x03; bit 0	R/W
Code	Function	
0	Pull-up resistors disconnected and error reporting disabled (default)	
1	Pull-up resistors and error reporting active on A/B inputs	

Table 7: Input signal error detection control

Gain and offset

Registers *CGAINA(2:0)* and *CGAINB(2:0)* are used to set the coarse gain. Coarse gain is static and it is not changed by the temperature or automatic compensation algorithm.

The highest legal value for *CGAINA(2:0)* and *CGAINB(2:0)* is 6. Equivalently registers *COFSA(5:0)* and *COFSB(5:0)* are used to control the static offset of the input signal. Note that *COFSA(5:0)* and

COFSB(5:0) are in 2's complement format and their value range is limited from -31 to +31.

CGAINA(2:0)	Addr. 0x07; bit 2:0	R/W
CGAINB(2:0)	Addr. 0x07; bit 5:3	R/W
Code	*gain = cgain x 6 dB*	
0x00	0 dB (default)	
0x01	6 dB	
...		
0x06	36 dB	

Table 8: Coarse gain select for channel A/B

COFSA(7:0)	Addr. 0x08; bit 7:0	R/W
COFSB(7:0)	Addr. 0x09; bit 7:0	R/W
Code 2'K	Code 5:0, and decimal	*offset = cofs x 40 mV*
0xE1	0x21, -31	-1240 mV
...	...	
0xFF	0x3F, -1	-40 mV
0x00	0x00, 0	0 mV (default)
0x01	0x01, +1	40 mV
...	...	
0x1F	0x1F, +31	1240 mV

Table 9: Coarse offset select for channel A/B

DGAINA(7:0)	Addr. 0x0A; bit 7:0	R/W
DGAINB(7:0)	Addr. 0x0B; bit 7:0	R/W
Code	*gain = dgain x 0.08 dB - 2 dB*	
0x00	-2 dB (default)	
...		
0x19	0 dB	
0x1A	0.08 dB	
...		
0xFF	18.4 dB	

Table 10: Dynamic gain select for channel A/B

DOFSA(7:0)	Addr. 0x0C; bit 7:0	R/W
DOFSB(7:0)	Addr. 0x0D; bit 7:0	R/W
Code	*offset = cofs x 2 mV*	
0x81	-254 mV	
...		
0xFF	-2 mV	
0x00	0 mV (default)	
0x01	2 mV	
...		
0x7F	254 mV	

Table 11: Dynamic offset select for channel A/B

Value *FGAINA/B* and *FOFSA/B* are fine gain and offset control respectively. They are calculated dynamically according to the temperature compensation algorithm. **In case temperature compensation is not enabled the values of FGAINA/B and FOFSA/B are equal to the register values in DGAINA/B(7:0) and DOFSA/B(7:0)**. Refer to chapter "Temperature Compensation" on page 22 for a detailed explanation of fine gain and fine offset calculations. *DGAINA/B(7:0)* and *DOFSA/B(7:0)* can be programmed to a fixed value or it is automatically updated when dynamic adaption is enabled.

Output driver

The output amplifier is capable of driving a 100 Ω differential load and is stable with capacitive loads of up to 100 nF. Control register *OGAIN(1:0)* is used to select the output amplifier gain. A gain of -3 dB is useful to accommodate input signals larger than 1 V and gain of +6 dB will provide a 1 Vpp single-ended output. Note that the selected output amplifier gain will influence the automatic gain compensation. Refer to section "Automatic Compensation" on page 19 for details.

OGAIN(1:0)	Addr. 0x01; bit 7:6	R/W
Code	Function	
0x00	0 dB (default)	
0x01	Reserved	
0x02	+6 dB	
0x03	-3 dB	

Table 12: Output amplifier gain on channel A/B

A programmable 1st-order low-pass filter can be enabled to limit the path bandwidth. The filter cut-off frequency can be set via the *FILTER(1:0)* register.

FILTER(1:0)	Addr. 0x04; bit 4:3	R/W
Code	Function	
0x00	1 MHz (default)	
0x01	500 kHz	
0x02	200 kHz	
0x03	reserved	

Table 13: Signal path filter

In order to save power the complete signal path can be disabled using the control bits *PDA* and *PDB* respectively. When disabled the outputs are high impedance. The dynamic adaption should be disabled when either channel A or B is disabled.

PDA	Addr. 0x04; bit 0	R/W
PDB	Addr. 0x04; bit 1	R/W
Code	Function	
0	Channel A/B is enabled (default)	
1	Channel A/B is powered down	

Table 14: Power down control on channel A/B

Z SIGNAL PATH (INDEX)

A third analog path is used for index signal processing frequently found in encoder applications. Refer to Figure 5 for an overview. An input amplifier with a gain range of 0 to 36 dB is used to amplify the index signal to an intermediate level. The input amplifier employs output referred offset correction. This is used to eliminate inherent amplifier offset as well as sensor offset. Additionally, the same offset correction is used to skew the comparator shift point to a desired level. The offset correction is temperature compensated with a LUT.

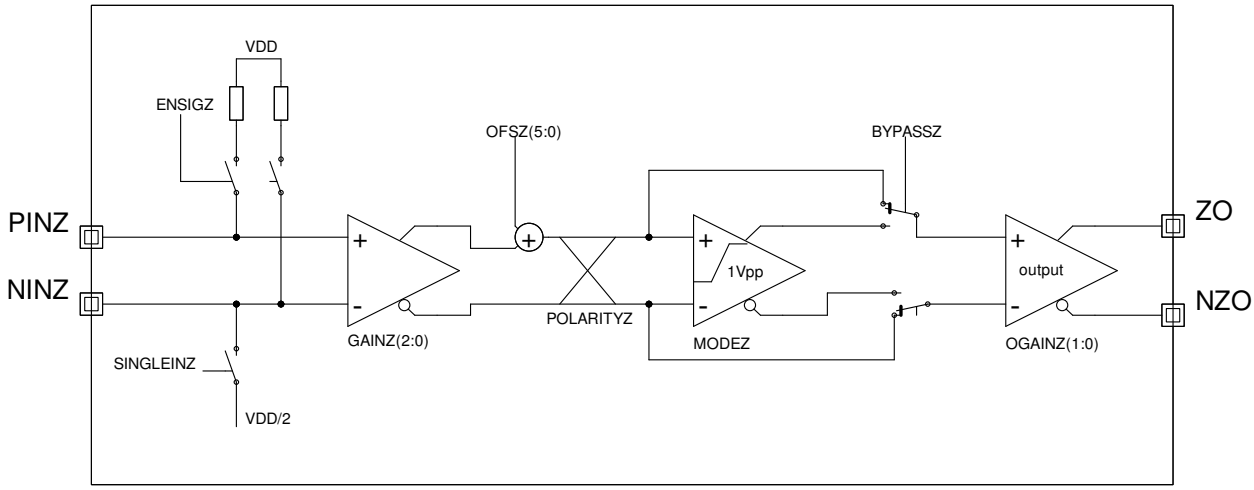


Figure 5: The Z signal path

	Input Amplifier	Output Amplifier	Composite
Gain range	0..36 dB	-3 dB, 0 dB, 6 dB	-3..42 dB
Gain step	6 dB		
Offset range input referred	$\frac{\pm 1.86\ V}{gain_{input}}$	$\frac{\pm 1.86\ V}{gain_{input}}$	
Offset step input referred	$\frac{60\ mV}{gain_{input}}$		
	$gain_{input} = 10^{\frac{gain\_of\_input\_amplifier\_in\_dB}{20}}$		

Table 15: Gain and offset characteristics for channel Z

A single ended input referenced to $V_{DD}/2$ is provided by setting bit *SINGLEINZ* of register 0x02. Alternatively, pin NINZ can be biased with an external voltage.

SINGLEINZ	Addr. 0x02; bit 1	R/W
Code	Function	
0	Channel Z input is differential (default)	
1	Channel Z is single ended	

Table 16: Single ended input functionality

A zero-crossing comparator generates a 1.0 $V_{peak-peak}$ output signal or a rail-to-rail signal depending on control bit *MODEZ*. The comparator can be bypassed which allows using the Z Path as a regular amplifier path. Bypassing can be toggled via bit *BYPASSZ* of register 0x02.

MODEZ	Addr. 0x02; bit 3	R/W
Code	Function	
0	1 Vpp out (default)	
1	Rail-to-rail output (requires OGAINZ(1:0) set to 0x2)	

Table 17: Channel Z output mode select

BYPASSZ	Addr. 0x02; bit 2	R/W
Code	Function	
0	Comparator is enabled (default)	
1	Comparator is bypassed	

Table 18: Channel Z comparator bypass

Gain and offset

Gain and offset selections on channel Z are made available by providing control bits *GAINZ(2:0)* and *OFSZ(5:0)*. Note that the maximum value for gain on channel Z is 6 which corresponds to a total gain of 36 dB.

GAINZ(2:0) is split up amongst register 0x06 which holds the MSB and register 0x07 holding the other two bits. *OFSZ(5:0)* is the correction value to the output of the input amplifier and is interpreted as 2's complement. The input referred offset is therefore gain dependent.

The output gain on channel Z can be set via control bits *OGAINZ(1:0)*. For more details again refer to section "A/B PATH" on page 15.

GAINZ(2:0)	Addr. 0x06; bit 7 Addr. 0x07; bit 1:0	R/W
Code	*gain = gainz x 6 dB*	
0x00	0 dB (default)	
0x01	6 dB	
...		
0x06	36 dB	

Table 19: Gain select for channel Z

OFSZ(5:0)	Addr. 0x06; bit 5:0	R/W
Code 2'K	Decimal	*offset = cofs x 60 mV*
0x21	-31	-1860 mV
...	...	
0x3F	-1	-60 mV
0x00	0	0 mV (default)
0x01	+1	60 mV
...	...	
0x1F	+31	1860 mV

Table 20: Offset select for channel Z

OGAINZ(1:0)	Addr. 0x02; bit 5:4	R/W
Code	Function	
0x00	0 dB (default)	
0x01	Reserved	
0x02	+6 dB	
0x03	-3 dB	

Table 21: Output amplifier gain on channel Z

Input error detection

Pull-up resistor and error detection on channel Z can be controlled by bit *ENSIGZ* of register 0x03, disabling of the complete Z path can be achieved by setting bit *PDZ* of register 0x04 to 1. For more detailed information on pull-up and power control refer to section "A/B PATH" on page 15 as the behaviour of index path and signal path equal regarding these matters.

ENSIGZ	Addr. 0x03; bit 1	R/W
Code	Function	
0	Pull-up resistors disconnected and error reporting disabled (default)	
1	Pull-up resistors and error reporting active on *inZ*	

Table 22: Input signal error detection control

PDZ	Addr. 0x04; bit 2	R/W
Code	Function	
0	Channel Z is enabled (default)	
1	Channel Z is powered down	

Table 23: Power-down control on channel Z

Polarity of channel Z

Furthermore, the polarity on channel Z can be inverted by setting or not setting bit *POLARITYZ*.

POLARITYZ	Addr. 0x02; bit 0	R/W
Code	Function	
0	Channel Z has normal polarity (default)	
1	Channel Z has inverted polarity	

Table 24: Channel Z polarity select

AUTOMATIC COMPENSATION

Automatic gain and offset correction is available for dual sensor bridges that are 90° out of phase. These types of sensors are used for encoder applications.

Automatic compensation removes any sensor offset and sets the gain to achieve a fixed output voltage. The target output voltage depends on the output gain *OGAIN(1:0)* as well as on the control bit *VEXT*. When using an external reference voltage, the appropriate voltage must be applied to pin VC.

VEXT	Addr. 0x02; bit 7	R/W
Code	Function	
0	Internally generated 1 V or 2 V is used as output target voltage, depending on register *OGAIN(1:0)*.	
1	Voltage applied to pin VC defines target output voltage (see Table 26).	

Table 25: Target voltage selection

OGAIN(1:0)	Output Gain	*VEXT*	Target Output Voltage V_{ppdiff}
00	0 dB	0	1 V
01	reserved	0	
10	6 dB	0	2 V
11	-3 dB	0	1 V
00	0 dB	1	2.21 V - VC
01	reserved	1	
10	6 dB	1	(2.21 V - VC) x 2
11	-3 dB	1	2.21 V - VC

Table 26: Target output voltages

Automatic compensation is enabled by setting control bit *DYNAMIC* of register 0x01 to 1. If enabled, it will constantly alter register *DOFSA/B* and *DGAINA/B* to maintain zero offset and the target output amplitude. Control bits *FREQ(1:0)* of register 0x01 are used to limit the tracking rate. If the input frequency increases above the limit tracking will stop. Normally, it is not required to limit the tracking frequency although it can be useful for certain bandwidth limited sensors.

DYNAMIC	Addr. 0x01; bit 1	R/W
Code	Function	
0	Automatic function is disabled	
1	Automatic function is enabled	

Table 27: Automatic compensation enable

Note that setting *FREQ(1:0)* to other values than 0 does not affect the signal bandwidth of the amplifier. It merely limits the rate of automatic adaption.

FREQ(1:0)	Addr. 0x01; bit 4:3	R/W
Code	Function	
00	No tracking limit (default)	
01	200 kHz	
10	20 kHz	
11	2 kHz	

Table 28: Automatic compensation adaption rate

In normal operation the compensation algorithm will adjust both gain and offset simultaneously in order to achieve fast convergence. If control bit *GENTLE* of register 0x01 is set, gain and offset registers are updated alternately. This reduces output jumpiness at the expense of slower convergence.

GENTLE	Addr. 0x01; bit 2	R/W
Code	Function	
0	Gain and offset are updated simultaneously	
1	Gain and offset are updated alternately	

Table 29: Automatic compensation sequence control

Automatic compensation can be used in conjunction with temperature compensation. Automatic compensation will then remove any residual offset or gain mismatch not corrected by the temperature correction algorithm.

Limitation

The automatic compensation measures the amplitude and offset at the output of iC-TW3. In order to provide meaningful information the output signals must be of reasonable encoder quality at all times. They need to be 90° out of phase and most importantly the amplitude must be larger than 0.5 V peak-peak differential (larger than 0.25 V peak-peak single ended) whereas the offset must be less then +/- 0.25 V. In situations where the minimum amplitude is not guaranteed, e.g by removing the MR input sensor from the magnetic source, wrong offset and gain control correction data might be generated.

TEMPERATURE SENSING

iC-TW3 contains an on-chip temperature sensor. Optionally, an external sensor can be used by setting bit *XCELSIUS* of register 0x02 to 1. An external temperature sensor is useful for remote temperature sensing or in situations where the internal sensor does not provide adequate accuracy. Also, device self-heating due to heavy output loads can have an impact on the internal sensor readings. Connect the external temperature sensor with its analog output to pin KELVIN.

XCELSIUS	Addr. 0x02; bit 6	R/W
Code	Function	
0	Select internal temperature sensor (default)	
1	Select external temperature sensor	

Table 30: Temperature sensor select

An ADC converts the analog temperature signal into an 8-bit digital word. In case the on-chip sensor is used the 8-bit value spans a temperature range of -50 °C to 150 °C. It is recommended to calibrate the ADC using register 0x05 even when using an external temperature sensor.

Calibrating the temperature ADC

The raw ADC value can be accessed through register 0x40. A ±2 increment hysteresis is applied to the ADC value to remove conversion noise and the offset register 0x05 is added. The final value is stored in register 0x12 and is used for temperature compensation.

To achieve best temperature accuracy it is required to calibrate the ADC by correctly programming register 0x05. At any known ambient temperature the register 0x05 is programmed such to read the expected ADC value. As an example, consider the product assembly floor with an ambient temperature of 20 °C. Due to device variation the ADC value read before calibration can be anything between 0 °C to 40 °C. Register 0x05 is now used to tune the ADC output value to the correct binary representation of 20 °C.

CCELSIUS(3:0)	Addr. 0x05; bit 7:4	R/W
Code	Bit 3 is sign, bits 2:0 are magnitude of correction	
1111	Most negative correction	
...	...	
1001	Least negative correction	
1000	No correction	
0000	No correction (default)	
0001	Least positive correction	
...	...	
0111	Most positive correction	

Table 31: Coarse offset correction

FCELSIUS(3:0)	Addr. 0x05; bit 3:0	R/W
Code	Value added to ADC reading is FCELSIUS(3:0) - 8	
0000	-8 (default)	
0001	-7	
...	...	
1111	7	

Table 32: Fine offset correction

CELSIUS(7:0)	Addr. 0x12; bit 7:0	R
Data	Function	
0x00 0xFF	Current temperature ADC value that is used for compensation calculations. Value of this register is 0x40 + *FCELSIUS(3:0)* - 8	

Table 33: Temperature data

Temperature alarm

The iC-TW3 features a built-in temperature alarm system. An alarm threshold can be specified by the user via the *TALARM(2:0)* bits in register 0x03. A temperature alarm is asserted once the temperature value generated by the ADC is above the defined threshold. The alarm is indicated by the *ERR_TEMP* bit set to 1 as well as by pin NERR going low.

TALARM(2:0)	Addr. 0x03; bit 4:2	R/W
Code	$temp_{threshold}$ = (*TALARM(2:0)* x 16) + 144	
000	144 (default)	
001	160	
...	...	
110	240	
111	Alarm disabled	

Table 34: Temperature alarm threshold

ERROR CONDITIONS

iC-TW3 maintains three status bits reporting system error conditions. These bits are *ERR_EE, ERR_TEMP* and *ERR_SIG* of register 0x03. If any error condition is triggered, i.e. indicated by any of these bits being set to 1, this will also assert pin NERR pulling it low.

ERR_EE	Addr. 0x03; bit 5	R
Code	Error message	
0	No error since the last reset	
1	One of the following error conditions has occurred since the last reset: 1. EEPROM checksum error* 2. EEPROM read error 3. EEPROM write error	
Notes	This error message can not be disabled and its bit status is maintained until the device is reset. *) A permanent logic zero read at SDA does not lead to a checksum error.	

Table 35: EEPROM data error

ERR_TEMP	Addr. 0x03; bit 6	R
Code	Error message	
0	ADC reading is below value defined in register *TALARM(2:0)*	
1	ADC reading is above value defined in register *TALARM(2:0)*	
Notes	This error is not latched. Disabling temperature monitoring is possible by setting *TALARM(2:0)* to '111'.	

Table 36: Temperature alarm

ERR_SIG	Addr. 0x03; bit 7	R
Code	Error message	
0	All input terminals are connected	
1	An input terminal is left unconnected	
Notes	This error is not latched. To enable this alarm *ENSIGAB* or *ENSIGZ* must be set 1.	

Table 37: Signal unconnected alarm

TEMPERATURE COMPENSATION

Temperature compensation is enabled by setting control bit *TEMP* of register 0x01. A piece-wise linear interpolation of values stored in a look-up-table (LUT) is employed to calculate the gain and offset for a given temperature. Figure 6 shows a sample configuration with seven breakpoints.

TEMP	Addr. 0x01; bit 0	R/W
Code	Function	
0	Temperature compensation is disabled (default)	
1	Temperature compensation is enabled	

Table 38: Temperature compensation enable

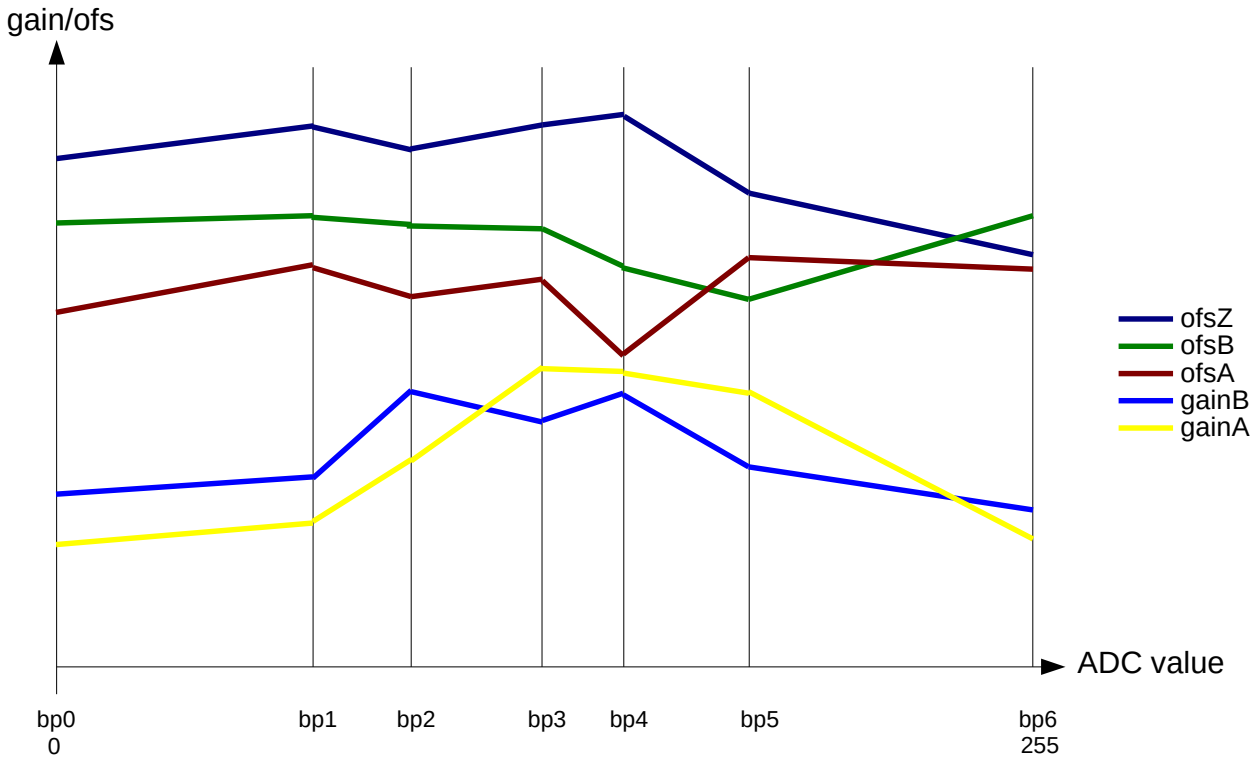


Figure 6: LUT with seven breakpoints

There can be a minimum of two up to a maximum of 16 temperature breakpoints within the LUT. Each breakpoint has five interpolation values associated to it namely *GAINA, GAINB, OFSA, OFSB* and *OFSZ*. For more details on the layout of the LUT refer to section "EEPROM" on page 12.

Breakpoints can be placed freely across the temperature axis except for the first and the last breakpoint. The first breakpoint must be located at ADC value 0 (which roughly corresponds to -50 °C when using the internal sensor), the last breakpoint must be located at ADC value 255 (150 °C with the internal sensor).

The LUT is stored in the off-chip EEPROM from memory location 0x10 onward. Note that the EEPROM address space maps to the 1-wire address 128. Accessing EEPROM address 0 is therefore equivalent to accessing memory location 128 through the 1-wire interface. The breakpoint entry with a value of 255 marks the last valid LUT entry. All addresses thereafter including their data will be ignored.

Temperature dependent gain and offset is determined by performing linear interpolation between breakpoints. Temperature dependent gain and offset are *TGAINA/B* and *TOFSA/B* respectively.

Fine gain *FGAINA/B* and fine offset *FOFSA/B* (see figure 4 on page 15) are calculated as follows:

$$fgain = tgain + dgain$$

$$fofs = tofs + dofs$$

Whereas *TGAIN* and *TOFS* are the temperature dependent values calculated using the LUT and *DGAIN* and

DOFS are registers updated either manually or by the automatic compensation function.

Example: Assuming the temperature is divided into 2 breakpoints only, with the first BP at position 0 (value BP0) and the second BP at position 255 (value BP255).

Linear interpolation is performed between these breakpoints and the tgain value is calculated as follows:

tgain = temperature * (BP255 – BP0) / 256

Note that automatic compensation should be turned off, otherwise dgain will counteract the changes of tgain.

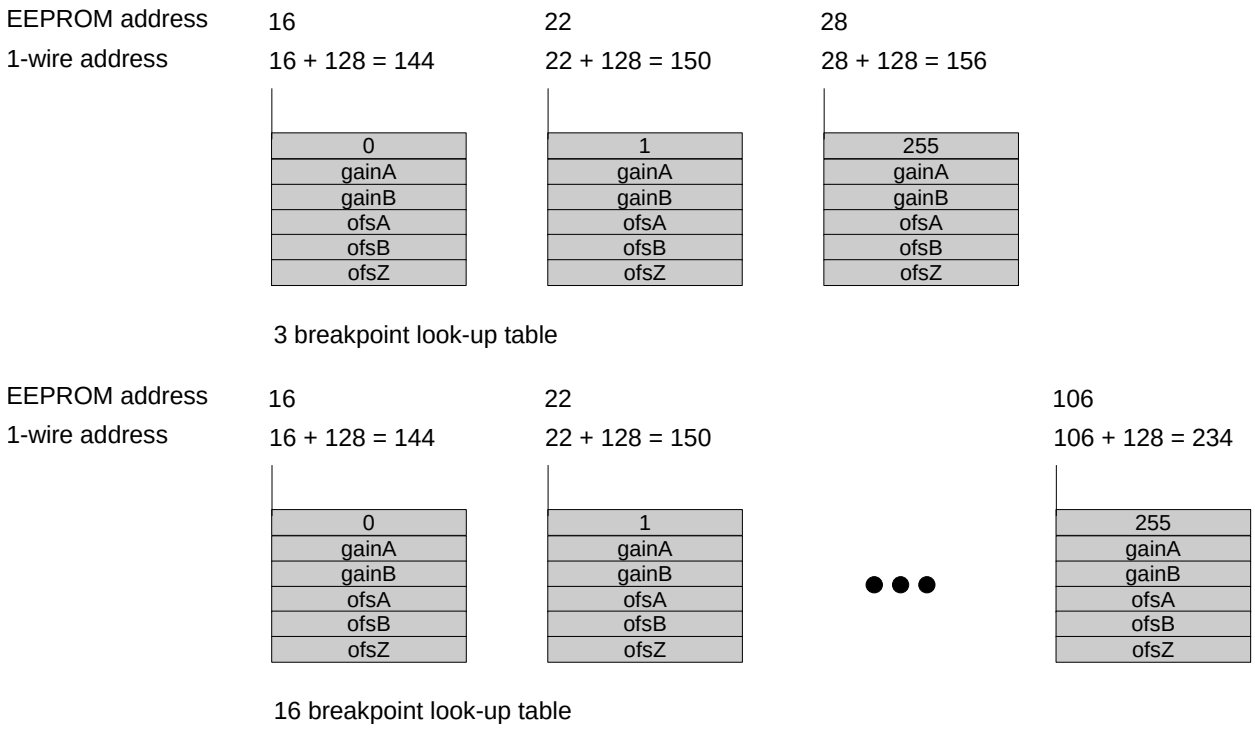


Figure 7: Temperature LUT memory map

TEST MODES

The iC-TW3 has two registers 0x0E and 0x10 which provide access to basic test functions. With the bit *PD_CELSIUS* the internal temperature sensor can be switched off. When the temperature sensor is off, the output value of the temperature sensor can be forced to a desired value by writing to register 0x40. The user can then test the compensation circuit without changing the device temperature.

Note: The read value of 0x40 is moved by one bit, ie. 0x20 is returned after writing 0x10.

PD_CELSIUS	Addr. 0x0E; bit 0	R/W
Code	Function	
0	Temperature sensor enabled (default)	
1	Temperature sensor disabled	

Table 39: Temperature sensor power control

TEST_CLK	Addr. 0x0E; bit 1	R/W
Code	Function	
0	Clock is not driven on any pin (default)	
1	Clock is driven on pin NERR	

Table 40: Internal clock oscillator

CLKDIV	Addr. 0x0E; bit 2	R/W
Code	Function	
0	$f_{system} = f_{osc} / 2$ (default)	
1	$f_{system} = f_{osc}$	

Table 41: Internal clock divider selection

TYPICAL APPLICATIONS

A typical application is shown in figure 8. Three differential MR sensor bridges are connected to the iC-TW3. A, B and Z outputs are driving 120Ω terminated transmission lines.

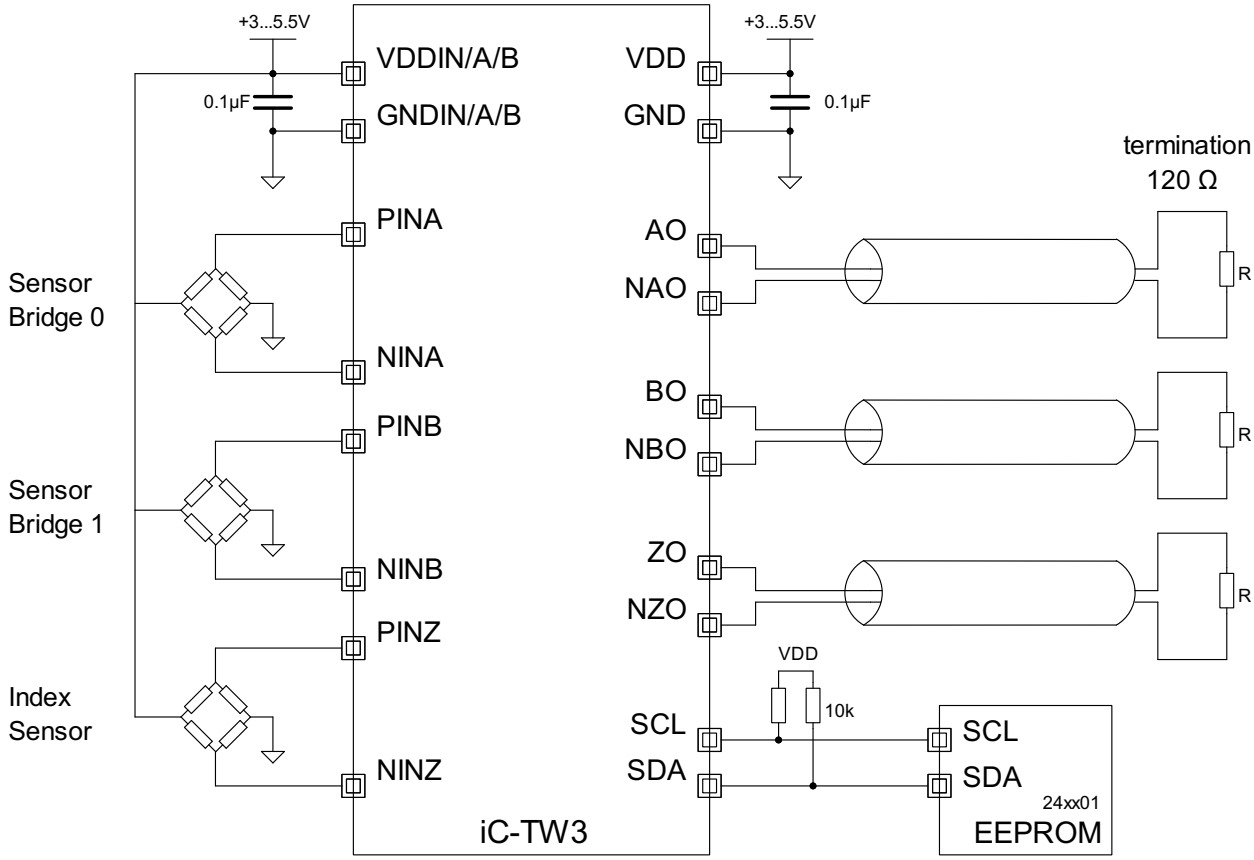


Figure 8: Typical application MR Sensors

REVISION HISTORY

Rel.	Rel. Date*	Chapter	Modification	Page
B2	2017-08-07	BLOCK DIAGRAM	Update of block diagram	1
		PACKAGING INFORMATION	QFN with top marking, revision of footnote, update of QFN package drawing	3ff
		I2C INTERFACE	Table 2: contents supplemented; text moves to grey note boxes.	12
		AUTOMATIC COMPENSATION	'Limitation' paragraph added.	19
		ORDERING INFORMATION	P/O code of eval board	26

Rel.	Rel. Date*	Chapter	Modification	Page
B3	2023-02-07	BLOCK DIAGRAM	Update of block diagram: correction of Z path	1
		ABSOLUTE MAXIMUM RATINGS	G009 added for Ptot; G011 Storage temperature moved to Thermal Data	5
		REGISTER MAP	Clarification of test bits	11
		I2C INTERFACE	Note box updated and relocated	12
		TEMPERATURE COMPENSATION	Example added for tgain	23
		TEST MODES	Update of description, Table 41: default value is zero	23

* Release Date format: *YYYY-MM-DD*

ORDERING INFORMATION

Type	Package	Order Designation
iC-TW3	32-pin QFN, 5 mm x 5 mm, thickness 0.9 mm, RoHS compliant	iC-TW3 QFN32
Evaluation board		iC-TW3 EVAL TW3D_2D

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