iC-RZ Series OPTICAL
TWIN-SCAN ENCODER IC WITH SAFETY CHANNEL

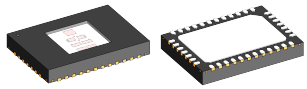
FEATURES

- Separate and independent 2-channel scanning
- Control/Safety Channel scan different positions of the code disc
- Fixed code disc diameters of 26.5 mm or 42.5 mm
- Control Channel (CC) features:
  - 10-bit Pseudo-random Code (PRC)
  - 5-bit real-time interpolator (1024 CPR sine/cosine)
  - Auxiliary sine/cosine scanning with differential analog outputs
  - BiSS interface
  - MT interface (SSI)
  - Pin-selectable modes of operation
  - Diagnostics (e.g Sin/Cos DC monitor)
- Safety Channel (SC) features:
  - 10-bit Pseudo-random Code (PRC)
  - 5-bit real-time interpolator (1024 CPR sine/cosine)
  - BiSS/SPI interface
  - MT interface (SSI)
  - Configuration via BiSS, SPI and I^2C from ext. EEPROM
  - Diagnostics (e.g Sin/Cos AC monitor)
  - On-chip temperature sensor

APPLICATIONS

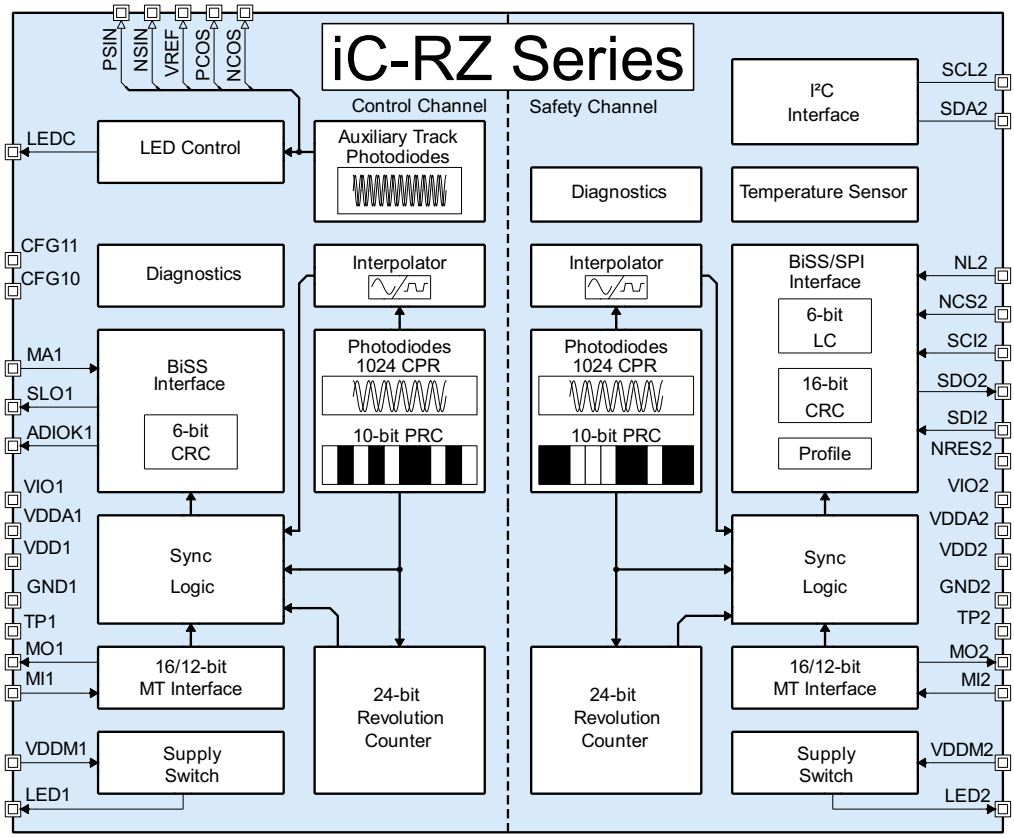
- High-resolution optical encoder for external interpolation (up to 24 bits using iC-MR3)
- Functional Safety Encoder

PACKAGES



38-pin optoQFN
7.0 mm x 5.0 mm x 1.0 mm
RoHS compliant

BLOCK DIAGRAM



DESCRIPTION

iC-RZ is an advanced optical sensor IC for transmissive encoders, with integrated photodiodes for reliable and redundant scanning of a code disc with 3 different tracks:

1. Incremental track (1024 CPR sine/cosine)
2. Pseudo-random Code track (10-bit PRC)
3. Auxiliary track (AT) (sine/cosine CPR is determined by the device version)

To do this, the iC-RZ is divided into two autonomous channels called Control Channel (CC) and Safety Channel (SC).

The Control Channel generates a 15-bit absolute position value by scanning the absolute 10-bit PRC track and the incremental track (1024 CPR sine/cosine). In doing so, the scanning of the PRC is synchronized with the 1024 CPR sine/cosine signals, which are further resolved by a 5-bit real-time interpolator.

The Safety Channel operates in exactly the same way, meaning that position data generation is fully redundant: the Control Channel generates the Control Position Word (CPW), and the Safety Channel the Safety Position Word (SPW).

The absolute position value of the CPW is output via a serial BiSS Interface using a 6-bit CRC. This data matches in phase with the sine/cosine signals generated from the auxiliary track, which are output as voltage signals over low-impedance buffers. It is therefore possible to increase the resolution of the CPW by connecting an external interpolator, preferably iC-MR3, featuring signal-conditioning to increase the position accuracy.

The absolute position value of the SPW is output via a serial BiSS/SPI Interface using a 16-bit CRC and 6-bit sign-of-life counter (LC). A standard SSI output is also possible, but without nE, nW, CRC and LC.

Each channel uses its absolute 10-bit PRC track photodiodes to capture and count revolutions (embedded 24-bit revolution counter). These revolution counters can be supplied from an independent external energy source (e.g. a battery).

An optional multiturn value (12 bit or 16 bit) can be read by the Control Channel and the Safety Channel through the MT interface of each channel, using the SSI protocol. This multiturn data is synchronized to the internally generated singleturn absolute value.

All integrated photodiodes used for the incremental scanning of sine/cosine signals are arranged as an *HD Phased Array*, providing excellent signal fidelity at relaxed alignment tolerances.

For safety-related applications the appropriate Safety Implementation Manual has to be considered.

General notice on materials under excessive conditions
Epoxy resins (such as solder resists, IC package and injection molding materials, as well as adhesives) may show discoloration, yellowing, and general surface changes when exposed long-term to high temperatures, humidity, irradiation, or due to thermal treatments for soldering and other manufacturing processes.

Equally, standard molding materials used for IC packages can show visible changes induced by irradiation, among others when exposed to light of shorter wavelengths, for instance, blue light. Such surface effects caused by visible or IR LED light are rated to be of cosmetic nature, without influence on the chip's function, its specifications or reliability.

Note that any other materials used in the system (e.g. varnish, glue, code disc) should also be verified for irradiation effects.

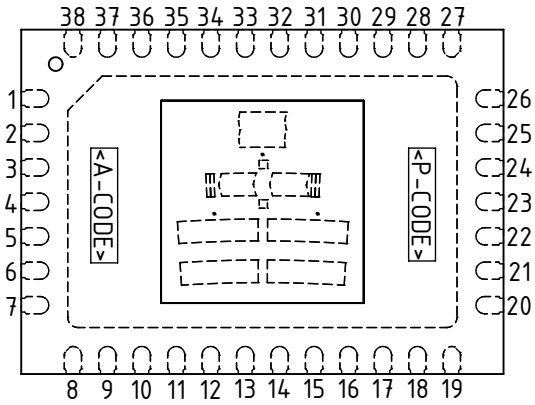
General notice on application-specific programming
Parameters defined in the datasheet represent supplier's attentive tests and validations, but - by principle - do not imply any warranty or guarantee as to their accuracy, completeness or correctness under all application conditions. In particular, setup conditions, register settings and power-up have to be thoroughly validated by the user within his specific application environment and requirements (system responsibility).

The chip's performance in application is impacted by system conditions like the quality of the optical target, the illumination, temperature and mechanical stress, sensor alignment and initial calibration.

CONTENTS

PACKAGING INFORMATION

PIN CONFIGURATION
oQFN38-7x5



PIN FUNCTIONS

No.	Name	Function
1	NCOS	Cosine Output, negative (CC [3])
2	PCOS	Cosine Output, positive (CC)
3	VREF	Reference Voltage Output (CC)
4	PSIN	Sine Output, positive (CC)
5	NSIN	Sine Output, negative (CC)
6	TP1	Test Input 1 (CC)
7	ADIOK1	Status Output [6] (CC)
8	MO1	MT Interface, clock output (CC)
9	MI1	MT Interface, data input (CC)
10	CFG11	Configuration Input 1 (CC)

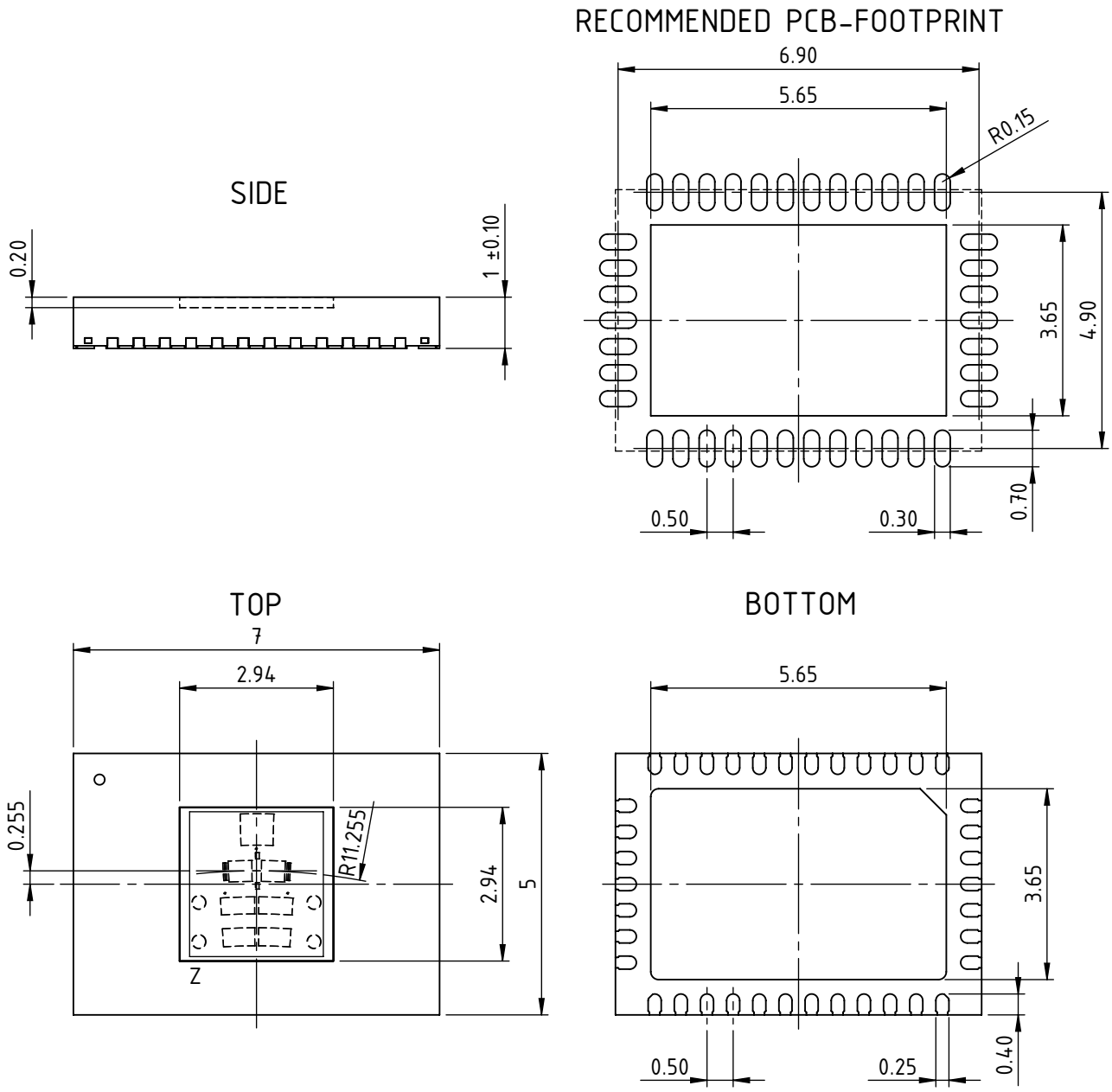
PIN FUNCTIONS

No.	Name	Function
11	CFG10	Configuration Input 0 (CC)
12	MA1	BiSS Interface, clock input (CC)
13	SLO1	BiSS Interface, data output (CC)
14	SCL2	I^2C Interface, clock line (SC [4])
15	SDA2	I^2C Interface, data line (SC)
16	SDO2	BiSS/SPI Interface, data output (SC)
17	SCI2	BiSS/SPI Interface, clock input (SC)
18	SDI2	BiSS/SPI Interface, data input (SC)
19	n.c. [1]	
20	NCS2	SPI Interface, chip select input [2] (SC)
21	NL2	SPI Interface, latch input [2] (SC)
22	MI2	MT Interface, data input (SC)
23	MO2	MT Interface, clock output (SC)
24	NRES2	REBOOT input/indication output (SC)
25	TP2	Test Input 2 (SC)
26	VIO2	+2.5 V...+5 V I/O Supply Voltage [7] (SC)
27	VDDM2	+3 V...+5 V MT Supply Voltage [8] (SC)
28	VDDA2	+5 V Analog (Supply Voltage [7] SC)
29	VDD2	+5 V Digital Supply Voltage [7] (SC)
30	GND2	Ground (SC)
31	LED2	LED Flashing Output [5] (MT) (SC)
32	LED1	LED Flashing Output [5] (MT) (CC)
33	GND1	Ground (CC)
34	VDD1	+5 V Digital Supply Voltage [7] (CC)
35	VDDA1	+5 V Analog Supply Voltage [7] (CC)
36	LEDC	LED Control Output [5] (CC)
37	VDDM1	+3 V...+5 V MT Supply Voltage [8] (CC)
38	VIO1	+2.5 V...+5 V I/O Supply Voltage [7] (CC)

IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes);
[1] Pin numbers marked n.c. are not connected.
[2] Pin is low active.
[3] **CC: Control Channel** Grounding all channel pins should be considered if not in use.
[4] **SC: Safety Channel** Grounding all channel pins should be considered if not in use.
[5] High-side current source output. If the battery-buffered MT function is not in use, connect LED1 to GND1, respectively LED2 to GND2.
[6] Open-drain output
[7] Supply voltage input must be blocked with a capacitor of at least 100 nF close to the chip's supply terminals.
[8] Supply voltage input must be blocked with a capacitor of at least 1 µF close to the chip's supply terminals. If the battery-buffered MT function is not in use, connect VDDM1 to VDDA1, respectively VDDM2 to VDDA2. Refer to footnote 5 for LED1, and LED2.

To better EMI immunity, unused pins should be wired externally according to the built-in pull-up/pull-down.
TP1/2 must be connected to GND1/2.
GND1 and GND2 must be connected to each other.
The thermal pad of the oQFN package (bottom side) must be connected by a single link to GND1 or GND2. A current flow across the paddle is not permissible.

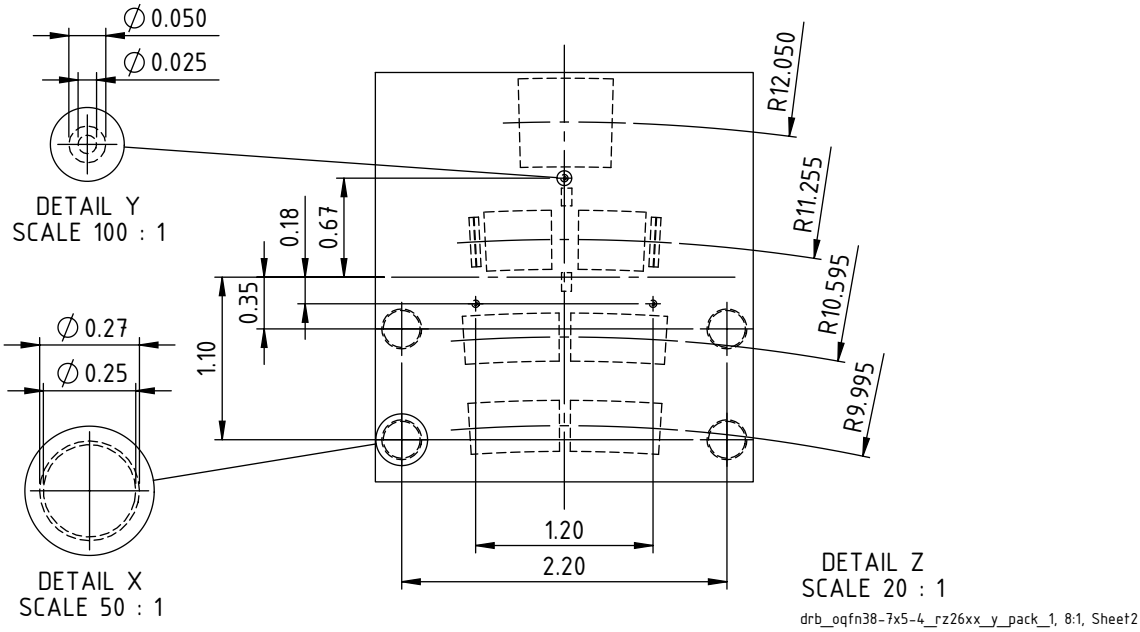
PACKAGE DIMENSIONS :iC-RZ26xx oQFN38-7x5



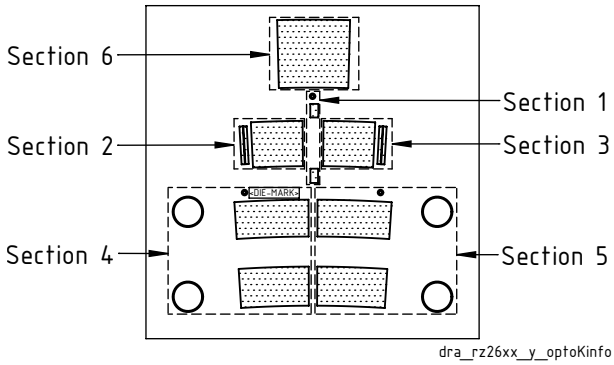
All dimensions given in mm. General tolerances of form and position according to JEDEC MO-220.
Positional tolerance of sensor pattern: ±70µm / ±0.6° (with respect to center of backside pad).
Maximum molding excess +10µm / -75µm versus surface of glass. Small pits in the mold surface, which may occasionally appear due to the manufacturing process, are cosmetic in nature and do not affect reliability.

drb_oqfn38-7x5-4_rz26xx_y_pack_1, 8:1, Sheet1

LAYOUT DETAILS: iC-RZ26xx



DETECTOR SECTIONS: iC-RZ26xx

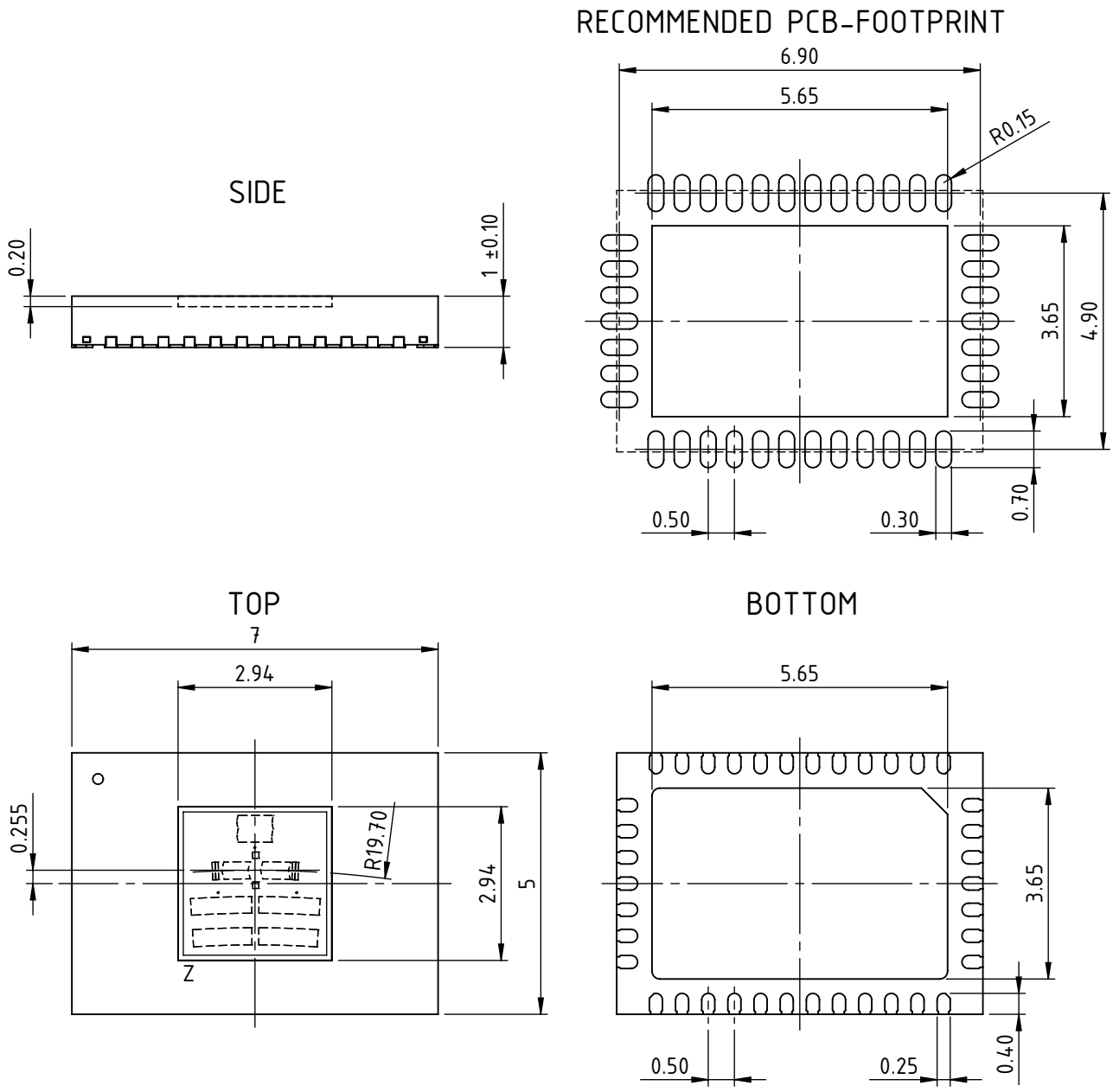


AOI CRITERIA

<Die Mark>	<Section>	<Area Class>[1]
iC RZ2624 iC RZ2648		
	1	A16
	2, 3	A25
	4, 5	A25
	6	A16

[1] Inspection class for the optical inspection of detector areas. Refer to Customer Information **V20-05** for description.

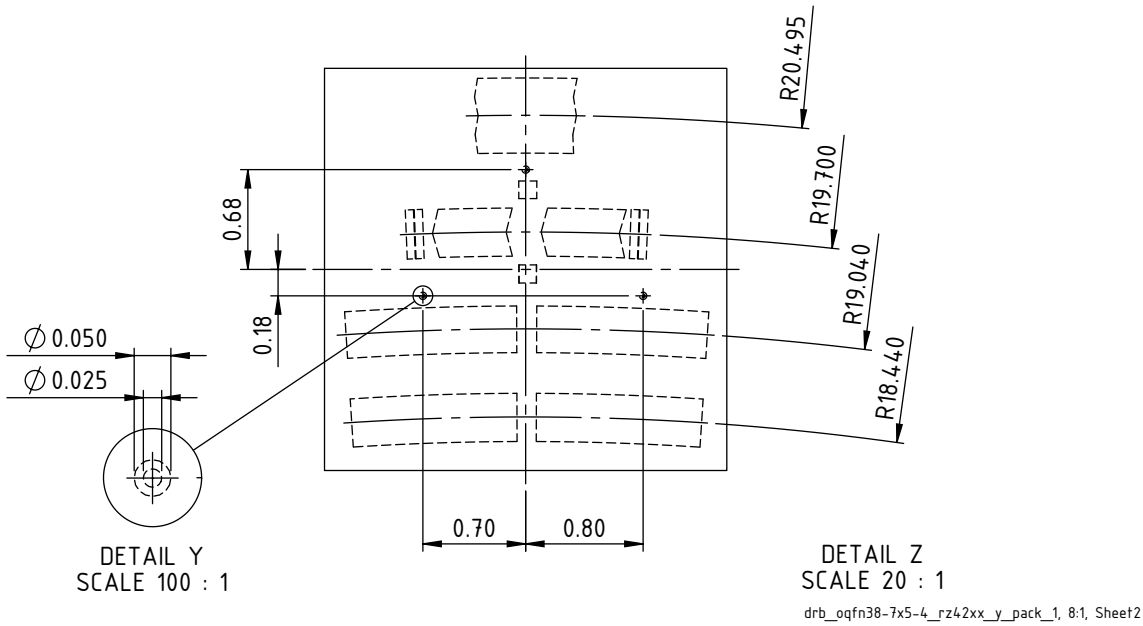
PACKAGE DIMENSIONS :iC-RZ42xx oQFN38-7x5



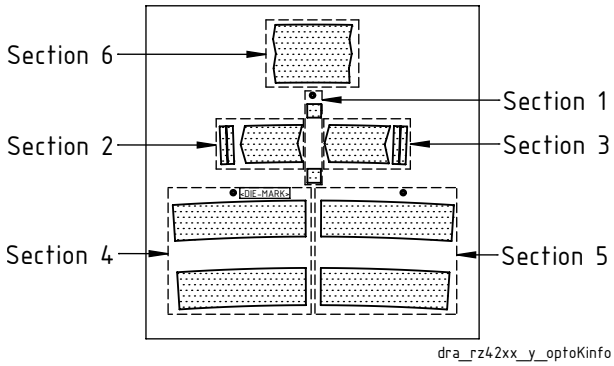
All dimensions given in mm. General tolerances of form and position according to JEDEC MO-220.
Positional tolerance of sensor pattern: ±70µm / ±0.6° (with respect to center of backside pad).
Maximum molding excess +10µm / -75µm versus surface of glass. Small pits in the mold surface, which may occasionally appear due to the manufacturing process, are cosmetic in nature and do not affect reliability.

drb_oqfn38-7x5-4_rz42xx_y_pack_1, 8:1, Sheet1

LAYOUT DETAILS: iC-RZ42xx



DETECTOR SECTIONS: iC-RZ42xx



AOI CRITERIA

<Die Mark>	<Section>	<Area Class>[1]
iC RZ4224 iC RZ4248		
	1	A16
	2, 3	A25
	4, 5	A25
	6	A16

[1] Inspection class for the optical inspection of detector areas. Refer to Customer Information **V20-05** for description.

ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	V(VDD)	Voltage at VDD1, VDD2, VDDA1, VDDA2	GND1, GND2 connected	-0.3	6	V
G002	V(VIO)	Voltage at VIO1, VIO2	GND1, GND2 connected	-0.3	6	V
G003	V(VDDM)	Voltage at VDDM1, VDDM2	GND1, GND2 connected	-0.3	6	V
G004	I(VDDx)	Current in VDD1, VDD2, VDDA1, VDDA2	GND1, GND2 connected	-20	50	mA
G005	I(VIOx)	Current in VIO1, VIO2	GND1, GND2 connected	-20	50	mA
G006	V()a	Pin Voltage, all signal analog outputs	GND1, GND2 connected	-0.3	VDDA + 0.3	V
G007	V()io	Pin Voltage, all signal digital output	GND1, GND2 connected	-0.3	VIO + 0.3	V
G008	I()	Pin Current, all signal outputs	GND1, GND2 connected	-10	10	mA
G009	Vd()	ESD Susceptibility at all Pins	HBM, 100 pF discharged through 1.5 kΩ		2	kV
G010	Tj	Junction Temperature		-40	150	°C

THERMAL DATA

Operating Conditions (x = 1,2):
VDDx = VDDAx = 4.5 . . . 5.5 V, GNDx = 0V, VDDMx = 2.9V . . . VDDAx, VIOx = 2.375V . . . VDDx

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range	oQFN38 7x5	-40		125	°C
T02	Ts	Permissible Storage Temperature Range	oQFN38 7x5	-40		125	°C
T03	Rthja	Thermal Resistance Chip to Ambient	oQFN38 7x5 soldered to PCB according to JEDEC 51		35		K/W

All voltages are referenced to ground (GND1 = GND2) unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions (x = 1, 2):
VDDx = VDDAx = VDDMx = 4.5 . . . 5.5 V, GNDx = 0 V, VIOx = 2.375 V . . . VDDx, T_j = -40 . . . 135 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device (x = 1, 2)							
001	VDDx	Permissible Supply Voltage		4.5		5.5	V
002	VDDAx	Permissible Supply Voltage		4.5		5.5	V
003	VIOx	Permissible Supply Voltage	VIOx ≤ VDDx VIOx must be up before tdr1() ends	2.375		5.5	V
004	VDDMx	Permissible Supply Voltage	if VDDx > VDDxon: VDDMx ≤ VDDx, VDDMx ≤ VDDAx	2.9		5.5	V
005	I(VDD1)	Supply Current VDD1	no load		2.5	5	mA
006	I(VDD2)	Supply Current VDD2	no load		4.0	8	mA
007	I(VDDA1)	Supply Current VDDA1	photocurrent amplifiers within op. range, no load		12.0	20	mA
008	I(VDDA2)	Supply Current VDDA2	photocurrent amplifiers within op. range, no load		6.0	10	mA
009	I(VIO1)	Supply Current VIO1	V(VIO1) = 5V, no load V(VIO1) = 3.3V, no load		0.5 0.3		mA mA
010	I(VIO2)	Supply Current VIO2	V(VIO2) = 5V, no load V(VIO2) = 3.3V, no load		1.2 0.7		mA mA
011	λar	Spectral Application Range		400		500	nm
012	S(λr)	Spectral Sensitivity	λ_{LED} = 460 nm		0.11		A/W
013	E()typ	Typical Irradiance	λ_{LED} = 460 nm , Vout() < Vout()mx		12		mW/cm²
014	C()	Required Backup Capacitor at Pin VDD1, VDD2, VDDA1, VDDA2, VIO1, VIO2	placed near by pin, recommended low ESR		100		nF
015	C(VDDMx)	Required Backup Capacitor at Pin VDDM1, VDDM2	C1 in Figure 43, MODE_MT_CC/SC = 0x0E (Battery-buffered revolution counter activated) placed near by pin, recommended low ESR		1		µF
Auxiliary Track Photodiodes and Amplifiers: PSIN, NSIN, PCOS, NCOS, VREF							
101	Aph()	Radiant Sensitive Area	DPSIN, DNSIN, DPCOS, DNCOS (sum of segments per signal) RZ2648 RZ4248 RZ2624 RZ4224		 0.058 0.064 0.042 0.053		 mm² mm² mm² mm²
102	Z()	Equivalent Transimpedance Gain	Z = Vout() / Iph(), Tj = 27 °C; RZ26xx RZ42xx		 0.971 0.780		 MΩ MΩ
103	TCz	Temperature Coefficient of Z()			-0.25		%/°C
104	fc()hi	Cut-off Frequency (-3 dB)	Signals PSIN, NSIN, PCOS, NCOS	250	550		kHz
105	ton()	Power-On Settling Time	VDD1 = 0 V → 5 V			100	µs
106	Vout()mx	Maximum Output Voltage at PSIN, NSIN, PCOS, NCOS	increasing illumination, EAMPA = 0 VDD1 = 4.5 V VDD1 = 5.5 V	 2.2 3.0			 V V
107	Vout()dc	Output Offset Voltage at PSIN, NSIN, PCOS, NCOS	amplitude controlled to 250 mV by LED control; signal contrast of 70 % (see 13 for details)		1.26		V
108	Vout()d	Dark Signal Level at VREF and PSIN, NSIN, PCOS, NCOS	no illumination	0.60	0.90	1.15	V
109	ΔZ()pn	Transimpedance Gain Matching	any output vs. any output	-0.2		0.2	%
110	ΔVout()pn	Signal Matching	any output vs. any output (without VREF) any output vs. VREF no illumination	-5 -6		5 6	mV mV
111	VNoise()	RMS Output Noise	illuminated to 500 mV signal level above dark level, 500 kHz bandwidth			1	mV
112	Iph()	Permissible Photocurrent Operating Range		0		1120	nA
113	Isc()hi	Short-Circuit Current hi from pins	load current to ground	-1000	-650	-200	µA

ELECTRICAL CHARACTERISTICS

Operating Conditions (x = 1, 2):
VDDx = VDDAx = VDDMx = 4.5 . . . 5.5 V, GNDx = 0 V, VIOx = 2.375 V . . . VDDx, T_j = -40 . . . 135 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
114	Isc(VREF)hi	Short-Circuit Current hi from pin VREF	load current to ground	-1500	-1000	-500	µA
115	Isc()lo	Short-Circuit Current lo in pins	load current to IC	200	650	1000	µA
116	Isc(VREF)lo	Short-Circuit Current lo in pin VREF	load current to IC	2000	4500	6000	µA
117	TCf	Temperature Coefficent VREF			-1.2		mV/°C
118	V(VREF)	Output Voltage	Tj = 27°C		890		mV
Power Down Reset: VDDx (x = 1, 2)							
401	VDDxon	Turn-on Threshold VDDx	increasing voltage at VDDx	3.8	4.2	4.45	V
402	VDDxoff	Turn-off Threshold VDDx (undervoltage reset)	decreasing voltage at VDDx	3.6	4.0	4.3	V
403	VDDxhys	Threshold Hysteresis VDDx	VDDxhys = VDDxon - VDDxoff	100			mV
Incremental Track (1024 CPR): Photodiodes and Amplifiers							
701	Aph()	Radiant Sensitive Area	sum of segments		0.033		mm^2
702	Z()	Equivalent Transimpedance Gain	Z = Vout() / Iph(), Tj = 27 °C		1.3		MΩ
703	TCz	Temperature Coefficient of Z()			-0.25		%/°C
704	fc()hi	Cut-off Frequency (-3 dB)		200	450		kHz
705	Vout()mx	Maximum Output Voltage	increasing illumination, EAMP24 = 0 VDDx = 4.5 V VDDx = 5.5 V	 2.2 3.0			 V V
706	Vout()d	Dark Signal Level	no illumination	0.6	0.9	1.15	V
5-bit real-time Interpolator							
801	RESsdc	Resolution Interpolator	reference one period of the 1024 track		5		bit
802	AAabs	Absolute Angular Accuracy	ideal input signals with an amplitude of 250 mV, quasi-static	-5.6		5.6	DEG
803	AArel	Relative Angle Accuracy	ideal input signals with an amplitude of 250 mV, quasi-static	-4.2		4.2	DEG
804	AAR	Repeatability Angle Accuracy	ideal input signals with an amplitude of 250 mV		± 0.5		DEG
805	Ahys	Angular Hysteresis	ideal input signals with an amplitude of 250 mV, quasi-static	± 0.5	± 2.8	± 5.6	DEG
806	Vamp()	Permissible Amplitude [1]	referring to single-ended 1024 track sin/cos signals, TEST_CC/SC = 0x03	175		500	mV
Sin/Cos AC Monitor (SC)							
A01	Vac()min	AC Level Monitoring, lower threshold	referring to single-ended sin/cos signals (all amplitudes equal), illumination decreasing AMNR = 0 AMNR = 1	 40 70	 75 125	 110 160	 mV mV
A02	Vac()max	AC Level Monitoring, upper threshold	referring to single-ended sin/cos signals (all amplitudes equal), illumination increasing AMNR = 0 AMNR = 1	 470 430	 585 525	 680 600	 mV mV
A03	Vac()hys	AC Level Monitoring, Hysteresis	referred to Vac()min, Vac()max	2	10	20	mV
Pin-Configuration Inputs CFG11, CFG10							
C01	Vt()lo	Tri-Level Threshold Voltage low		15			%VIO
C02	Vt()hi	Tri-Level Threshold Voltage high				85	%VIO
C03	Vt()mid	Tri-Level Threshold Voltage mid		35		65	%VIO
C04	V0()	Pin-Open Voltage		45	50	55	%VIO
C05	Rpd()	Internal Pull-Down Resistor	V() = VIOx	50		175	kΩ
C06	Rpu()	Internal Pull-Up Resistor	V() = GNDx	50		175	kΩ
Oscillators							
E01	fsys()	System Clock		6	10	16	MHz

[1] For iC-RZ Y and iC-RZ Y1: Please refer to the design review on p. 70.

ELECTRICAL CHARACTERISTICS

Operating Conditions (x = 1, 2):
VDDx = VDDAx = VDDMx = 4.5 . . . 5.5 V, GNDx = 0 V, VIOx = 2.375 V . . . VDDx, T_j = -40 . . . 135 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
E02	fmc()	Internal Position Clock	normal operation battery operation: VDDAx = VDDx = 0 V, VDDMx = 2.9 ... 3.6 V, error-free position detection, STEP = 0; see also Tables 71 and 72	1.2 0.018	2	4.1	MHz MHz
E03	TCfmc	Temperature Coefficient of fmc()		0.20		0.37	%/°C
E04	fmo()	SSI Clock Frequency at MOx			fsys/66		
E05	fi2c()	I2C Clock Frequency at SCL2			fsys/128		
E06	tdr1()	Wait Time after Power-on or Command REBOOT	see Figure 14		870	1500	µs
E07	tdr2()	Wait Time after Command RESET	see Figure 14		78	130	µs
E08	tcfg(SC)	SC: Configuration Time	without EEPROM EEPROM access without I^2C read error EEPROM access with I^2C read error I^2C bus busy (e.g. SDA=0)		10 4 12 2	18 7 21 3.5	ms ms ms ms
E09	tstg()	Generation Time ST Position during Start Up	no illumination error	1.4			µs
E10	tmtg()	Generation Time MT Position during Start Up	external MT without error external MT with error			2.6 170	ms ms
Sin/Cos DC Monitor (CC)							
F01	Vdc()min	DC Level Monitoring, lower threshold	Vdc() referred to VREF, EDC24 = 0 RZ26xx RZ42xx	 90 70	 160 140	 230 200	 mV mV
F02	Vdc()hys	DC Level Monitor Hysteresis		10	25	50	mV
Temperature Sensor (SC)							
H01	TEMP	Digital Temperature Representation	8-bit value; Tj = -40 °C Tj = 20 °C Tj = 100 °C		0x18 0x54 0xA4		
H02	ΔT	Measurement Resolution			1		°C/LSB
H03	T_{os}	Measurement Offset Error	Tj = -40 .. 130 °C, OTEMP = 0x00	-15		15	°C
H04	INL	Integral Linearity Error	Tj=25 °C and Offset Error corrected	-3		3	LSB
H05	DNL	Differential Linearity Error		-1		1	LSB
H06	Tr	Refresh Rate			1024/fsys		
Digital Inputs (MT, BiSS/SPI, I^2C Interfaces): MI1, MA1, MI2, SCI2, SDI2, NCS2, NL2, SCL2, SDA2, NRES2							
I01	Vt()hi	Threshold Voltage hi			66	70	%VIO
I02	Vt()lo	Threshold Voltage lo		30	33		%VIO
I03	Vt()hys	Hysteresis	Vt()hys = Vt()hi - Vt()lo	200			mV
I04	Ipd()	Pull-Down Current at MI1, MI2	V() = 1 V . . . VIOx	10	20	100	µA
I05	Ipu()	Pull-Up Current at MA1, NRES2, SCI2, SDI2, NCS2, NL2, SCL2, SDA2	V() = 0 . . . VIOx - 1 V	-100	-20	-10	µA
I06	tpw1()	Minimal Required Pulse Width at NRES2		3			µs
I07	tpw2()	Maximum Required Pulse Width at NRES2				10	µs
Test Current Inputs: TP1, TP2							
K01	Ipd()	Pull-Down Current at TP1, TP2	V() = 1 V . . . VDDAx	50	20	5	µA
LED Control (CC): LEDC							
L01	Vs()hi	Saturation Voltage hi	Vs()hi = VDD1 - V(LEDC); I() = -20 mA		0.3	0.6	V
L02	Isc()hi	Short-Circuit Current hi	V() = 0 V ENIK(1:0) = 00 ENIK(1:0) = 01 ENIK(1:0) = 10 ENIK(1:0) = 11	 -100 -0.1 -9 -18	 -50 0 -4 -8	 -25 0.1 -2 -4	 mA mA mA mA

ELECTRICAL CHARACTERISTICS

Operating Conditions (x = 1, 2):
VDDx = VDDAx = VDDMx = 4.5 ... 5.5 V, GNDx = 0 V, VIOx = 2.375 V ... VDDx, T_j = -40 ... 135 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
L03	Iop()	Permissible LED Output Current Control Range	ENIK(1:0) = 00	-25		-0.05	mA
L04	Vpk()	Regulated Mean Target Amplitude with Square Control	Vpk() = V(PSIN) - V(NSIN), Vpk() = V(PCOS) - V(NCOS) respectively; ENIK(1:0) = 00, VSET(1:0) = 11		500		mV
L05	ton	Power-On Settling Time	ENIK(1:0) = 00			800	µs
L06	Va()min	Low Amplitude Monitoring Threshold	according to L04; refers to $\sin^2+\cos^2$ vector amplitude, threshold to trigger status ELEDC		50		%
Digital Outputs (MT, BiSS/SPI, I²C Interfaces): MO1, SLO1, CFG11, MO2, SDO2, SCL2, SDA2, ADIOK1, NRES2							
O01	Vs()hi	Saturation Voltage hi	Vs()hi = VIOx - V() MO1, SLO1, MO2, SDO2, CFG11 (only if TEST_CC = 0x07) VIOx = 2.375 ... 3.0 V, I() = -1.0 mA VIOx = 3.0 ... 5.5 V, I() = -1.5 mA SCL2, SDA2 (only if TEST_SC = 0x07) VIOx = 2.375 ... 3.0 V, I() = -2.5 mA VIOx = 3.0 ... 5.5 V, I() = -3.5 mA			400	mV
O02	Isc()hi	Short-Circuit Current hi	MO1, SLO1, MO2, SDO2, CFG11 (only if TEST_CC = 0x07) SCL2, SDA2 (only if TEST_SC = 0x07)	-100 -100		-1.6 -4	mA mA
O03	Vs()lo	Saturation Voltage lo	MO1, SLO1, MO2, SDO2, ADIOK1, NRES2, CFG11 (only if TEST_CC = 0x07) VIOx = 2.375 ... 3.0 V, I() = 1.0 mA VIOx = 3.0 ... 5.5 V, I() = 1.5 mA SCL2, SDA2 VIOx = 2.375 ... 3.0 V, I() = 2.5 mA VIOx = 3.0 ... 5.5 V, I() = 4.0 mA			400	mV
O04	Isc()lo	Short-Circuit Current lo	MO1, SLO1, MO2, SDO2, ADIOK1, NRES2, CFG11 (only if TEST_CC = 0x07) SCL2, SDA2	1.6 4		100 100	mA mA
O05	t_{out}()	BiSS Adaptive Slave Timeout at SLOx	refer to timing Figure 1 t_{init} measured as first 1.5 · T(MAx) each frame	2 / fsys	t_{init} + 4 / fsys	300 / fsys	
O06	Ipu()	Pull-Up Current at ADIOK1	V() = 0 ... VDDA1 - 1 V	-20	-10	-5	µA
O07	t_{P3}()	Propagation Delay: SLO stable after MA lo → hi	refer to timing Figure 1 BiSS (CC and SC) and SSI Mode (SC)			50	ns
10-bit PRC Track: Photodiodes and Amplifiers							
R01	Aph()	Radiant Sensitive Area	Random track (single photodiode) RZ26xx RZ42xx		0.0085 0.0167		mm^2 mm^2
R02	Z()	Equivalent Transimpedance Gain			2.6		MΩ
R03	Vt(hys)	Threshold Hysteresis Referred to (I(DRPi)+I(DRNi)) / 2	I(DRPi, DRNi) = 5 .. 75 nA		6	20	%
Supply Switch and Battery Monitoring (VDDMx and LEDx with x = 1, 2)							
V01	V()max	Permissible LED Operating Voltage at LEDx	While flashing the LED			VDDMx - 200	mV
V02	Vt()hi	Threshold Voltage hi at VDDAx for Supply of the Battery-buffered Multiturn Counter	VDDAx rising, Vt()hi = VDDAx - VDDMx VDDx < VDDxon (VDDx rising) VDDMx = 2.9 ... 3.6 V	60		500	mV
V03	Vt()lo	Threshold Voltage lo at VDDAx for Supply of the Battery-buffered Multiturn Counter	VDDAx falling, Vt()lo = VDDAx - VDDMx VDDx < VDDxoff (VDDx falling) VDDMx = 2.9 ... 3.6 V	0		400	mV
V04	Vt()hys	Threshold Hysteresis	Vt()hys = Vt()hi - Vt()lo	30		300	mV
V05	VDDSon	Turn-on Threshold (power-on release) for Switched Supply Voltage (VDDMx or VDDx)	VDDAx < VDDMx increasing voltage at VDDMx	1.1	2.25	2.9	V
V06	V()led	Permissible Voltage at LEDx	VDDAx ≥ VDDMx, I(LEDx) < 10 µA	0		5.5	V

ELECTRICAL CHARACTERISTICS

Operating Conditions (x = 1, 2):
VDDx = VDDAx = VDDMx = 4.5 . . . 5.5 V, GNDx = 0 V, VIOx = 2.375 V . . . VDDx, T_j = -40 . . . 135 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V07	Ipk()	Pulse Current at LEDx for Flashing	VDDMx = 2.9 ... 3.6 V, V(LEDx) = 1.4 V .. V(LEDx)max	2		10	mA
V08	tw()	Pulse Width at LEDx for Flashing	VDDMx = 2.9 ... 3.6 V, V(LEDx) = 1.4 V .. V(LEDx)max	1		3	µs
V09	f_{Flash}()	Flash Frequency at LEDx	VDDAx = VDDx = 0 V, TSLEEP_CC/SC = 0x0A, with error-free position detection; STEP* = 3 STEP = 2 STEP = 1 STEP = 0 * see page 54	 2183 1092 448 207	 4138 2103 850 391	 6896 3448 1402 644	 Hz Hz Hz Hz
V10	TCf	Temperature Coefficient of f_{Flash}		0.2		0.37	%/°C
V11	IB(VDDMx)	Average Supply Current VDDMx During Battery Operation	VDDAx = VDDx = 0 V, TSLEEP_CC/SC = 0x0A, with error-free position detection; STEP* = 3 STEP = 2 STEP = 1 STEP = 0 * see page 54		 30 16 7 5		 µA µA µA µA
V12	IL(VDDMx)	Leakage Current at VDDMx During Normal Operation	VDDAx = VDDx, VDDAx > VDDMx + Vt()hi	-1	0	1	µA
V13	Rd	Resistor between VDDMx and GNDx for Discharging	BLEED_CC = 1, LOAD_CC = 0 resp. BLEED_SC = 1, LOAD_SC = 0	35	50	80	kΩ
V14	Rc	Resistor between VDDMx and VDDAx for Charging	BLEED_CC = 0, LOAD_CC = 1 resp. BLEED_SC = 0, LOAD_SC = 1	35	50	80	kΩ
Alignment Photodiodes and Amplifiers (SC): DJH, DJL							
W01	Aph()	Radiant Sensitive Area	RZ26xx RZ42xx		0.0085 0.015		mm^2 mm^2
W02	Z()	Equivalent Transimpedance Gain	Z = Vout() / Iph(), Tj = 27 °C		8		MΩ
W03	TCz	Temperature Coefficient of Z			-0.25		%/°C
W04	fc()hi	Cut-off Frequency (-3 dB)			30		kHz
W05	Vout()d	Dark Signal Level	no illumination, TEST_SC = 0x19	0.6	0.9	1.15	V
W06	ΔVout()pn	Signal Matching	no illumination, Tj < 50 °C	-20	0	20	mV
W07	Iph()	Permissible Photocurrent Operating Range		0		250	nA
W08	Isc()hi	Short-Circuit Current hi	MO2, SDO2; TEST_SC = 0x19, load current to ground		-650		µA
W09	Isc()lo	Short-Circuit Current lo	MO2, SDO2; TEST_SC = 0x19, load current to IC		450		µA

OPERATING REQUIREMENTS: BiSS, SSI Interface

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
BiSS C Protocol						
I001	t_C	Permissible Clock Period		100	2x t_{out}	ns
I002	t_{L1}	Clock Signal Hi-Level Duration		50	t_{out}	ns
I003	t_{L2}	Clock Signal Lo-Level Duration		50	t_{out}	ns
I004	t_{P3}	Propagation Delay		see Elec. Char. O07		
I005	t_{out}	Adaptive Slave Timeout		see Elec. Char. O05		
I006	t_{busy}	Minimum Data Output Delay	visible for t_C > 4/fsys	2 t_C		
I007	t_{busy}	Maximum Data Output Delay	visible for t_C < 4/fsys	1.5 t_C + 4/fsys	2.5 t_C + 4/fsys	
I008	t_{S1}	Setup Time: SDI2 stable before SCI2 hi → lo	see Figure 2	25		ns
I009	t_{H1}	Hold Time: SDI2 stable after SCI2 hi → lo	see Figure 2	10		ns
I010	t_{IS}	Wait Time: Switching from BiSS to SPI and vice versa	IF_MODE = 0x0 (SC), see Figure 3	40		µs
I011	t_{frame}	Permissible Frame Repetition		*)	indefinite	
SSI Protocol (SC only, IF_MODE = 0x02, 0x03)						
I012	t_C	Permissible Clock Period	after t_{RQ}	250	2x t_{out}	ns
I013	t_{L1}	Clock Signal Hi-Level Duration		50	t_{out}	ns
I014	t_{L2}	Clock Signal Lo-Level Duration	note t_{RQ} as exception	50	t_{out}	ns
I015	t_{P3}	Propagation Delay		see Elec. Char. O07		
I016	t_{out}	Slave Timeout		50	t_{out}	ns
I017	t_{RQ}	Processing Time		4/fsys		
I018	t_{frame}	Permissible Frame Repetition		*)	indefinite	

Note: *) Allow t_{out} to elapse.

Control Channel

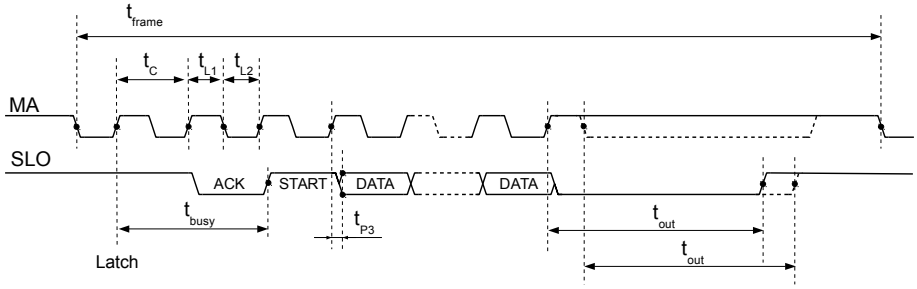


Figure 1: BiSS Protocol Timing (CC). Signal MA refers to input MA1, signal SLO to output SLO1.

Safety Channel

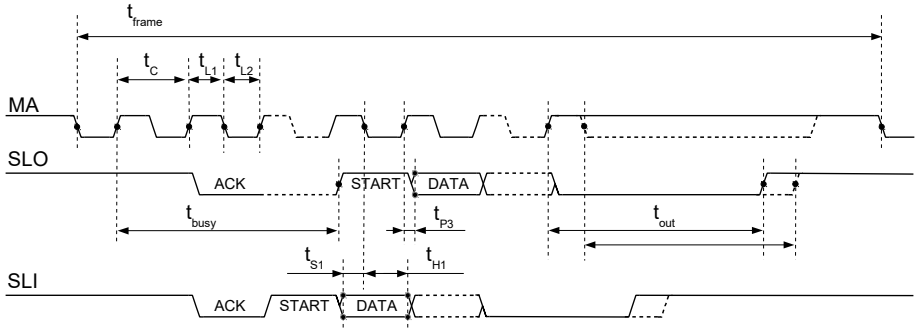


Figure 2: BiSS Protocol Timing (SC: IF_MODE = 0x0, 0x1). Signal MA refers to input SCI2, signal SLO to output SDO2, signal SLI to input SDI2.

Safety Channel

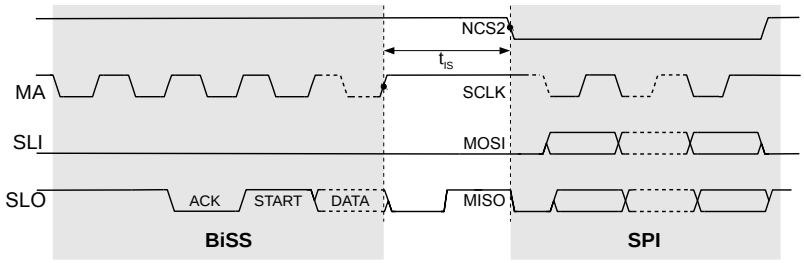


Figure 3: Switching from BiSS to SPI (SC: IF_MODE = 0x0).
Signals MA / SCLK refer to input SCI2, signals SLO / MISO to output SDO2, signals SLI / MOSI to input SDI2.

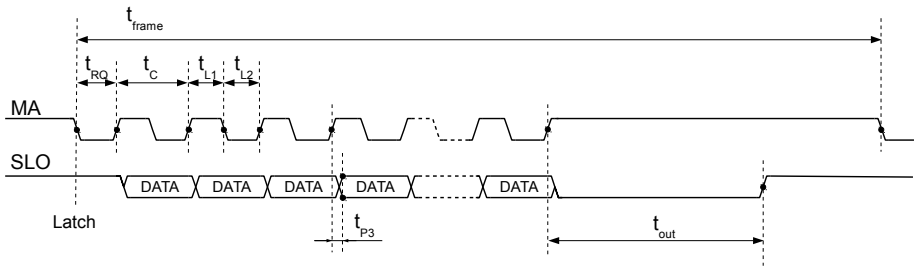


Figure 4: SSI Protocol Timing (SC: IF_MODE = 0x2, 0x3).
Signal MA refers to input SCI2, signal SLO to output SDO2.

OPERATING REQUIREMENTS: SPI Interface

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
I101	t_{C1}	Permissible Clock Period at SCLK		100		ns
I102	t_{L1}	Clock Signal lo Level Duration		50		ns
I103	t_{L2}	Clock Signal hi Level Duration		50		ns
I104	t_{W1}	Wait Time: Between NCS2 lo → hi and hi → lo		800		ns
I105	t_{S1}	Setup Time: NCS2 stable before SCLK lo → hi		100		ns
I106	t_{P1}	Propagation Delay: MISO stable after NCS2 hi → lo	CL = 10 pF		50	ns
I107	t_{P2}	Propagation Delay: MISO tristate after NCS2 lo → hi	CL = 10 pF		50	ns
I108	t_{H1}	Hold Time: NCS2 lo after SCLK lo → hi	valid for SPI mode 3	50		ns
I109	t_{H3}	Hold Time: NCS2 lo after SCLK hi → lo	valid for SPI mode 0	50		ns
I110	t_{S2}	Setup Time: MOSI stable before SCLK lo → hi		50		ns
I111	t_{H2}	Hold Time: MOSI stable after SCLK lo → hi		50		ns
I112	t_{P3}	Propagation Delay: MISO stable after MOSI change	MOSI forwarded to MISO, CL = 10 pF		50	ns
I113	t_{P4}	Propagation Delay: MISO stable after SCLK hi → lo	data output to MISO, CL = 10 pF		50	ns
I114	t_{W2}	Wait Time: SCLK stable after NCS2 lo → hi	IF_MODE = 0x4, 0x5	800		ns
I115	t_{IS}	Wait Time: Switching from SPI to BiSS and vice versa	IF_MODE = 0x0, see Figure 6	40		µs

Safety Channel

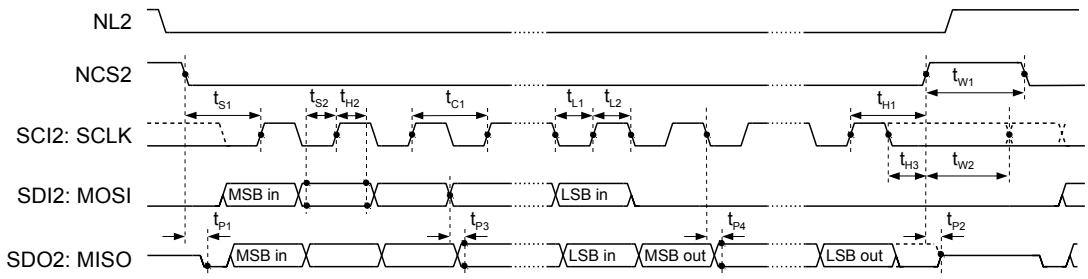


Figure 5: SPI Timing (IF_MODE = 0x0, 0x4, 0x5)

Safety Channel

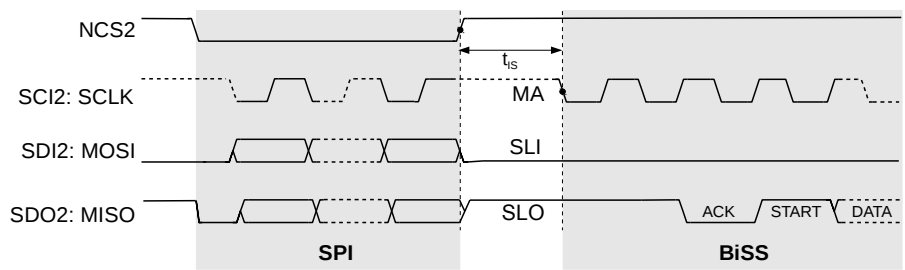


Figure 6: Switching from SPI to BiSS (IF_MODE = 0x0)

OPERATING REQUIREMENTS: MT Interface

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
I201	t_C	Clock Period		1/fmo[1)]		
I202	t_{L1}, t_{L2}	Clock Signal hi/lo Level Duration		50		%t_C
I203	t_S	Setup Time: Data stable before clock edge hi → lo		100		ns
I204	t_H	Hold Time: Data stable after clock edge hi → lo		100		ns
I205	t_{out}	Timeout		5.75		µs
I206	t_{frame}	Clock Frame Repetition		0.94	2.5	ms

Note: [1)] see Elec. Char. E04

Control Channel

Safety Channel

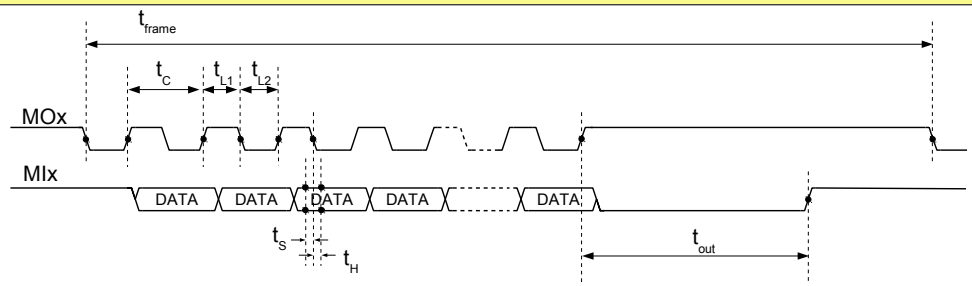


Figure 7: Multiturn SSI Interface Timing (x = 1, 2; MODE_MT = 0x0..0x5, 0x8..0xD)

OPERATING REQUIREMENTS: I²C Interface

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
I301	t_C	Clock Period		1/fi2c[2)]		

Note: [2)] see Elec. Char. E05

Safety Channel

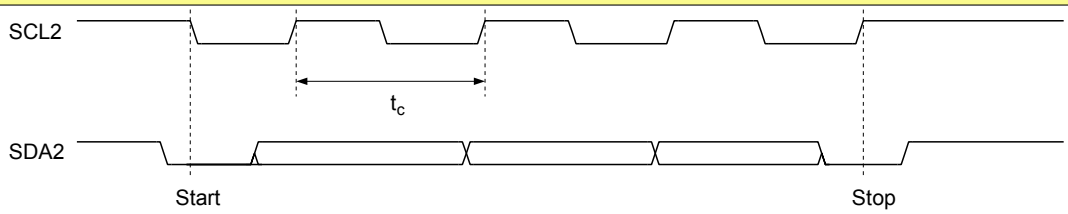


Figure 8: I²C Timing

SYSTEM OVERVIEW

Overview

The iC-RZ is divided into two sections called the Control Channel (CC) and the Safety Channel (SC): each section decodes the absolute singleturn position from the code disc (CPW and SPW).
The code disc contains 3 different tracks: 1 incremental track of 1024 CPR, 1 absolute Pseudo-random Code track (10-bit PRC) and 1 auxiliary track (AT), where the cycles per revolution depends on the device version. The two channels are on the same substrate, but are separated by a trench. Each channel features its own photodiodes for scanning the tracks of the code disc. Due to this, the absolute singleturn position is generated from two different code sections of the code disc. The following figure shows the general data flow.

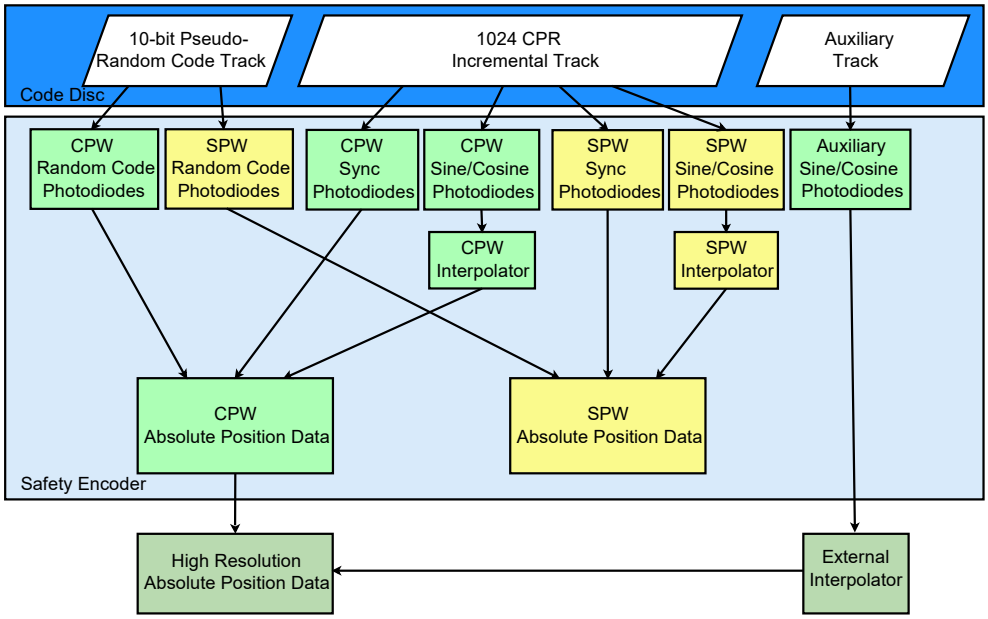


Figure 9: Principle data flow

According to the chip's sine/cosine photosensor layout, a phase-shift exists between the 3 different sine/cosine tracks as shown in the following figure (exemplary with 2048 CPR for the auxiliary sine/cosine track):

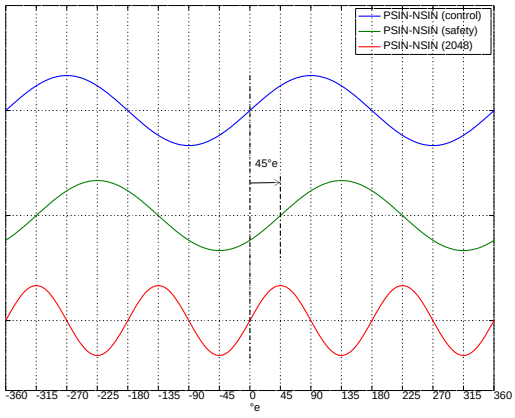


Figure 10: Sine/Cosine phase-shift, °e = with reference to one electrical period

As for the sine/cosine photosensors, there is also a permanent difference between the two 10-bit Pseudo-random code values. The PRC sensor sections are arranged to give a constant difference of 11.125 LSB, with respect to a 10-bit resolution.

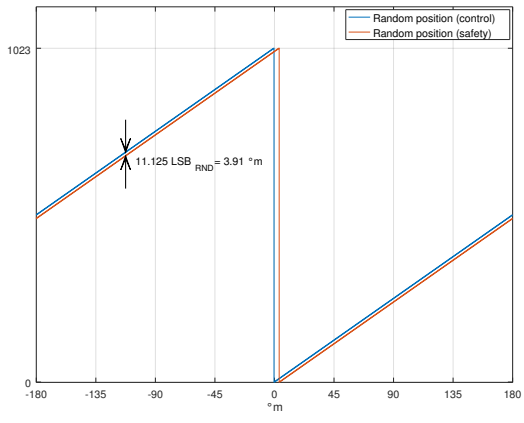


Figure 11: PRC position difference, °m = with reference to one mechanical revolution

Because of the two generated positions the iC-RZ is suitable for use in safety-related applications. Therefor the system requirements and restrictions (particularly the use of the sin/cos signals) described in the appropriate Safety Implementation Manual must be considered.

For safety-related applications the appropriate Safety Implementation Manual has to be considered.

Control Channel (CC)
The Control Channel consists of the following blocks:

- Photodiodes with amplifiers for auxiliary sin/cos signals
- Photodiodes with amplifiers for 1024 CPR sin/cos signals
- Photodiodes with amplifiers and comparators for 10-bit PRC scanning
- 5-bit real-time interpolator for the sin/cos signals of 1024 CPR
- Multiturn section
- Diagnostics (e.g. sin/cos DC monitor)
- Serial BiSS interface for position data output and configuration
- Pin configuration inputs CFG10, CGF11
- LED control output (based on the auxiliary sin/cos signals)
- Index pulse generation

The generated position word of the Control Channel is called Control Position Word (CPW).

Safety Channel (SC)
The Safety Channel consists of the following blocks:

- Photodiodes with amplifiers for 1024 CPR sin/cos signals
- Photodiodes with amplifiers and comparators for 10-bit PRC scanning
- 5-bit real-time interpolator for the sin/cos signals of 1024 CPR
- Multiturn section
- Serial interface (BiSS/SSI, SPI) for position data output and configuration
- Serial I^2C interface for configuration
- Diagnostics (e.g. sin/cos AC monitor)
- Temperature sensor

The generated position word of the Safety Channel is called Safety Position Word (SPW).

I/O PIN OVERVIEW

Control Channel
The pins summarized in Table 8 are powered by VIO1 and have CMOS thresholds.

Control Channel			
Pins powered by VIO1			
Pin No.	Name	Pin No.	Name
7	ADIOK1	10	CFG11
8	MO1[1]	11	CFG10
9	MI1[1]	12	MA1
		13	SLO1
	[1] Supplied by VDDM1 in battery-buffered mode.		

Table 8: Supply of digital pins (CC)

Safety Channel
The pins summarized in Table 9 are powered by VIO2 and have CMOS thresholds.

Safety Channel			
Pins powered by VIO2			
Pin No.	Name	Pin No.	Name
14	SCL2	20	NCS2
15	SDA2	21	NL2
16	SDO2	22	MI2[1]
17	SCI2	23	MO2[1]
18	SDI2	24	NRES2
	[1] Supplied by VDDM2 in battery-buffered mode.		

Table 9: Supply of digital pins (SC)

CONFIGURATION PARAMETERS

REGISTER MAP (CC)

OVERVIEW CONTROL CHANNEL

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Configuration								
0x00 ... 0x0F	not available							
Multiturn Configuration								
0x10	SBL_MT_CC(1:0)		EBL_MT_CC(1:0)		MODE_MT_CC(3:0)			
0x11	TSLEEP_CC(7:0)							
Interface Configuration								
0x12	0	0	DL_MT_CC(1:0)		DL_ST_CC(3:0)			
0x13	0	0	0	0	0	0	0	NWRN_ECP
0x14 ... 0x18	not available							
Status Masking								
0x19	EMASK_CC(7:0)							
0x1A	WMASK_CC(7:0)							
0x1B ... 0x2F	not available							
Test								
0x30	0	BLEED_CC	LOAD_CC	TEST_CC(4:0)				
0x31	VSET(1:0)		ENIK(1:0)		SELRND_CC(3:0)			
0x32 ... 0x3F	not available							
BiSS Standard Register								
0x40 0x41	not available							
0x42 0x43	Profile ID							
0x44 ... 0x47	0x00							
0x48 ... 0x6F	not available							
Status Messages*								
0x70	$EB3_L$	$EB2_L$	$EB1_L$	$EB0_L$	$ESSI_L$	ERC_L	EST_L	$EINT_L$
0x71	$EDC24_L$	$ELEDC_L$	$EAMPA_L$	$EAMP24_L$	$EAMPR_L$	0	$EPDN_L$	ERL_L
0x72	$EMTSYNC_L$	$ESTSYNC_L$	IFFOR	WFOR	EFOR	ENRPCFG	ECP_L	TEST
0x73 ... 0x75	not available							

OVERVIEW CONTROL CHANNEL								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMD_STAT_CC Register (Revision)								
0x76	CMD_STAT_CC(7:0) (revision only)							
Command Register: CMD_CC(7:0)								
0x77	CMD_CC(7:0)							
BiSS Identifier (only readable)								
0x78	Device ID - 0x52 ('R')							
0x79	Device ID - 0x5A ('Z')							
0x7A	Revision - CHIP_REVISION(7:0)							
0x7B	Device ID - (b"00" & DL_MT_CC & DL_ST_CC)							
0x7C	Device ID - 0x00							
0x7D	Device ID - 0x00							
0x7E	Manufacturer ID - 0x69 ('i')							
0x7F	Manufacturer ID - 0x43 ('C')							

* $_L$ = latched status information, command **SCLEAR** required for reset

Table 10: Register map of Control Channel

REGISTER MAP (SC)

OVERVIEW SAFETY CHANNEL								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Configuration								
0x00 ... 0x0F	not available							
Multiturn Configuration								
0x10	SBL_MT_SC(1:0)		EBL_MT_SC(1:0)		MODE_MT_SC(3:0)			
0x11	TSLEEP_SC(7:0)							
Interface Configuration								
0x12	0	0	DL_MT_SC(1:0)		0	DL_ST_SC(2:0)		
0x13	IF_MODE(2:0)			0	0	0	0	ENESTL
0x14	0	0	0	0	0	0	0	0
0x15	0	0	CRC_ID(5:0)					
Diagnostic/Temperature Sensor Configuration								
0x16	AMNR	TWARNSW	OTEMP(5:0)					
0x17	TWARN(7:0)							
0x18	TERR(7:0)							
Status Masking								
0x19	EMASK_SC(7:0)							
0x1A	WMASK_SC(7:0)							
0x1B ... 0x1D	0x00							
Protect Configuration								
0x1E	PROT_CFG(7:0)							
0x1F	CRC_CFG(7:0)							
Output Format Configuration								
0x20	OFF_MT(23:16)							
0x21	OFF_MT(15:8)							
0x22	OFF_MT(7:0)							
0x23	OFF_ST(14:7)							
0x24	OFF_ST(6:0)							DIR
0x25 ... 0x2D	0x00							
0x2E	PROT_OFF(7:0)							
0x2F	CRC_OFF(7:0)							
Test Configuration								
0x30	0	BLEED_SC	LOAD_SC	TEST_SC(4:0)				
0x31	0	0	0	0	SELRND_SC(3:0)			
0x32 ... 0x3F	not available							

OVERVIEW SAFETY CHANNEL								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BiSS Standard Register								
0x40	I2CDEV(2:0)			BSEL(4:0)				
0x41 ... 0x6F	Defined by BiSS							
Status Messages*								
0x70	$EB3_L$	$EB2_L$	$EB1_L$	$EB0_L$	$ESSI_L$	ERC_L	EST_L	$EINT_L$
0x71	$EMIN_L$	$EMAX_L$	0	$EAMP24_L$	$EAMPR_L$	0	$EPDN_L$	ERL_L
0x72	NOEPR	ENRPCFG	ENRPOFF	$ETEMP_L$	$WTEMP_L$	ETSL	ECRC	TEST
0x73	TEMP(7:0)							
0x74	$EMTSYNC_L$	$ESTSYNC_L$	IFFOR	WFOR	EFOR	$EI2C_L$	ECRC_OFF	ECRC_CFG
0x75	0	0	0	0	0	0	0	0
CMD_STAT_SC Register (Revision)								
0x76	CMD_STAT_SC(7:0) (revision only)							
Command Register								
0x77	CMD_SC(7:0)							
BiSS Identifier								
0x78 ... 0x7D	BiSS Device Identifier							
0x7E ... 0x7F	BiSS Device Manufacturer Identifier							

* $_L$ = latched status information, command **SCLEAR** required for reset

Table 11: Register map of Safety Channel

PHOTODIODES

Overview
Figure 12 shows the different photodiode tracks of iC-RZ. Both channels have incremental photodiodes for internal interpolation ② and random track photodiodes for the absolute position ③.

Additionally, the Control Channel has auxiliary track photodiodes with differential analog outputs ① which are also used by the LED control unit.

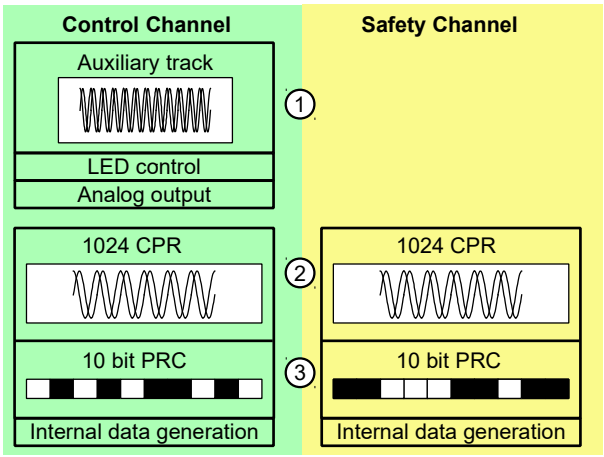


Figure 12: Photodiode tracks of iC-RZ

Auxiliary track photodiodes with differential analog outputs (CC)
The auxiliary track photodiodes generate the differential sine and cosine signals, which are output to PSIN, NSIN, and PCOS, NCOS, respectively. The number of cycles per revolution depends on the chip version and the corresponding code disc. These sin/cos signals allow to higher the resolution when connecting an external interpolation IC (e.g. iC-MR3).

The internal LED control circuit uses these sin/cos signals to adjust the LED current, to obtain an output amplitude of about 250 mV at PSIN, NSIN, and PCOS, NCOS (see Chapter LED CONTROL (CC)).

Using an external LED control is possible too; pin LEDC should then be left open. In this case the external LED control needs to evaluate the PSIN, NSIN, and PCOS, NCOS output signals and adjust the LED current to obtain amplitudes of about 250 mV again.

For accuracy of external interpolation, the system should be installed in a way that an optical contrast of at least 50 % is reached. This contrast ratio is visible as the AC to DC ratio of the electrical sin/cos output signals (see formula in Figure 13). Furthermore, a reasonable optical contrast also avoids signal clipping due to amplifiers operating in saturation.

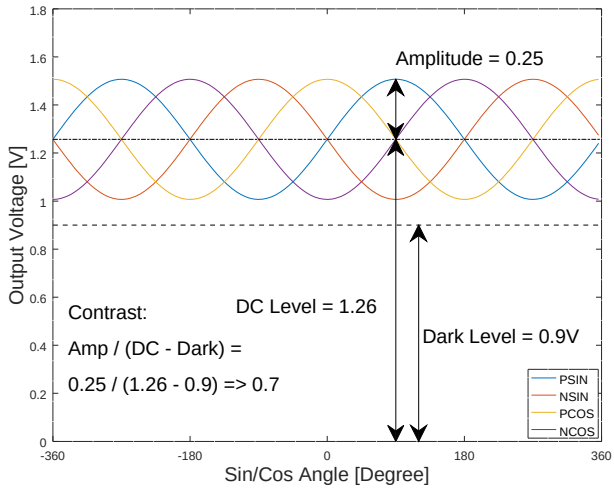


Figure 13: Signal level for contrast 70%

The output's DC voltage level rises with the intensity of illumination; the maximum possible output voltage (see Elec. Char. 106) can be reached at excessive illumination, and when the LED control tries to balance an optical contrast which is too poor. The status bit EAMPA signals those excessive conditions (see Table 81, page 60).
For reliable operation, however, a maximum differential signal is still output at PSIN against NSIN and at PCOS against NCOS to prevent an external LED controller from further increasing the LED current.

If single-ended sin/cos signals are required (with or without level shifting to VDD/2), these signals must be generated from P- versus N-outputs with VREF as ground reference.

Incremental track photodiodes for the internal 5-bit interpolator
The incremental track photodiodes generate the sine/-cosine signals with 1024 cycles per revolution for the internal 5-bit real-time interpolator. These signals are only used for internal interpolation and can not be seen on pins in the normal function mode. The photodiode area and the amplifier gain of the 1024 CPR are designed to achieve the same amplitude (250 mV) as the auxiliary track with uniform illumination.

The layout of the photodiodes for the Control and the Safety Channel is such that the resulting signals of the channels have a 45 ° phase shift relative to one another (see Figure 10, page 20).

Control Channel status bits:
EAMP24 signals an incorrect amplifier operating point.
EDC24 signals that the minimum working light level is not reached (see Table 81, page 60).

Safety Channel status bits:
EAMP24 signals an incorrect amplifier operating point.
A *sin*^{2} + *cos*^{2} *monitor* signals with EMIN and EMAX where the amplitude lies in relation to the limits (for status bits see Table 90, page 63, for limits see Elec. Char. A01, A02).

PRC track photodiodes
The Pseudo-random Code (PRC) on the code disc is scanned by differential, leading/trailing photodiodes to get a secured position value. A selection signal for the leading or trailing photodiodes is generated by separate photodiodes scanning the 1024 PPR track (② in Figure 12).

A differential evaluation of the random photodiodes results in 10 digital comparator signals for each channel. These comparator signals represent the scanned random code with a bit length of 10 bits. The code offset between CPW and SPW equals 11.125 LSB.

These photodiodes can also be used for multiturn applications. For further information about the supervision and processing of these signals see the multiturn description.

LED CONTROL (CC)

An external LED is powered by pin LEDC, and optionally by the pins LED1 (CC) **or** LED2 (SC) when a battery-buffered multiturn function is required.

In battery-buffered mode the pins LED1 (CC) or LED2 (SC) are used to flash the external LED to get the singleturn position and to update the internal multiturn counter (see description of **Battery-buffered revolution Counter** on page 54).
For this purpose the pins LEDC and LED1, **or** LEDC and LED2, must be connected to the LED.

If using an external LED control and LEDC is not connected, pin LED1 **or** LED2 can be connected additionally for battery-buffered revolution counting.

In fully supplied mode the internal LED control can be used for light regulation, based on the sine/cosine signals of the auxiliary incremental track. For this purpose, iC-RZ has a controlled high-side current source at pin LEDC to power the external LED.

By default the Square Control Mode is active which keeps the sum of the sine/cosine amplitude squares at a constant value (sin^2+ cos^2 = const.). For alignment or debugging, the mode of the regulation can be changed with parameter ENIK from Square Control Mode to a constant current mode.

Control Channel	
ENIK(1:0)	Addr. 0x31; bit 5:4
Code	Current
00	Square Control Mode (default)
01	0 mA constant current
10	4 mA constant current
11	8 mA constant current

Table 12: LED control mode

The target amplitude for the Square Control Mode is set with parameter VSET and must be set to default value of 250 mV (see Table 13).

Control Channel	
VSET(1:0)	Addr. 0x31; bit 7:6
Value	Target Amplitude of Auxiliary Sin/Cos (AT)
00 01 10	not allowed
11	250 mV (default)

Table 13: LED control amplitude

The status bit ELEDC (see Table 81, page 60) is set when the actual amplitude (sin^2 + cos^2) is less than half of the target amplitude (<50% of 250mV).

STARTUP PROCESS

The Control Channel (CC) and the Safety Channel (SC) are starting up according to the following sequence.

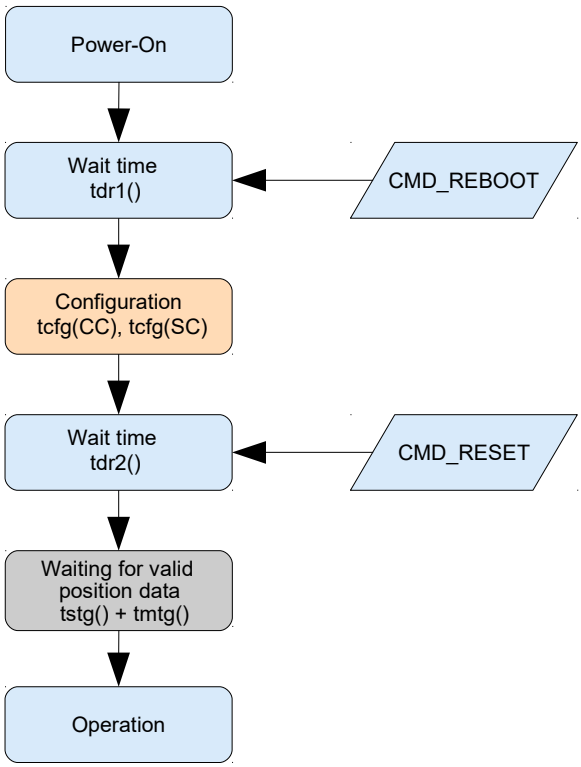


Figure 14: Overview of startup process

A reboot is performed on power-on, or can be triggered by sending the **REBOOT** command, or by applying a low level to pin NRES2 (Safety Channel only)
A reset using the existing RAM configuration can be triggered by sending the **RESET** command.

The actual startup state can be tracked as follows:

Control Channel		
State	Pin ADIOK	BiSS
Power-on	0	Position data*, nE, nW are set to 0
Wait time tdr1()	0	Position data*, nE, nW are set to 0
Configuration	0	Position data*, nE, nW are set to 0
Waiting for valid position data	0	Position data, nE, nW are set to 0
Operation	Z	Position data available
Notes	* Data length is 9-bit ST by default until end of configuration.	

Table 14: Startup state detection CC

Safety Channel		
State	SPI	BiSS
Power-on	disabled SDO2=Z	disabled SDO2=Z
Wait time tdr1()	disabled SDO2=Z	disabled SDO2=Z
Configuration	disabled SDO2=Z	disabled SDO2=Z
Waiting for valid position data	Position data, nE, nW, LC are set to 0	Position data, nE, nW, LC are set to 0
Operation	Position data available, LC≠0	Position data available, LC≠0

Table 15: Startup state detection SC

VIO1 and VIO2 must both be up ahead of the power-up wait time tdr1() has elapsed (see Elec. Char. E06).

The state 'Operation' should have been reached ahead of position data requests via BiSS/SSI.
With an error-free startup this state is reached after tdr1() + tcfg() + tdr2() + tstg() + tmtg(). See Elec. Char. E06, E08, E07, E09, E10. Time tcfg(CC) is negligible due to pin configuration.

Configuration of Control Channel
After power-on reset, the initial configuration for the Control Channel is provided by pin configuration, from CFG11 and CFG10, which are 3-level sensitive. In any case, the Control Channel uses BiSS for register and sensor data communication.

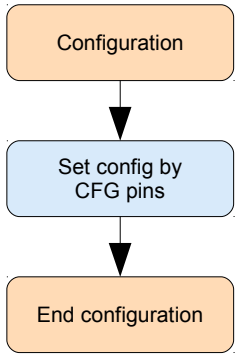


Figure 15: Startup configuration CC

The pin states of CFG11 and CFG10 are sampled at startup – after the wait time tdr1() (see Elec. Char. E06) – and initialize the configuration parameters of the Control Channel according to Table 17.

This includes the MT operating mode (MODE_MT_CC), the count of synchronization bits (SBL_MT_CC) and error bits (EBL_MT_CC), as well as the output length

of singleturn and multiturn data (DL_ST_CC, and DL_MT_CC). Furthermore, the status messaging (EMT) is assigned.

Control Channel		
Addr.	Default Value	Description
0x11	0xFF*)	TSLEEP_CC
0x19	0x77	EMASK_CC
0x1A	0x7F	WMASK_CC
0x31	0xC0	LED Square Control Mode 250mV
Note	*) If no battery is connected to VDDM1 and until first configuration of the battery-buffered TSLEEP_CC value. All other registers are preset with 0x00.	

Table 16: Default configuration after power-on

The configuration registers are write-protected afterwards. However, the configuration of the Control Channel can still be changed, but only if the write protection has been deactivated before.

The pin states are monitored in operation. If any logic level differs from the original state at startup, status bit ECP is set. The configuration registers remain protected and are not updated.

Control Channel							
CFG11/10[1]	**MODE_MT_CC**	**SBL_MT_CC**	**EBL_MT_CC**	**DL_ST_CC**	**DL_MT_CC**	**Index Pulse**	**EMT Status**
0 0	0x6 (No multiturn)	00 (1 bit)	00 (no err)	0111 (16 bit)	00 (no MT)	-	0
0 1	0x0 (Synced Mode 12 bit)	10 (3 bit)	01 (1 err)	1111 (24 bit)	01 (12 bit)	-	EB3..0 or ESSI or ERC_C
0 x	0xA (iC-LV Mode 12 bit)	10 (1 bit)	01 (1 err)	1111 (24 bit)	01 (12 bit)	-	EB3..0 or ESSI or ERC_C
1 0	0x3 (Synced Mode 16 bit)	10 (3 bit)	01 (1 err)	1111 (24 bit)	10 (16 bit)	-	EB3..0 or ESSI or ERC_C
1 1	0xE (Internal counter battery-buffered)	00 (1 bit)	00 (no err)	1111 (24 bit)	11 (24 bit)	✓	$EPDN_L$ or ERL_L or ERC_C
1 x	0xD (iC-LV Mode 16 bit)	10 (1 bit)	01 (1 err)	1111 (24 bit)	10 (16 bit)	-	EB3..0 or ESSI or ERC_C
x 0	0x1 (iC-MV Mode 12 bit)	10 (3 bit)	01 (1 err)	1111 (24 bit)	01 (12 bit)	-	EB3..0 or ESSI or ERC_C
x 1	0x4 (iC-MV Mode 16 bit)	10 (3 bit)	01 (1 err)	1111 (24 bit)	10 (16 bit)	-	EB3..0 or ESSI or ERC_C
x x	0xF (Internal counter)	00 (1 bit)	00 (no err)	1111 (24 bit)	11 (24 bit)	✓	ERC_C
Notes	[1] x = pin open or set to 1/2 of VIO1, or VIO2. Multiturn parameters: MODE_MT_CC, EBL_MT_CC and SBL_MT_CC, see Table 60, page 51 ff. Output data length: DL_MT_CC, DL_ST_CC, see Table 27, page 37 f. Index pulse output see page 57 EMT status information see Table 83, page 60						

Table 17: Pin configuration of Control Channel.

Configuration of Safety Channel

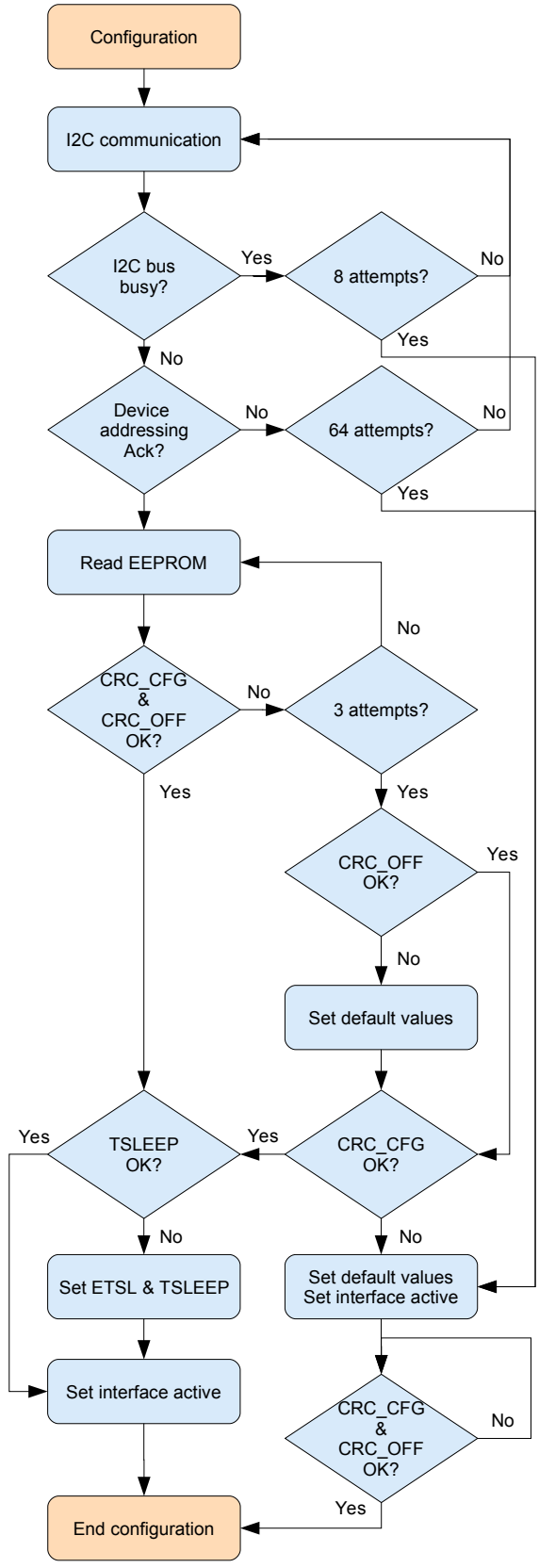


Figure 16: Startup configuration SC

After power-on reset and expiration of the wait time tdr1() (see Elec. Char. E06) the configuration of the Safety Channel is read from an external EEPROM via the I^2C interface.

The timing for the configuration phase depends on the I^2C status, see elec. char. E08 for more information.

If no EEPROM is connected or if the CRC check fails in any of the two configuration areas, the internal registers of the failing CRC check section are preset with the values given in Table 18.
If CRC_CFG is correct, the battery-buffered TSLEEP_SC value is compared with the TSLEEP_SC value read from the EEPROM. In case of a mismatch between the two (e.g. after battery replacement), the battery-buffered TSLEEP_SC is updated with the EEPROM value.

If no EEPROM is connected or if the CRC_CFG crc check fails, the absolute position data is not available. If position data is requested, a zero value is returned. In addition, within the BiSS SCD, SPI position read command response, or extended SSI frame, the error and warning bits are active (nE = nW = 0).

If error and warning bits are both active, iC-RZ must be configured including a valid CRC_CFG and CRC_OFF by using the serial interface. After the configuration, CMD_SC = **RESET** must be executed to start the position data generation.

The Safety Channel can use BiSS, SSI, Extended SSI or SPI for sensor data communication and BiSS or SPI for register communication.

Safety Channel		
Addr.	Default Value	Description
0x10	0x06	No multiturn
0x11	0xFF*)	TSLEEP_SC
0x17	0xBD	TWARN: 125 °C
0x18	0xCC	TERR: 140 °C
0x19	0xDF	EMASK_SC
0x1A	0xDF	WMASK_SC
Note	*) If no battery is connected to VDDM2 and until first configuration of the battery-buffered TSLEEP_SC value. All other registers are preset with 0x00.	

Table 18: Default configuration with wrong CRC_CFG or w/o EEPROM

Position data initialization

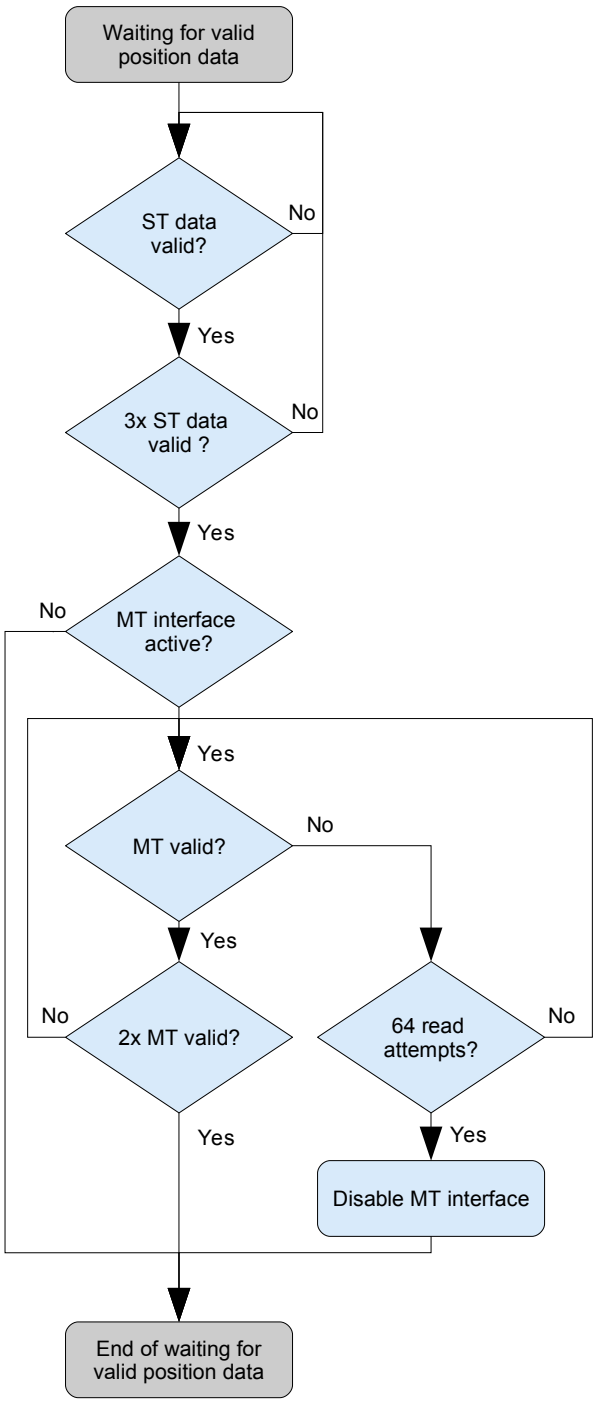


Figure 17: Position data initialization

The startup sequence for getting valid position data is the same for the Control Channel and Safety Channel. The position data generation is started after wait time tdr2 has elapsed (see Elec. Char. E07).

The timing depends on the configuration, status of the illumination and the status of the external MT sensor. For more information see Elec. Char. E09 and E10.

A valid ST position (only random track) is awaited, and after getting 3 valid ST positions, the MT interface is activated if enabled.

If activated, the MT interface reads the connected MT slaves, and after receiving 2 correct data values the channel switches to operation mode. After a maximum of 64 failed MT read attempts, the status bit ESSI is set and the state switches to operating mode, but with deactivated MT interface. Thereafter, no further clock pulses are output at MO1/MO2.

I2C INTERFACE (SC)

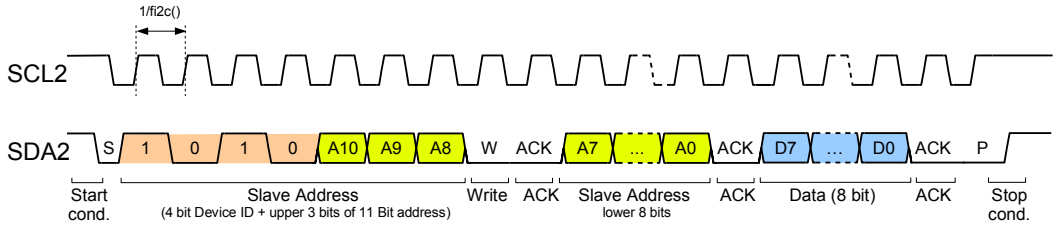


Figure 18: Example of line signals for I2C protocol: write single byte to EEPROM. The second part of the slave address (lower 8 bits) is representing the register address.

General

To automatically configure the Safety Channel at startup an external I²C memory (EEPROM) can be connected at the pins SDA2 and SCL2.

The I²C protocol uses a 7-bit slave ID (0b"1010 AAA") and an 8-bit register address.

I2C Master Performance	
Protocol	Standard I²C
Clock Rate (Output)	125 kHz max. (refer to Elec.Char. E05
Addressing	11-bit: 8-bit register address plus 3-bit block selection
Access Trials	Read: 3x at power-up with CRC failure
Multi-Master Capability	Yes
EEPROM Device Requirements	
Supply Voltage	2.375 V to 5.5 V
Addressing	11-bit address max.
Device Address	0x50 ('1010 000' w/o R/W bit), 0xA0 ('1010 0000' with R/W = 0)
Page Buffer	Not required (byte write only)
Recommended Size	16 Kbit (8x 256x8 bits = 2048 Bytes), type 24C16

Table 19: EEPROM interface performance

If the startup fails, e.g. no EEPROM or incorrect CRC_CFG, the status bits NOEPR or ECRC are set (see Table 91). In this case, the configuration with valid CRC_CFG must be written into the RAM via BiSS or SPI. The command CMD_SC = RESET then has to be executed.

Communication problems, e.g. no slave acknowledge, are signaled on status bit EI2C (see Table 92).

Programming Hint: After writing a byte to the EEPROM, the same byte should be read back. Several read attempts may be required if the I²C interface is still blocked, causing iC-RZ to refuse the read access. When writing to the EEPROM without reading the byte back, a waiting time longer than the write processing time of the EEPROM (typ. about 4 ms) must be allowed after each register.

CRC: General and Output Format Configuration

The configuration for the iC-RZ is split into two areas.

- General configuration (addr. 0x10 to 0x1F)
- Output format configuration for position data (addr. 0x20 to 0x2F)

Each section has its own CRC security against change of configuration. Both the general configuration data and the output format configuration data are protected with a 8-bit CRC (CRC_CFG, CRC_OFF).

At startup the configuration is read and the CRC values are checked. If the check in one configuration section fails, all registers of this configuration section are initialized with the values given in Table 18, the status bit ECRC and according to the failing CRC check ECRC_OFF or ECRC_CFG are set (see Table 91, and 92).

During operation the CRC is checked continuously with the internal system clock fsys (see E01) and the status is displayed at ECRC. If the continuous CRC check fails, zeroed position data is output but no re-initialization is triggered (as it would be the case on re-boot/power-on).

Safety Channel	
CRC_CFG(7:0) Addr. 0x1F; bit 7:0	
Code	Description
0x0 ... 0xFF	CRC value for configuration data (0x10 to 0x1A, 0x1E)
Note	Polynomial 0x11D, start value 0x04

Table 20: CRC value for general configuration

Safety Channel	
CRC_OFF(7:0) Addr. 0x2F; bit 7:0	
Code	Description
0x0 ... 0xFF	CRC value for offset data (0x20 to 0x24, 0x2E)
Note	Polynomial 0x11D, start value 0x04

Table 21: CRC value for output format configuration

The user must calculate the correct CRC_CFG and CRC_OFF values when configuring the EEPROM content for the iC-RZ Safety Channel. An example of a CRC calculation routine for CRC_CFG is given in Listing 1.

```
unsigned char ucDataStream = 0;
int iCRC_CFGPoly = 0x11D;
unsigned char ucCRC_CFG;
int i = 0;

ucCRC_CFG = 4; // start value !!!
// Reg 0x10 to 0x1A
for (iReg = 0x10; iReg<0x1B; iReg ++)
{
  ucDataStream = ucGetValue(iReg);
  for (i=0; i<=7; i++) {
    if ((ucCRC_CFG & 0x80) != (ucDataStream & 0x80))
      ucCRC_CFG = (ucCRC_CFG << 1) ^ iCRC_CFGPoly;
    else
      ucCRC_CFG = (ucCRC_CFG << 1);
    ucDataStream = ucDataStream << 1;
  }
}
// Reg 0x1E
  ucDataStream = ucGetValue(iReg);
  for (i=0; i<=7; i++) {
    if ((ucCRC_CFG & 0x80) != (ucDataStream & 0x80))
      ucCRC_CFG = (ucCRC_CFG << 1) ^ iCRC_CFGPoly;
    else
      ucCRC_CFG = (ucCRC_CFG << 1);
    ucDataStream = ucDataStream << 1;
  }
```

Listing 1: C++ example of CRC_CFG checksum calculation

SERIAL I/O INTERFACES

Both channels have a serial interface to read position data and to write and read registers.

Control Channel

The Control Channel uses the BiSS protocol with the I/O pins summarized in Table 22.

Control Channel		
Pin	BiSS	Function
MA1	MA	Master Clock In
SLO1	SLO	Slave Data Out
-	SLI[1]	Slave Data In
Note	[1] internally connected to ground	

Table 22: Control Channel serial interface pins

Safety Channel

The Safety Channel is capable of using the BiSS, SSI, Extended SSI or SPI protocol with the I/O pins summarized in Table 23.

Safety Channel			
Pin	BiSS/SSI	SPI	Function
NL2	'1'	NL	Not Latch In
NCS2	'1'	NCS	Not Chip Select In
SCI2	MA	SCLK	Master Clock In
SDO2	SLO	MISO	Slave Data Out
SDI2	SLI	MOSI	Slave Data In

Table 23: Safety Channel serial interface pins

The parameter IF_MODE selects the interface protocol. With IF_MODE set to BiSS/SPI (0x0) the logic level at pin NCS2 selects the BiSS or the SPI protocol.

If IF_MODE is set to SPI or SPI-NL (0x4, 0x5), pin SDO2 switches to tristate while iC-RZ is not selected (NCS2 = hi).

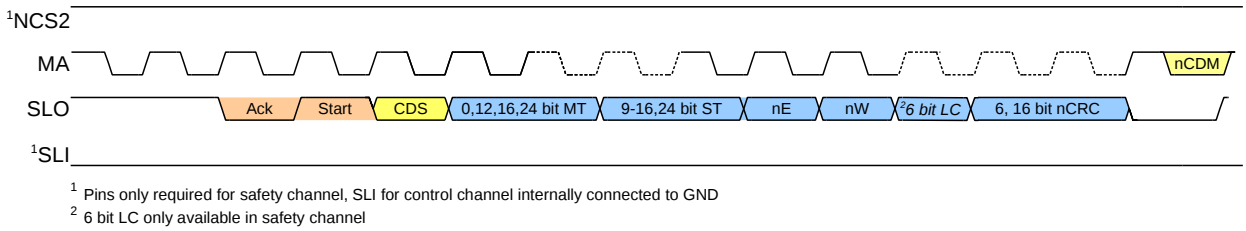
Safety Channel		
IF_MODE(2:0) Addr. 0x13; bit 7:5		
Code	Function	Notes
0x0	BiSS/SPI	NCS2 = hi → BiSS NCS2 = lo → SPI
0x1	BiSS	
0x2	SSI	
0x3	EXTSSI	
0x4	SPI	SDO2 is tristate if NCS2 = hi
0x5	SPI-NL	NL2 = hi → lo: sensor data is requested with the falling edge of NL2; SDO2 is tristate if NCS2 = hi
0x6, 0x7	reserved	

Table 24: Interface mode

Using the serial interface, position data can be obtained only if CRC_CFG and CRC_OFF are both valid.

When operating the channels in BiSS chain, the Control Channel must be in front (no SLI input) and occupy the BiSS slave ID 0.

BiSS INTERFACE



[1] Pins only required for safety channel, SLI for control channel internally connected to GND
[2] 6 bit LC only available in safety channel

Figure 19: BiSS protocol single cycle data (actual pin names see Table 22, 23)

Overview

BiSS Slave Performance		
Parameter	Symbol	Description
Clock Rate	t_C	10 MHz max.
Timeout	t_{out}	adaptive (typ. 0.35 µs @ 10 MHz)
Control Channel		
Safety Channel		
Process.T.	t_{busy} [1]	typ. 0.5 µs
Inp. Buffer		8 bit max. for SLI data buffering
SCD Channel 1: Position Data		
Bits/cycle	ID	Description
Control Channel		
12, 16, 24	MT	Multiturn Data (right-justified)
16, 20, 24	ST	Singleturn Data (left-justified)
1	nE [2]	Error bit ERR
1	nW [2]	Warning bit WARN
6	CRC [3]	Polynomial 0x43, start value 0x00
Safety Channel		
12, 16, 24	MT	Multiturn Data (right-justified)
9 ... 16	ST	Singleturn Data (left-justified)
1	nE [2]	Error bit ERR
1	nW [2]	Warning bit WARN
6	LC	Sign-of-life Counter
16	CRC [3]	Polynomial (0x190D9), adjustable start value [4]
CD Channel: Control Data		
Bits/cycle	ID	Description
Control Channel		
Safety Channel		
1	nCDM [2], CDS	Full support of bidirectional register access and selected BiSS protocol commands (see Table 26)
Notes	[1] See Operating Requirements, items I006, I007; [2] Low active transmission [3] Bit inverted transmission. [4] See Table 31 for CRC_ID	

Table 25: BiSS slave performance

The BiSS C interface serial bit stream is binary coded. The error and warning bits are low active. Transmission of sensor and register data is implemented. The BiSS protocol is compatible with the BiSS Safety Standard for the Control and Safety Position Words (CPW resp. SPW).

BiSS protocol commands

BiSS C protocol commands are supported according to Table 26. These commands can be used for BiSS bus establishment if more than 8 slaves are connected to the BiSS Master. For further information regarding the BiSS-C protocol visit www.ichaus.de/BiSS Interface.

CD Channel: BiSS Protocol Commands		
Control Channel		
Safety Channel		
CMD	Availability	Function
Addressed (IDS > 0x00)		
00	Yes	Activate Single-Cycle Data channels
01	—*	Deactivate control communication
10	—	To be defined
11	—	To be defined
Broadcast (all slaves: IDS = 0x00)		
00	Yes	Deactivate Single-Cyc. Data channels
01	—	Activate control communication
10	—	Bus coupler bypass
11	—	Reserved
Notes	* Command w/o function, but will be acknowledged.	

Table 26: BiSS Protocol Commands

Control Channel

Multiturn, singleturn position, error bit (nE) and warning bit (nW) can be transmitted in the single cycle data of the Control Channel. The data is secured with a 6-bit CRC transmitted inverted (nCRC).

A physical slave data input pin does not exist for the Control Channel. It acts as if a virtual slave data input is connected to low.

Thus the Control Channel must always be the last slave in a BiSS chain.

The initial configuration of the singleturn and multiturn data length for the Control Channel (CPW) is done with pins CFG11/10 and is summarized in Table 27.

The state of the pins CFG11/10 is latched at power-on and the resulting data length configuration is saved in parameters DL_ST_CC and DL_MT_CC.

See Table 17 for a summary of the Control Channel features configured with the CFG10 and CFG11 pins.

Control Channel			
Pins CFG11/10: Single Cycle Data Length			
CFG11	**CFG10**	**DL_ST_CC**	**DL_MT_CC**
0	0	16 bit[2]	0 bit
0	1 / x[1]	24 bit[2]	12 bit
x[1]	0	24 bit[2]	12 bit
1	0 / x[1]	24 bit[2]	16 bit
x[1]	1	24 bit[2]	16 bit
1	1	24 bit[2]	24 bit
x[1]	x[1]	24 bit[2]	24 bit
Notes	With MT only 24 bit ST is possible (due to ADI of iC-MR3). [1] x = pin open or set to 2.5V (= VIO1/2) [2] ST data is resolved to 15 bits; remaining bits are 0.		

Table 27: BiSS Configuration Control Channel

A temporary change of the ST and MT data length during operation is possible using parameters DL_ST_CC and DL_MT_CC.

Control Channel			
DL_ST_CC(3:0) Addr. 0x12; bit 3:0			
Code	ST length	Code	ST length
0000	9 bits	1000	17 bits
0001	10 bits	1001	18 bits
0010	11 bits	1010	19 bits
0011	12 bits	1011	20 bits
0100	13 bits	1100	21 bits
0101	14 bits	1101	22 bits
0110	15 bits	1110	23 bits
0111	16 bits	1111	24 bits
Note	Reset value configurable with pins CFG11/10 ST data is resolved to 15 bits; remaining bits are 0. Settings marked blue are available by pin configuration at CFG11/CFG10.		

Table 28: Singleturn Data Length

Control Channel	
DL_MT_CC(1:0) Addr. 0x12; bit 5:4	
Code	MT length
00	0 bit
01	12 bits
10	16 bits
11	24 bits
Note	Reset value configurable with pins CFG11, CFG10. All settings available by pin configuration.

Table 29: Multiturn Data Length

Safety Channel

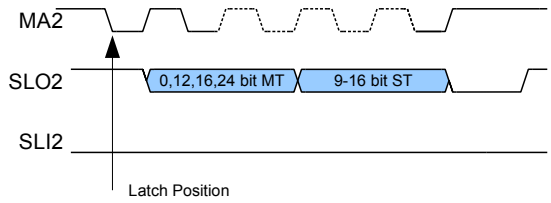


Figure 20: SSI protocol

The Safety Channel can be configured to use the BiSS, SSI or Extended SSI protocol using parameter IF_MODE (see Table 30). For an example of the BiSS signals refer to Figure 19, for the SSI signals refer to Figure 20.

Ensure that SLI (SDI2) is connected to GND2 if the BiSS interface of the iC-RZ Safety Channel is connected to a BiSS master in a point-to-point, single slave application.

To get position data after startup, the configuration data of the Safety Channel has to be marked valid by a correct CRC_CFG check (see info box on page 31).

The startup phase must be completed before BiSS/SSI communication. A minimum waiting time of **15 ms*** should be kept ahead of clocking at SCI2 (= MA). Alternatively, startup completion can be observed at pin SDO2 changing from tristate to driving high.

*) An external MT could add a delay. See chapter STARTUP PROCESS for further details on timings.

Safety Channel		
IF_MODE(2:0) Addr. 0x13; bit 7:5		
Code	Function	Notes
0x0	BiSS/SPI	NCS2 = hi → BiSS
0x1	BiSS	
0x2	SSI	
0x3	EXTSSI	

Table 30: Interface Mode: BiSS/SSI

When using the BiSS or the Extended SSI protocol (EXTSSI) a sign-of-life counter (LC) is transmitted after the nE/nW bits. The counter is incremented after every complete SCD frame transmission and has a value range of 1 to 63.

If the transmission is interrupted before sending the CRC value, the sign-of-life counter (LC) is not increased.

BiSS and SPI are using a shared sign-of-life counter, i.e. when using IF_MODE = 0x0 the LC will count on BiSS and SPI sensor data requests.

The data is secured with a 16-bit CRC transmitted inverted (nCRC). The start value for the CRC calculation can be configured with CRC_ID (see Table 31).

In the extended SSI mode all data is sent with the MSB first and is equivalent to the data package that is output when using the BiSS protocol.

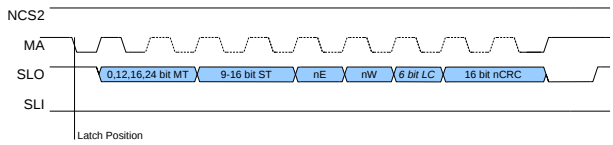


Figure 21: Extended SSI protocol

Safety Channel	
CRC_ID(5:0) Addr. 0x15; bit 5:0	
Code	CRC start value
000000	000000 *(default)*
...	...
111111	111111

Table 31: CRC Start Value for Position Data

The multiturn output data length can be configured with DL_MT_SC.

Safety Channel	
DL_MT_SC(2:0) Addr. 0x12; bit 5:4	
Code	MT length
00	0 bit
01	12 bits
10	16 bits
11	24 bits

Table 32: Multiturn Data Length

When using the SSI protocol with multiturn data, note that DL_MT has to be set to 12 bit to match Standard SSI.

The singleturn output data length can be configured with DL_ST_SC.

Safety Channel			
DL_ST_SC(2:0) Addr. 0x12; bit 2:0			
Code	ST length	Code	ST length
000	9 bits	100	13 bits
001	10 bits	101	14 bits
010	11 bits	110	15 bits
011	12 bits	111	16 bits[1]
Note	[1] ST data is resolved to 15 bits; remaining bits are 0.		

Table 33: Singleturn Data Length

When using the standard SSI protocol with singleturn data length (DL_ST) < 13 bits the SSI data word is zero filled to match an output data length of 13 bit.

SPI INTERFACE (SC)

SPI Protocol

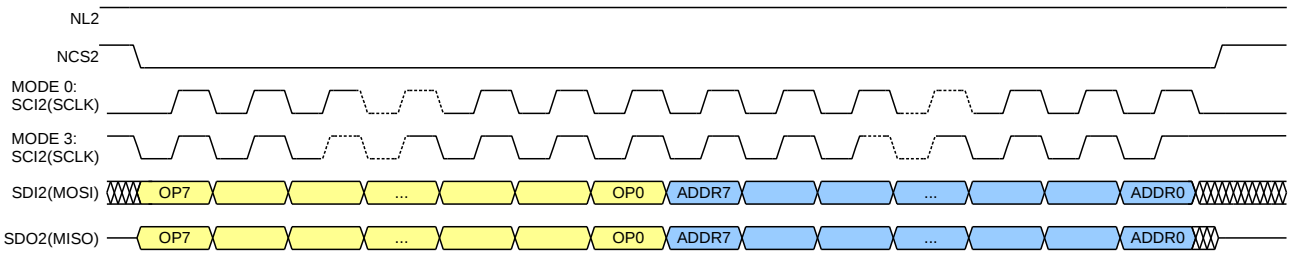


Figure 22: SPI protocol Safety Channel

Safety Channel	
SPI Sensor Data	
CRC Bits	16
Polynomial	0x190D9[1)]
Start Value	programmable[2)]
Closing Value	0xFFFF[3)]
Error	1-bit low active
Warning	1-bit low active
Sign-of-life(LC)	6-bit
Notes	[1)] Polynomial with first and last 1 [2)] CRC_ID see Table 31 [3)] i.e. CRC transmitted inverted

Table 34: SPI SDAD transmission parameters

Safety Channel		
IF_MODE(2:0) Addr. 0x20; bit 7:5		
Code	Function	Notes
0x0	BiSS/SPI	NCS2 = lo → SPI
0x4	SPI	SDO2 is tristate if NCS2 = hi
0x5	SPI-NL	NL2 = hi → lo: sensor data is requested with the falling edge of NL2; SDO2 is tristate if NCS2 = hi

Table 35: Interface Mode: SPI

The Serial Peripheral Interface (SPI) can be used to read/write registers and to read position data. SPI modes 0 and 3 are supported, i.e. idle level of SCLK 0 or 1, acceptance of data on a rising edge (see Figure 22).

iC-RZ is selected with a logic level 0 on NCS2. Data is sent in packets of 8 bits with the MSB first. Each data transmission starts with the master sending an opcode (Table 36) to the slave.

Safety Channel	
OPCODE	
Code	Description
0xB0	ACTIVATE
0xA6	SDAD-transmission (sensor data)
0xF5	SDAD Status
0x97	Read REGISTER(single)
0xD2	Write REGISTER (single)
0x81	Read REGISTER (cont.) delayed *
0xCF	Write REGISTER (cont.)
0x9C	Read STATUS (STATUS_SPW0..STATUS_SPW3)
0xD9	Write INSTRUCTION (CMD_SC)
0xAD	REGISTER status/data
Notes	* Address range 0x00 to 0x2F can be read out, but data is only available from 0x10.

Table 36: SPI OPCODEs

Opcode ACTIVATE

Safety Channel	
OPCODE	
Code	Description
0xB0	ACTIVATE

Table 37: SPI Opcode: ACTIVATE

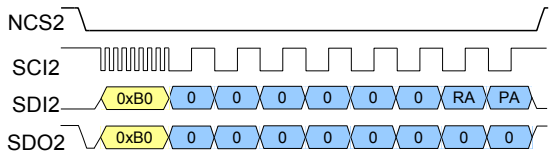


Figure 23: Set ACTIVATE: RACTIVE/PACTIVE

Using the **ACTIVATE** command, the register and sensor data channels of the connected slaves are switched on and off. After startup the register communication

and data channel are activated, so no action by the user is necessary.

Safety Channel	
RACTIVE	
Code	Description
0	Register communication deactivated
1	Register communication activated*)
PACTIVE	
Code	Description
0	Sensor data channel deactivated
1	Sensor data channel activated*)
Note	*) default after startup

Table 38: RACTIVE and PACTIVE bits

Opcode Read REGISTER (single)

Safety Channel	
OPCODE	
Code	Description
0x97	Read REGISTER (single)

Table 39: SPI Opcode: Read REGISTER (single)

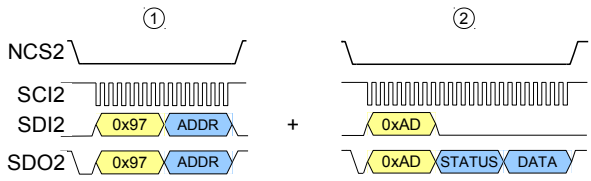


Figure 24: Read Register: set the read address (1) + command REGISTER status/data to read-out data (2)

To read register data from the slave byte by byte, the **Read REGISTER (single)** command can be used. The master first transmits the Read REGISTER opcode followed by the address ADDR. The slave immediately outputs the opcode and address at MISO.

Following this, using the **REGISTER status/data** command the master can poll until the validity of the DATA following the SPI-STATUS byte is signaled via SPI-STATUS.

Opcode REGISTER status/data

Safety Channel	
OPCODE	
Code	Description
0xAD	REGISTER status/data

Table 40: SPI Opcode: REGISTER status/data

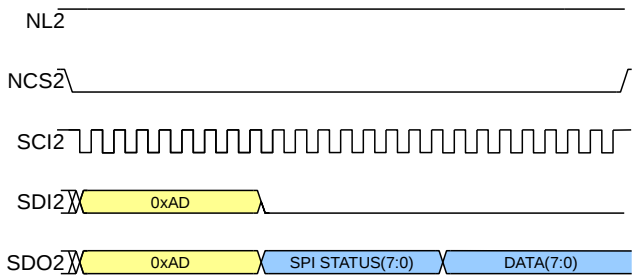


Figure 25: Read Status and Data

The **REGISTER status/data** command can be used to request the status of the last register communication and/or the last data transmission. The SPI-STATUS byte contains the information summarized in Table 41.

All SPI status bits are updated with each register access. The exception to the rule is the ERROR bit; this bit indicates whether an error occurred during the last SPI-communication with the slave.

The master transmits the **REGISTER status/data** opcode. The slave immediately passes the opcode on to MISO. The slave then transmits the SPI-STATUS byte and a DATA byte.

Safety Channel		
SPI-STATUS		
Bit	Name	Description of the status report
7	ERROR	Opcode not implemented, sensor data were not ready for output
6..4	-	Reserved
Status bits of the register communication		
3	DISMISS	Address rejected
2	FAIL	Data request has failed
1	BUSY	Slave is busy with a request
0	VALID	DATA is valid/register communication terminated successfully
Note	Display logic: 1 = true, 0 = false	

Table 41: Communication status byte

Following the **Read REGISTER (single)** command the requested data byte is returned via DATA . The validity of the DATA byte is signaled with the VALID status bit.

Following the **Write REGISTER (single)** command, the data to be written is repeated in the DATA byte. With all other opcodes, the DATA byte is not defined.

In general bits 0 to 3 of the SPI-STATUS byte reflect the status of the register communication.

Opcode Write REGISTER (single)

Safety Channel	
OPCODE	
Code	Description
0xD2	Write REGISTER (single)

Table 42: SPI Opcode: Write REGISTER (single)

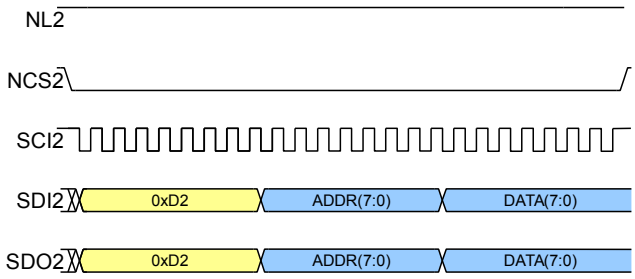


Figure 26: Write Register

Data is written to the slave byte by byte using the **Write REGISTER (single)** command.

The master first transmits the **Write REGISTER (single)** opcode followed by the address (ADDR) and the data (DATA). The slave immediately outputs the opcode, address, and data at MISO.

Using the **REGISTER status/data** command, the master can poll the end of communication (signaled via the SPI-STATUS byte).

Opcode Read REGISTER (cont.) delayed

Safety Channel	
OPCODE	
Code	Description
0x81	Read REGISTER (cont.) delayed

Table 43: SPI Opcode: Read REGISTER (cont.)

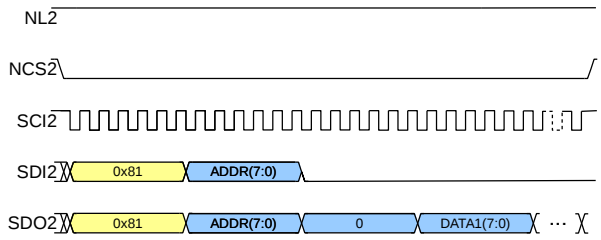


Figure 27: Read Register (cont.)

This command can only be used for reading data from internal registers. When reading data from internal registers the slave does not need any processing time.

The internal iC-RZ registers are addressed with BSEL = 0x0, I2CDEV = 0x0 and addr. 0x00 to 0x2F and also addr. 0x40 to 0x7F. These registers can be read out in continuous mode.

The master transmits the **Read REGISTER (cont.) delayed** opcode. In the second byte, the start address ADDR is transmitted. The slave immediately outputs the opcode, address followed by a ZERO-byte and then transmits the DATA1 data. The internal address counter is incremented following each data packet.

If an error occurs during register readout in continuous mode (e.g. the address is invalid or the requested data is not yet valid on data byte clock out), the internal address counter is no longer incremented and the error bit FAIL is set in the communication status register.

The command **Read REGISTER (cont.) delayed** can not be used to continuously read data from an external EEPROM as iC-RZ needs processing time to obtain the data.

The status of the register communication should be checked using the **REGISTER status/data** command.

Opcode Write REGISTER (cont.)

Safety Channel	
OPCODE	
Code	Description
0xCF	Write REGISTER (cont.)

Table 44: SPI Opcode: Write REGISTER (cont.)

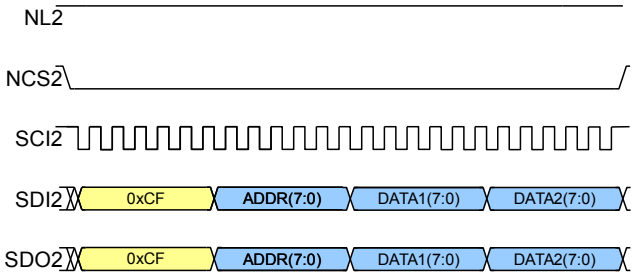


Figure 28: Write Register (cont.)

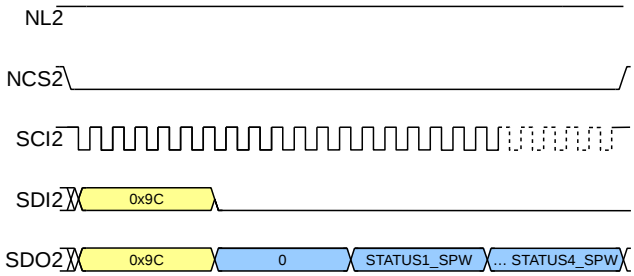


Figure 29: Read Status

When writing data into internal registers, the slave does not need any processing time.

The internal iC-RZ registers are addressed with BSEL = 0x0, I2CDEV = 0x0 and addr. 0x00 to 0x3F. These registers can be written in continuous mode.

The master transmits the **Write REGISTER (cont.)** opcode. In the second byte start address ADDR is transmitted, followed by the DATA1-DATAn data packets to be written. The slave immediately outputs the opcode, address and data at MISO. The slave increments its internal address counter following each data packet.

If an error occurs while writing to a register in continuous mode (e.g. the address is invalid or the data write process of the last address was not finished), the internal address counter is no longer incremented and the error bit FAIL is set in the communication status register.

The status of the register communication should be checked using the **REGISTER status/data** command.

Opcode Read STATUS

Safety Channel	
OPCODE	
Code	Description
0x9C	Read STATUS registers

Table 45: SPI Opcode: Read STATUS

The command **Read STATUS** gives access to the internal status registers and the temperature value.

The opcode is followed by a ZERO-byte and the STATUS1_SPW, STATUS2_SPW, STATUS3_SPW, TEMP and STATUS4_SPW bytes. For more information regarding the status bytes refer to page 62 ff. The temperature representation of TEMP can be found in Table 76, page 58.

The status of the register communication should be checked using the **REGISTER status/data** command.

Opcode Write INSTRUCTION

Safety Channel	
OPCODE	
Code	Description
0xD9	Write INSTRUCTION (CMD_SC)
Note	CMD_SC see page 67

Table 46: SPI Opcode: Write INSTRUCTION

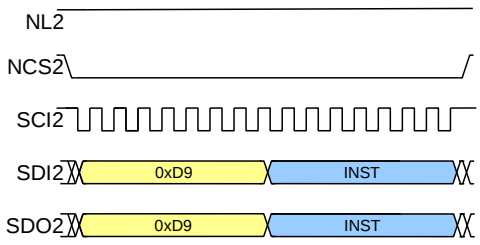


Figure 30: Write INSTRUCTION

The command **Write INSTRUCTION** gives access to the internal, slave-specific command register. Command CMD_SC (see Table 101) is set with the instruction data byte (INST), which is send after the opcode.

The status of the register communication should be checked using the **REGISTER status/data** command.

Opcode SDAD-transmission

Safety Channel	
OPCODE	
Code	Description
0xA6	SDAD-transmission (sensor data)

Table 47: SPI Opcode: SDAD-transmission

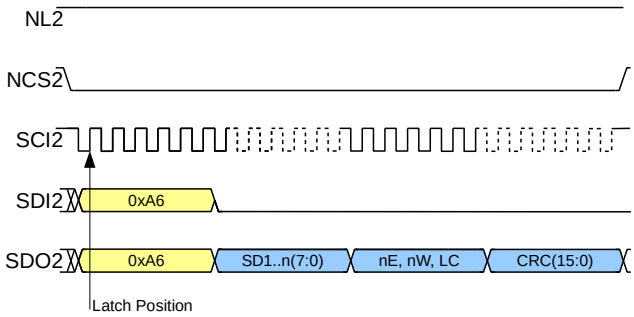


Figure 31: Sensor data read with latching by SCI2 (IF_MODE = 0x0, 0x4)

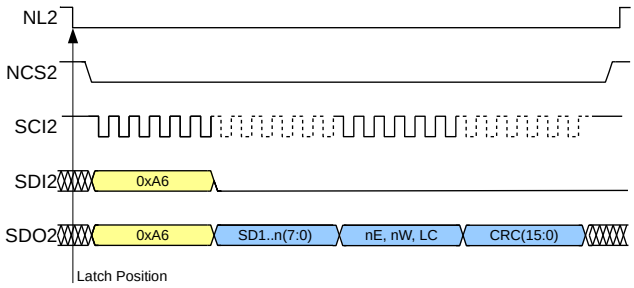


Figure 32: Sensor data read with latching triggered by NL2 (IF_MODE = 0x5)

To read position data, the command **SDAD-transmission** must be used.

The sample point for the internal data generation is defined as follows:

1. IF_MODE = 0x0, 0x4: sample point defined by NCS = 0 and first rising edge SLC2 (see Figure 31)
2. IF_MODE = 0x5: sample point defined by falling edges NL2 (see Figure 32). NL must stay at zero until the sensor data was read out using command SDAD transmission.

The slave is able to output the sensor data (SD) immediately after the master has send the **SDAD transmission** opcode. After the opcode the sensor data shift register is clocked out.

The variable bit count for the sensor data following the SPI opcode **SDAD transmission** is derived from the parameters DL_ST_SC (Table 33). The sensor data is followed by one additional byte, consisting of one low-active Error bit, one low-active Warning bit and a 6 bit sign-of-life counter (range of values: 1 to 63). iC-RZ ensures that the total output data length is a multiple of 8 bits by adding zero-bits between the sensor data and the additional byte. The sensor data, optional zero-bits and the additional byte is secured with a 16 bit CRC formed with the polynomial 0x190D9 transmitted inverted (nCRC). The start value for the CRC calculation can be selected with the parameter CRC_ID (see Table 31).

SPI and BiSS are using a shared sign-of-life counter, i.e. when using IF_MODE = 0x0 the LC will count on SPI and BiSS sensor data requests.

If the internal data generation was not completed or iC-RZ is not ready for sensor data requests but data is sampled in the sensor data shift register, the ERROR bit is set in the SPI-STATUS byte (see Table 41) and the sensor data and the additional byte are set to zero.

Opcode SDAD status

Safety Channel	
OPCODE	
Code	Description
0xF5	SDAD Status (sensor data)

Table 48: Opcode: SDAD Status

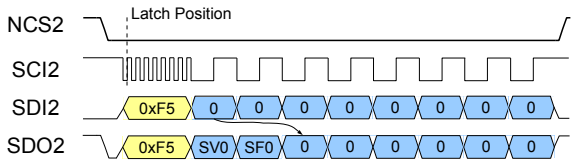


Figure 33: SDAD status

For compatibility issues with other iC-Haus products using this SPI protocol the SDAD status command is supported, i.e. sensor data can be requested using the opcode **SDAD status**. Each iC-RZ has one SVALID (SV) register to signal the end of conversion and one SFAIL (SF) register to signal a failing sensor data request. If iC-RZ is connected directly to the SPI master the SVALID (SV0) and SFAIL (SF0) bits are placed at bit positions 7 and 6 in the SVALID byte as shown in Figure 33.

The **SDAD status** command causes:

1. All slaves activated with PACTIVE = 1 (see Table 38) to output their SVALID and SFAIL registers in the data byte following the opcode.
2. The next request for sensor data started with the first rising edge at SCL2 of the next SPI communication is ignored by the slave.

Using this command, the master can cyclically poll for the successful end of the sensor data generation signaled with SVALID (SV). The sensor data is read out with the command **SDAD transmission**.

After SFAIL (SF) was set, the first rising edge at SCL2 of the next SPI communication requests new sensor data (Figure 34).

Safety Channel	
SVALID	
Code	Description
0	Sensor data generation in progress
1	Sensor data ready
SFAIL	
Code	Description
0	Sensor data request okay
1	Sensor data request failed, e.g. iC-RZ not ready for position data output

Table 49: SVALID and SFAIL bits

Figure 34 shows the interaction of the two commands **SDAD Status** and **SDAD transmission**. The sensor data communication starts with the command **SDAD Status** (1). The first **SDAD Status** requests new data. Following **SDAD Status** commands are used to check for the data to be ready to output (no new sensor data requests are issued). If the sensor data is signaled to be ready with SVALID (SV), the opcode **SDAD-transmission** (2) must be sent to read out the sensor data. At this point sensor data requests are enabled again. Finally the command **REGISTER status/data** should be executed to detect an unsuccessful SPI communication.

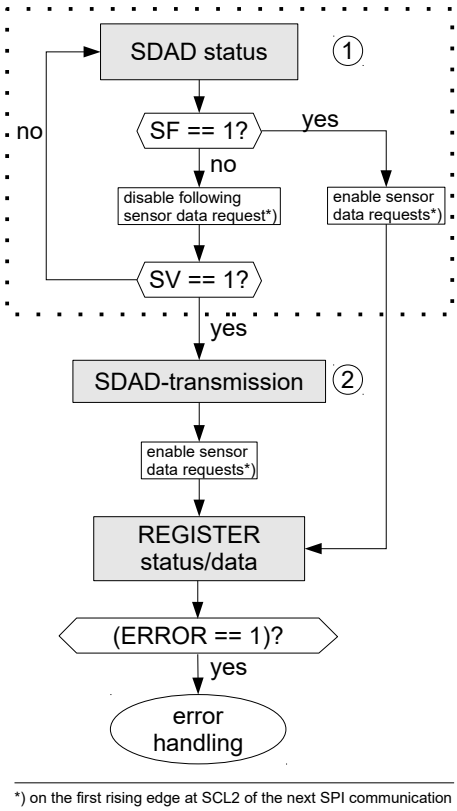


Figure 34: Example sequence of the commands SDAD Status/SDAD-transmission

If a test mode is activated, SPI communication is no longer possible. A reset per pin or a power cycle is required.

REGISTER ACCESS

Control Channel: BiSS

Figure 35 summarizes the accessible registers of the Control Channel using the BiSS protocol. For the configuration parameters of the Control Channel refer to chapter REGISTER MAP (CC).

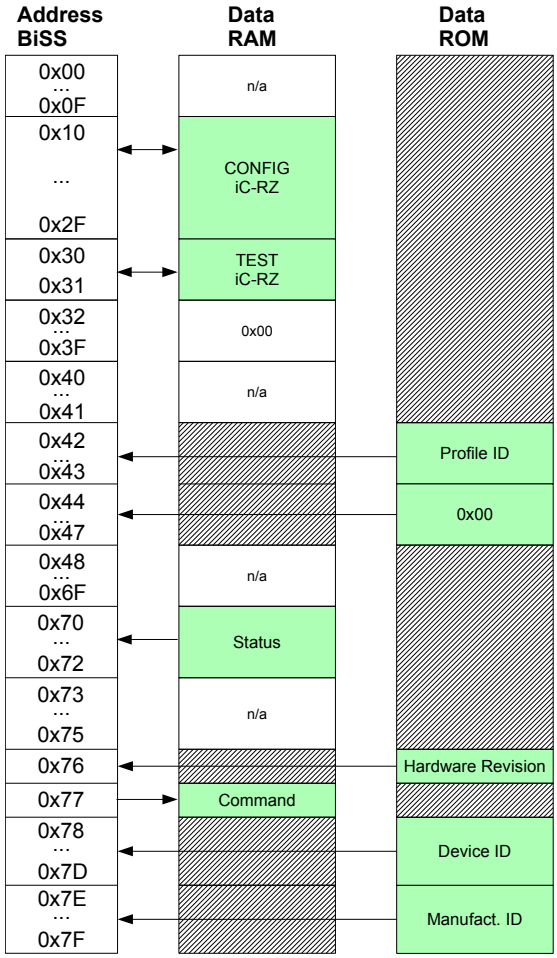


Figure 35: Control Channel: accessible registers

After startup the register write protection is enabled to prevent unwanted changes of the configuration data. CMD_CC = **RPL_RESET** can be used to disable the register write protection. CMD_CC = **RPL_SET_RO** can be used to enable the register write protection.

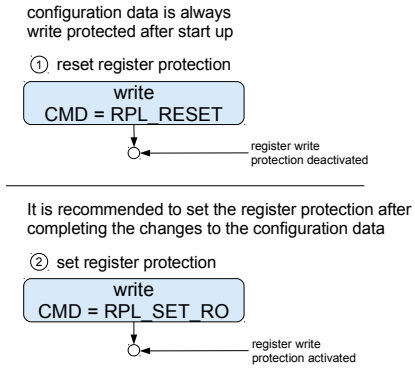


Figure 36: Setting/resetting register protection

Safety Channel: Overview and register protection

The Safety Channel uses BiSS or SPI for register communication.

The configuration data of the Safety Channel of iC-RZ is split into two areas.

- General configuration (addr. 0x10 to 0x1F)
- Output format configuration for position data (addr. 0x20 to 0x2F)

Each area has its own register protection against change of configuration.

Register protection for the general configuration data is configured with PROT_CFG, for the output format with PROT_OFF. A value other than 0x0 has to be written to PROT_CFG or PROT_OFF to set the register protection for the corresponding configuration data area.

Tables 50 and 51 summarize the affected addresses for each register protection area.

Safety Channel		
PROT_CFG		
Protection active for	**write protection** PROT_CFG(6:0) /= 0	**read&write protection** PROT_CFG(7) /= 0
Bank 0: Addr. 0x10 - 0x1F	✓	✓
Bank 0: Addr. 0x30 - 0x31	✓	✓
Bank 1: Addr. 0x00 - 0x1F	✓	✓
Protection active for	**write protection** PROT_CFG /= 0	
Bank 2-15 Addr. 0x41-0x6F	✓ ✓	

Table 50: PROT_CFG: Protected addresses

Safety Channel	
PROT_OFF	
Protection active for	**write protection** PROT_OFF /= 0
Bank 0: Addr. 0x20 - 0x2F	✓
Bank 1: Addr. 0x20 - 0x2F	✓

Table 51: PROT_OFF: Protected addresses

Register protection can be configured temporarily by setting PROT_CFG or PROT_OFF in the internal RAM (bank 0) or permanently by setting PROT_CFG or PROT_OFF in the EEPROM (bank 1). If it is enabled in the EEPROM, the register protection for each area is automatically activated after startup and a valid CRC check of the corresponding area. If it is enabled in the internal RAM, the register protection for each area is activated with the command **RESET** (see Table 101) if the CRC of the corresponding area is valid.

To reset the register protection of the configuration or output format register area, the register value of PROT_CFG or PROT_OFF respectively has to be written into the internal RAM (bank 0) again.

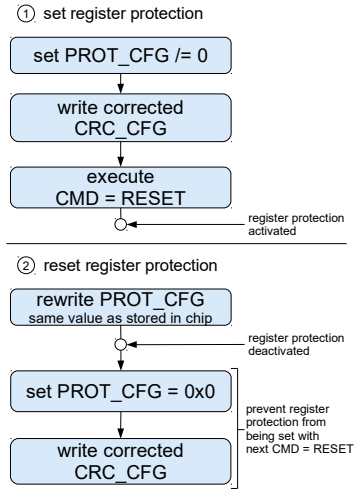


Figure 37: Enabling/disabling register protection

Safety Channel	
PROT_CFG(7:0) Addr. 0x1E; bit 7:0	
Code	Description
0x00	No protection (default)
0x01 ... 0x7F	Write protection
0x80 ... 0xFF	Write and read protection

Table 52: Register Protection for General Configuration

Safety Channel	
PROT_OFF(7:0) Addr. 0x2E; bit 7:0	
Code	Description
0x00 0x01 ... 0xFF	No protection (default) Write protection

Table 53: Register Protection for Output Format and Offset

The status of the register protection can be checked with status bits ENRPCFG and ENRPOFF (see Table 91). If set to '1', register protection is active.

Safety Channel: SPI and BiSS

The address mapping of iC-RZ corresponds to the document BiSS C Protocol Description, which can be downloaded at www.ichaus.de/BiSS_Interface.

iC-RZ supports an addressing scheme using banks. Therefore the internal address space is divided into banks of 64 bytes each. The address sections visible via the I/O interface consists of a dynamic section (addr. SER: 0x00 to 0x3F, content selectable with BSEL and I2CDEV) and a static section which is permanently visible (addr. SER: 0x40 to 0x7F, content independent of BSEL and I2CDEV).

The different memory banks can be addressed with BSEL. With I2CDEV set to 0x0, BSEL is used to address the EEPROM memory range from 0x000 to 0x7FF (11-bit address range) as well as the internal RAM content. Bank 0 selects the internal RAM content with the configuration parameters (refer to chapter REGISTER MAP (SC)). Starting with bank 1 the EEPROM is addressed. The memory map in Figure 38 summarizes the accessible registers and the EEPROM areas using the parameter BSEL.

Safety Channel	
BSEL(4:0) Addr. 0x40; bit 4:0	
Code	Selected bank
0x00 ... 0x1F	Bank 0 ... Bank 31
Note	To access the iC-RZ configuration area, parameter I2CDEV must be set to 0x00.

Table 54: Bank Selection

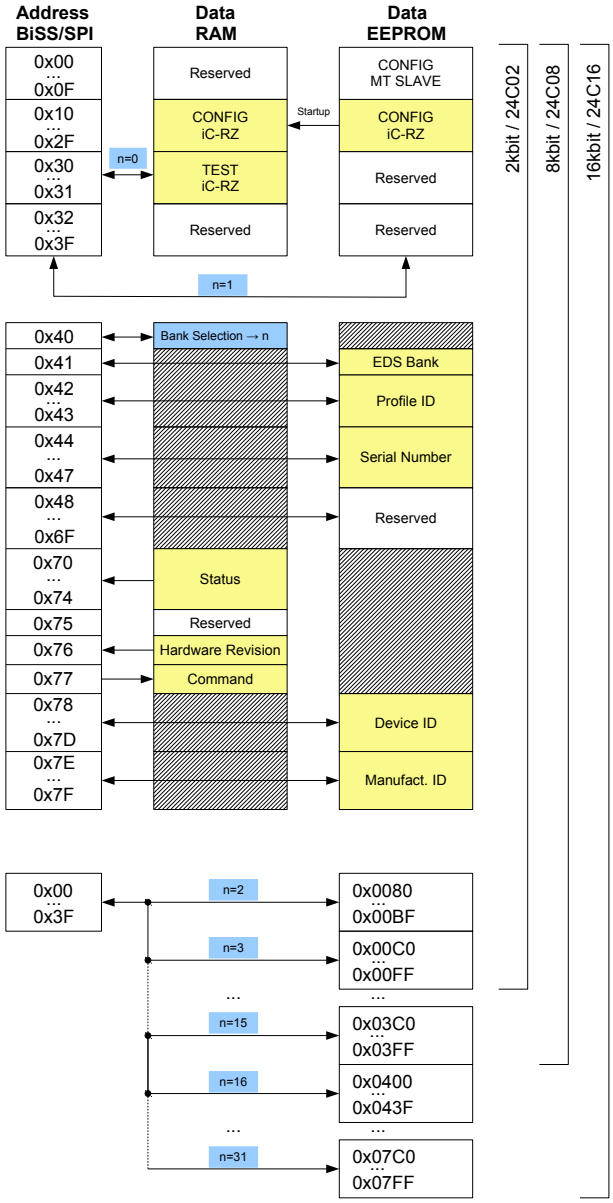


Figure 38: EEPROM register map with I2CDEV = 0x00

I2CDEV determines the I2C Device ID (upper 4 bits, see Figure 18, page 33). This enables access to I2C slaves other than the configuration EEPROM, which are connected to the same I2C bus using different I2C device IDs (see Figure 39 for address mapping).

Safety Channel	
I2CDEV(2:0)	Addr. 0x40; bit 7:5
Code	Device ID
0x0	0b"1010"
0x1	0b"1001"
0x2	0b"1010"
0x3	0b"1011"
0x4	0b"1100"
0x5	0b"1101"
0x6	0b"1110"
0x7	0b"1111"
Note	Only devices with an addressing scheme similar to Figure 18 can be used.

Table 55: Device ID

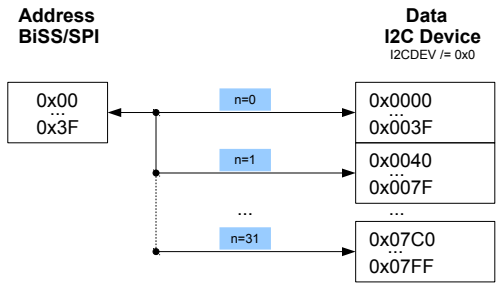


Figure 39: Register map of dynamic section with I2CDEV

SYNCHRONIZATION LOGIC

Position Data Generation
The internal position signals are latched with an incoming position data request from the BiSS (CC and SC), SSI or SPI (only SC) interface.

The following position data is used:

- 5-bit interpolation value of 1024 CPR sine/cosine signals
- 10-bit absolute code from random track
- multiturn value (optional)

The internal interpolation is done using a real-time analog-to-digital converter with no processing time or delay, generating a 5-bit digital word.

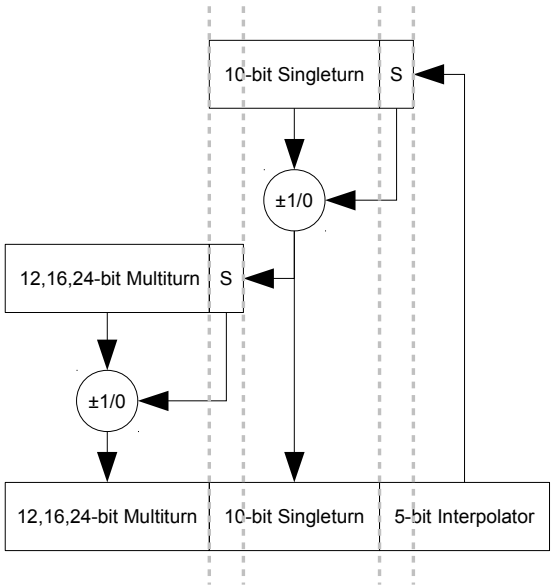


Figure 40: Synchronization position value

The 10-bit absolute digital value, converted from the 10-bit absolute Pseudo-random Code, is synchronized with the 5-bit interpolation value.

The phase-shift between 1024 CPR sine/cosine and the random track should not exceed ±90°. A precise alignment of code disc to sensor is required (see chapter ALIGNMENT page 68).

The multiturn data is also synchronized with the 15-bit singleturn position data to obtain a continuous data value. For this purpose, the multiturn value must count up or down around the zero position of the singleturn to obtain the maximum margin of synchronization. For further details about the configuration of the multiturn system see chapter MULTITURN FUNCTIONS (page 50).

Safety Channel: Offset
For the Safety Position Word (SPW), a position offset can be programmed and an inversion of the code direction can be selected (see Figure 41).

Safety Channel	
OFF_MT(23:16)	Addr. 0x20; bit 7:0
OFF_MT(15:8)	Addr. 0x21; bit 7:0
OFF_MT(7:0)	Addr. 0x22; bit 7:0
Code	Description
0x000000 ... 0xFFFFFF	Multiturn Offset Data (right,aligned, LSB position fix, zero-padded, see Figure 41)

Table 56: Multiturn Offset Data

Safety Channel	
OFF_ST(14:7)	Addr. 0x23; bit 7:0
OFF_ST(6:0)	Addr. 0x24; bit 7:1
Code	Description
0x0000 ... 0x7FFF	Singleturn Offset Data (left-aligned, MSB position fix, zero-padded, see Figure 41)

Table 57: Singleturn Offset Data

To get the same position as the Control Channel (CPW), a ST offset of about 356 has to be set. The effective value has to be measured for each system.

Safety Channel	
DIR	Addr. 0x24; bit 0
Code	Description
0	Code direction not inverted
1	Code direction inverted

Table 58: Code Direction

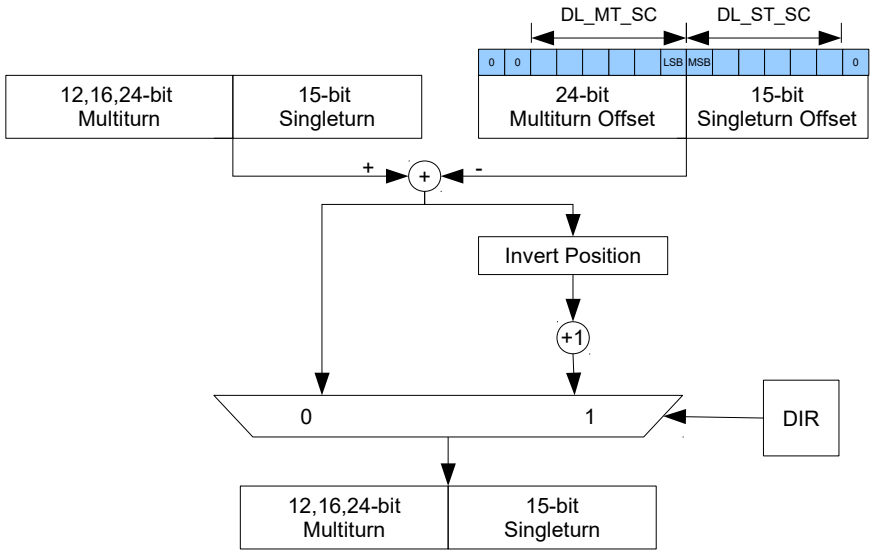
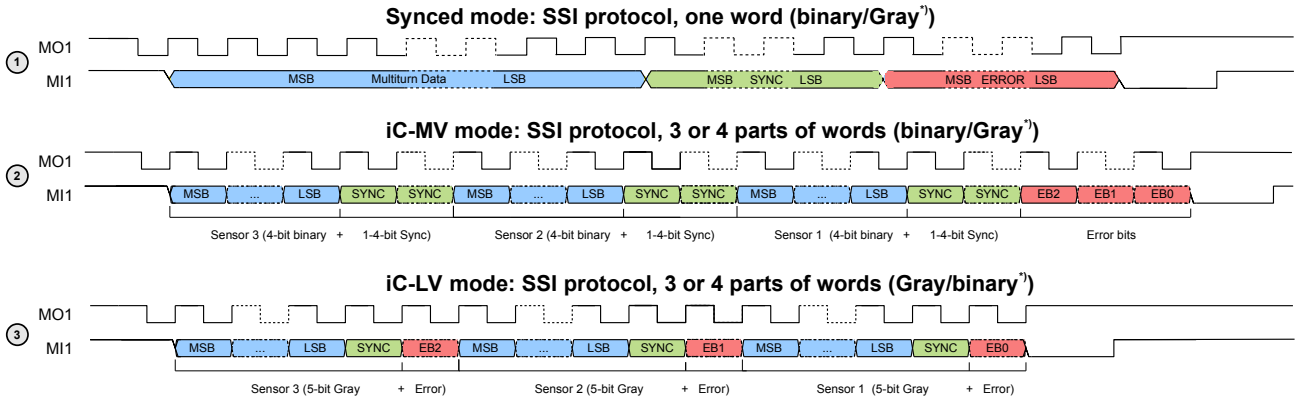


Figure 41: Offset and code direction calculation (Safety Channel only)

MULTITURN FUNCTIONS



*) CC: first option pin programmable; second option configurable with MTMODE

Figure 42: External serial MT interface: SSI protocol with possible MT data formats

The Control and Safety Channel are both multiturn capable. The multiturn functions are identical, just the way of configuration is different. The multiturn information can be obtained from an external or internal data source:

- External serial multiturn interface: SSI
- Internal 24-bit revolution counter

Key features:

- SSI Master
- SSI Protocol with sync and error bit
- Data formatted as one word (synced) or parts of words (unsynced)
- Adjustment mode available (see Table 69, p. 54)

MT Interface: SSI Overview

Control Channel	
Safety Channel	
MT Parameter: SSI	
typ. Timing	
Clock frequency	150 kHz
Timeout	20 µs
Cycle time	1.5 ms
Data length	
Data length	12 / 16 bit
Sync. bits	CC pin config: 1 or 3; SBL_MT_x: 1-4
Error bits (active low)	CC pin config: 0 or 1; EBL_MT_x: 0-4
Control Channel	
Function	Pin
Clock output	MO1
Data input	MI1
Safety Channel	
Function	Pin
Clock output	MO2
Data input	MI2

Table 59: External MT protocol parameters

The internal SSI multiturn master is reading the multiturn information from external MT devices. Pin MO1 is the clock output and MI1 the data input of the Control Channel. Pin MO2 is the clock output and MI2 the data input of the Safety Channel.

The number of clock cycles depends on the configuration of the multiturn interface. Multiturn data can be received as one word or as parts of words, each with its own synchronization bits. The multiturn interface uses the synchronization information to synchronize the parts of words of the multiturn data to each other and synchronizes the resulting multiturn data word to the singleturn data.

The tolerable phase shift / synchronization range depends on the number of synchronization bits. The optimum phase shift (mechanical offset) is in the middle of the synchronization range.

The number of error bits which are send with the multiturn data package is configurable.

The CC and SC multiturn masters are checking the following protocol error conditions. If violated, the status bit ESSI (see Table 80, page 60) is set.

Protocol checks (x = 1, 2):

1. MIx line is 1, right before the first MOx falling edge
2. MIx line is 0, right after the last MOx rising edge (Stop-Zero)

If the first protocol check is not valid (MIx=0) no clock pulse at MOx is generated

The first protocol check verifies, that the previous read frame was correctly finished and thus detects if MI1 or MI2 is stuck-at-zero. To verify the correct timeout and protocol length and to detect if MI1 or MI2 is stuck--at-one, the second check is used.

Multiturn Configuration: Control Channel
The multiturn master interface of the Control Channel can be configured with pins CFG10/CFG11 (see Table 60).

Control Channel		
Pins CFG11/10: MT Configuration		
CFG11/10	MT Data	Input Data
No Multiturn		
00	0 bit	No multiturn
Synced mode (single binary coded word)		
01	12 bit	12-bit data + 3-bit sync + 1-bit error
10	16 bit	16-bit data + 3-bit sync + 1-bit error
iC-MV Mode (parts of words, binary coded)		
x0	12 bit	3 * (4-bit data + 3-bit sync) + 3-bit error
x1	16 bit	4 * (4-bit data + 3-bit sync) + 4-bit error
iC-LV Mode (parts of words, Gray coded)		
0x	12 bit	3 * (4-bit data + 1-bit sync + 1-bit error)
1x	16 bit	4 * (4-bit data + 1-bit sync + 1-bit error)
Internal 24-bit revolution counter		
11[1]	24 bit	Battery required
xx[1]	24 bit	No battery required
Note	x = pin open or set to 2.5V (=VIO1/2) [1] Index-Pulse output at MO1 (see DIGITAL INDEX PULSE (CC))	

Table 60: Pin-Configured Multiturn Operating Mode

The state of the CFG10 and CFG11 pins is latched at power-on and the resulting multiturn configuration is saved in parameters MODE_MT_CC, SBL_MT_CC and EBL_MT_CC.

See Table 17 for a summary of the control channel features configured with the CFG10 and CFG11 pins.

When reading data from an external multiturn sensor, pin MO1 is the clock output and MI1 the data input of the Control Channel. These pins are supplied by VIO1. Refer to Figure 42 for an example of the line signals for the Synced Mode, iC-MV Mode and iC-LV Mode.

A temporary change of the MT mode, the synchronization settings, and the error bit length is possible. A change has an effect only after sending the **RESET** command.

Table 61 summarizes all possible MT modes for iC-RZ and their data length dependencies on SBL_MT_CC and EBL_MT_CC. The values selectable with pins CFG11/10 are marked in blue.

Control Channel		
MODE_MT_CC(3:0) Addr. 0x10; bit 3:0		
Code	MT Data	Input Data
No Multiturn		
0x6	0 bit	no multiturn
Synced Mode (single binary coded word)		
0x0	12 bit	12-bit + SBL_MT_CC + EBL_MT_CC
0x3	16 bit	16-bit + SBL_MT_CC + EBL_MT_CC
iC-MV Mode (parts of words, binary coded)		
0x1	12 bit	3* **(4-bit + SBL_MT_CC)** + 3* EBL_MT_CC
0x4	16 bit	4* **(4-bit + SBL_MT_CC)** + 4* EBL_MT_CC
iC-LV Mode (parts of words, binary coded)		
0x2	12 bit	3* **(4-bit + SBL_MT_CC + EBL_MT_CC)**
0x5	16 bit	4* **(4-bit + SBL_MT_CC + EBL_MT_CC)**
Synced Mode (single Gray coded word)		
0x8	12 bit	12-bit + SBL_MT_CC + EBL_MT_CC
0xB	16 bit	16-bit + SBL_MT_CC + EBL_MT_CC
iC-MV Mode (parts of words, Gray coded)		
0x9	12 bit	3* **(4-bit + SBL_MT_CC)** + 3* EBL_MT_CC
0xC	16 bit	4* **(4-bit + SBL_MT_CC)** + 4* EBL_MT_CC
iC-LV Mode (parts of words, Gray coded)		
0xA	12 bit	3* **(4-bit + SBL_MT_CC + EBL_MT_CC)**
0xD	16 bit	4* **(4-bit + SBL_MT_CC + EBL_MT_CC)**
Internal 24-bit revolution counter		
0xE	24 bit	internal revolution counter battery-buffered
0xF	24 bit	internal revolution counter
Adjustment Mode		
0x7	32 bit	Adjustment mode (raw MT data, no sync to ST)
Note	Settings marked blue are available by pin configuration (for a detailed mapping see Table 17). The reset value depends on the pins CFG11/10.	

Table 61: Multiturn Operating Mode

Parameter SBL_MT_SC configures the number of synchronization bits and thus the possible synchronization range. The function of SBL_MT_CC in iC-LV Mode differs from the other modes (see Table 63).

Control Channel		
For all MODE_MT_CC except iC-LV mode		
SBL_MT_CC(1:0) Addr. 0x10; bit 7:6		
Value	Sync. Bits	Sync. Range
00	1	±90 °m
01	2	±135 °m
10	3	±157.5 °m
11	4	±168.75 °m
Note	°m = with reference to one mechanical revolution Settings marked blue are available by pin configuration at CFG11 and CFG10. The reset value depends on the pins CFG11/10.	

Table 62: MT Synchronization Bits: iC-MV Mode and Synced Mode

Control Channel		
Only iC-LV Mode		
SBL_MT_CC(1:0) Addr. 0x10; bit 7:6		
Value	Sync. Bits	Sync. Range
00	1	Sync-slave and sync-master aligned (mounting offset = 0°m) => +/- 1 synchronization
01	1	Sync-slave pre-positioned by 90°m with respect to sync-master => - 1 synchronization
10	1	Sync-slave post-positioned by 90°m with respect to sync-master => + 1 synchronization
11	1	Sync-slave and sync-master aligned (mounting offset = 0°m) => +/- 1 synchronization
Note	Settings marked blue are available by pin configuration at CFG11 and CFG10. The reset value depends on the pins CFG11/10. This setting rules the synchronization from gear to gear stage, only between the iC-LV's. The MT to ST synchronization is not covered.	

Table 63: MT Synchronization Bits: iC-LV Mode

In iC-MV Mode and iC-LV Mode, parameter EBL_MT_CC configures the number of error bits related to each MT part of words. In the Synced Mode, EBL_MT_CC configures the overall error bit data length.

Control Channel		
EBL_MT_CC(1:0) Addr. 0x10; bit 5:4		
Code	iC-LV/MV Mode (parts of words)	Synced Mode
00	0	0
01	1 (active low)	1 (active low)
10	not allowed*	2 (active low)
11	not allowed*	3 (active low) for 12 bit MT data or 4 (active low) for 16 bit MT data
Note	Settings marked blue are available by pin configuration at CFG11 and CFG10. The reset value depends on the pins CFG11/10. *) An incorrect configuration of the error bit length EBL_MT_CC in iC-MV Mode or iC-LV Mode will be reported by the status bit ESSI.	

Table 64: MT Error Bits

Multiturn Configuration: Safety Channel
The multiturn master interface of the Safety Channel can be configured with parameters MODE_MT_SC (see Table 65), SBL_MT_SC (see Table 66) and EBL_MT_SC (see Table 68).

After power-on, the multiturn parameters are only effective if the CRC_CFG is valid, i.e. if reading from the EEPROM was successful, or the **RESET** command was executed.

When reading data from an external multiturn sensor, pin MO2 is the clock output and MI2 the data input of the Safety Channel. Refer to Figure 42 for an example of the line signals for the Synced Mode, iC-MV Mode, and iC-LV Mode.

Safety Channel		
MODE_MT_SC(3:0)	Addr. 0x10; bit 3:0	
Code	MT data	Input Data
No Multiturn		
0x6	0 bit	No multiturn
Synced Mode (one binary word)		
0x0	12 bit	12-bit + SBL_MT_SC + EBL_MT_SC
0x3	16 bit	16-bit + SBL_MT_SC + EBL_MT_SC
iC-MV Mode (parts of words, binary)		
0x1	12 bit	3* **(4-bit + SBL_MT_SC)** + 3* EBL_MT_SC
0x4	16 bit	4* **(4-bit + SBL_MT_SC)** + 4* EBL_MT_SC
iC-LV Mode (parts of words, binary)		
0x2	12 bit	3* **(4-bit + SBL_MT_SC + EBL_MT_SC)**
0x5	16 bit	4* **(4-bit + SBL_MT_SC + EBL_MT_SC)**
Synced Mode (one gray word)		
0x8	12 bit	12-bit + SBL_MT_SC + EBL_MT_SC
0xB	16 bit	16-bit + SBL_MT_SC + EBL_MT_SC
iC-MV Mode (parts of words, gray)		
0x9	12 bit	3* **(4-bit + SBL_MT_SC)** + 3* EBL_MT_SC
0xC	16 bit	4* **(4-bit + SBL_MT_SC)** + 4* EBL_MT_SC
iC-LV Mode (parts of words, gray)		
0xA	12 bit	3* **(4-bit + SBL_MT_SC + EBL_MT_SC)**
0xD	16 bit	4* **(4-bit + SBL_MT_SC + EBL_MT_SC)**
Internal 24-bit revolution counter		
0xE	24 bit	internal revolution counter battery-buffered
0xF	24 bit	internal revolution counter
Adjustment Mode		
0x7	32 bit	Adjustment Mode (raw MT data, no sync to ST)
Note	Reset value 0x06: No multiturn	

Table 65: Multiturn Operating Mode

Parameter SBL_MT_SC configures the number of synchronization bits and thus the possible synchronization range. The function of SBL_MT_SC in iC-LV Mode differs from the other modes (see Table 67).

Safety Channel		
For all MODE_MT_SC except iC-LV Mode		
SBL_MT_SC(1:0)	Addr. 0x10; bit 7:6	
Code	Sync. Bits	Sync. Range
00	1	±90 °m (Default)
01	2	±135 °m
10	3	±157.5 °m
11	4	±168.75 °m
Note	°m = with reference to one mechanical revolution.	

Table 66: MT Synchronization Bits: iC-MV Mode and Synced Mode

Safety Channel		
Only iC-LV Mode		
SBL_MT_SC(1:0)	Addr. 0x10; bit 7:6	
Value	Sync. Bits	Sync. Range
00	1	Sync-slave and sync-master aligned (mounting offset = 0°m) => +/- 1 synchronization
01	1	Sync-slave pre-positioned by 90°m wrt sync-master => - 1 synchronization
10	1	Sync-slave post-positioned by 90°m wrt sync-master => + 1 synchronization
11	1	Sync-slave and sync-master aligned (mounting offset = 0°m) => +/- 1 synchronization
Notes	This setting rules the synchronization from gear to gear stage, only between the iC-LV's. The MT to ST synchronization is not covered.	

Table 67: MT Synchronization Bits: iC-LV Mode

In iC-MV Mode and iC-LV Mode, parameter EBL_MT_SC configures the number of error bits related to each MT part of words. In the Synced Mode, EBL_MT_SC configures the overall error bit data length.

Safety Channel		
EBL_MT_SC(1:0)	Addr. 0x10; bit 5:4	
Code	iC-LV/MV Mode (parts of words)	Synced Mode
00	0	0
01	1 (active low)	1 (active low)
10	Not allowed*	2 (active low)
11	Not allowed*	3 (active low) for 12 bit MT data or 4 (active low) for 16 bit MT data
Note	An incorrect configuration of the error bit length EBL_MT in iC-MV or iC-LV Mode is reported on the status bit ESSI.	

Table 68: MT Error Bits

MT Adjustment Mode

The adjustment mode can be used to get the raw position information from the MT slave(s). To read out the raw position information, the BiSS protocol must be selected with IF_MODE = 0x0 or 0x1. The read out data length of the MT interface is changed according to Table 69 and no synchronization with the ST value is performed.

This enables the user to read the raw data from individual multiturn sensors of a multiturn gear box, e.g. with iC-MV, and to calculate the correct offset values which have to be programmed for each multiturn sensor.

Control Channel		
MODE_MT_CC(3:0)	Addr. 0x10; bit 3:0	
Safety Channel		
MODE_MT_SC(3:0)	Addr. 0x10; bit 3:0	
Code	MT Ext. Data Length	DL_MT
0x7	32 bit	Forced to 32 bit
Note	After activation or deactivation of the adjustment mode, the command RESET must be executed for each channel (CMD_CC/CMD_SC = 0x11) .	

Table 69: Configuration MT SSI format

For adjustment between ST and MT, use the adjustment mode with slow rotation speed only. This restriction applies because the MT data is latched with the normal MT readout cycle (see Op. Req. I206).

Internal 24-bit Revolution Counter

Key features:

- Utilization of the random track for revolution counting
- 24-bit revolution counter
- Integrated supply switch at VDDM1 / VDDM2
- Dedicated LED control pin (LED1 / LED2)

Reset Value Revolution Counter

The internal revolution counter is reset

Control Channel		
Safety Channel		
ST Position	ST Value*	MT Value
≤180° m >180° m	0 - 512 513 - 1023	0 -1 (= max. value)
	*only 10-bit random value is used	

Table 70: MT value after power-on

Internal Revolution Counter (non-battery powered)

The absolute value scanned from the random track is used to control the internal revolution counter.

In this mode the status messages $EPDN_L$ and ERL_L are not used. So after power-on, as soon as a correct ST position can be evaluated, the system is in an error-free condition (nE/nW bits are high).

Internal Revolution Counter (battery powered)

The Control Channel and the Safety Channel offer the possibility to maintain the respective internal revolution counter and to continue counting if the main power supply VDDA1/VDD1 (CC) or VDDA2/VDD2 (SC) has failed. To achieve this, the power supply of the MT circuit of the respective channel can switch to a battery supply connected to pin VDDM1 (CC), respectively to VDDM2 (SC).

In the following, the supply voltage switching (VDDA1/VDD1 → VDDM1) and the LED flashing (output LED1) of the battery-buffered MT of the Control Channel is described. The same applies to the Safety Channel which uses the pins VDDA2,VDD2, VDDM2 and LED2 for this purpose.

If the main supply voltage on VDDA1 drops below the threshold voltage Vt()lo with respect to VDDM1, the internal circuit will be powered by VDDM1 instead of VDDA1 (see Elec. Char. V03).

In this battery-buffered mode, the LED will be flashed using pin LED1 (provides an unregulated constant current over a certain duration, see Elec. Char. V08) in order to read the singleturn position from the code disc and, if necessary, to update the internal revolution counter. Depending on the power source used, e.g. a 3.6 V battery with 0.55 Ah capacity, the device can operate for several years without losing the position information.

If the battery-buffered MT feature of the Control Channel is not used, VDDM1 must be connected to VDDA1 and LED1 to GND1.

If the battery-buffered MT feature of the Safety Channel is not used, VDDM2 must be connected to VDDA2 and LED2 to GND2.

LED flashing is limited to a single output, either using LED1 or LED2, not both at a time.

An external bootstrap circuit is required if a blue LED is to be powered by a 3.6 V battery.

To allow power savings, the LED flashing and multiturn update interval for battery operation can be adapted to the encoder's application requirements using TSLEEP_x (x = CC, SC). This battery-buffered register configures the maximum flashing interval of position evaluation, and determines the maximum speed and acceleration which can be tracked during a power failure.

The minimum battery load is obtained at standstill, depending on f_{Flash}, and increases with movements when STEP automatically highers the update rate via the position clock $f_{mc,min}$.

The LED flashing frequency is gradually increased (STEP: 0→1→2→3) if a change of more than 45° is detected between measurements. If a change of less than 11° is measured, the frequency is gradually reduced (STEP: 3→2→1→0).

Control Channel	
Safety Channel	
STEP	Min. Internal Position Clock $f_{mc,min}$
0	18 kHz
1	39 kHz
2	95 kHz
3	190 kHz

Table 71: Flashing Frequency Stepping

The following equation calculates the LED flashing frequency:

$$f_{Flash} = \frac{f_{mc,min}}{TSLEEP\_x \cdot 8 + 7} \quad (1)$$

An adjustment to the required maximum rotational speed and acceleration is made by TSLEEP_x to achieve maximum battery life. The maximum rotational speed is calculated in [rpm] as follows:

$$\omega_{max} = \frac{f_{mc,min} \cdot 60}{2 \cdot (TSLEEP\_x \cdot 8 + 7)} \quad (2)$$

And the maximum acceleration (in rad/s^2) is:

$$\alpha_{max} = 2 \cdot \pi \cdot f_{Flash}^2 \quad (3)$$

Table 72 provides some examples for different values of TSLEEP_x, calculated with the minimum position clock of Table 71. It must be considered that for the values of f_{Flash} it is assumed that the encoder shaft is stationary (STEP = 0), that f_{Flash} for the maximum rotational speed ω_{max} has increased (STEP = 3), and that the encoder shaft is accelerated from standstill (STEP = 0).

Control Channel			
TSLEEP_CC(7:0) Addr. 0x11; bit 7:0			
Safety Channel			
TSLEEP_SC(7:0) Addr. 0x11; bit 7:0			
Code	Max. $1/f_{Flash}$ [ms]	Max. Speed [rpm]	Max. Acceleration [rad/s^2]
0x00	0.39	814286	41545960
...			
0x0A	4.83	65517	268959
...			
0x64	44.83	7063	3126
...			
0xFF	113.72	2785	486
Note	The reset value is 0xFF until the first configuration of the battery-buffered value, or if no battery is connected to VDDM1 resp. VDDM2.		

Table 72: Flashing Interval vs. Speed/Acceleration

Check TSLEEP_SC Value (SC)
After startup, when using an EEPROM and CRC_CFG is correct, the battery-buffered TSLEEP_SC value is compared with the TSLEEP_SC value read from the EEPROM.

In case of a mismatch between the two, the battery-buffered TSLEEP_SC is updated with the EEPROM value and status bit ETSL is set (see chapter STARTUP PROCESS).

For the continuous CRC check during normal operation the battery-buffered TSLEEP_SC value is taken.

Using BLEED/LOAD
The register bit LOAD_x enables the charging of an external capacitor via the pin VDDM1 (CC) / VDDM2 (SC) in the main power mode.

The principle circuit diagram is shown in Figure 43.

Control Channel	
LOAD_CC Addr. 0x30; bit 5	
Safety Channel	
LOAD_SC Addr. 0x30; bit 5	
Code	Description
0	Capacitor load current out of VDDM1 (CC) / VDDM2 (SC) disabled
1	Capacitor load current[1] out of VDDM1 (CC) / VDDM2 (SC) enabled
Note	[1]see Elec. Char. V14

Table 73: Capacitor Charge Current

The register bit BLEED_x enables discharging of the battery connected to pin VDDM1 (CC) / VDDM2 (SC) while main power is supplied, in order to "wake up" the battery.

This may be necessary depending on the battery used if the encoder has not been in battery-buffered mode for a long time. Please refer to the specification of the battery used in your application for further information.

Control Channel	
BLEED_CC	Addr. 0x30; bit 6
Safety Channel	
BLEED_SC	Addr. 0x30; bit 6
Code	Description
0	Discharge current in VDDM1 (CC) / VDDM2 (SC) disabled
1	Discharge current[1] in VDDM1 (CC) / VDDM2 (SC) enabled
Note	[1]see Elec. Char. V13

Table 74: Battery Discharge Current

LOAD_x and BLEED_x shall not be enabled at the same time.

Notice on Battery Usage

Note that the iC-RZ will operate in battery-buffered mode when a battery is connected during the shipment or storage. This can lead to a reduced lifetime of the battery, especially if the system is operated without a code disc.

If an external battery is used in combination with the iC-RZ, an additional RC circuit is recommended (refer to Figure 43).

This RC filter structure smoothes the pulsed current drain. The battery experiences a more continuous current drain that is closer to the average current.

Furthermore, the resistor R1 limits the charge current in case of a supply switch malfunction in the iC-RZ.

The resistor value must be suitable to limit the charge current to the desired limit in all possible error cases.

Additionally, the voltage drop during normal operation should be minimal. Capacitor C1 must be selected so that it can supply the energy for a single flash pulse to LED1 (CC) / LED2 (SC).

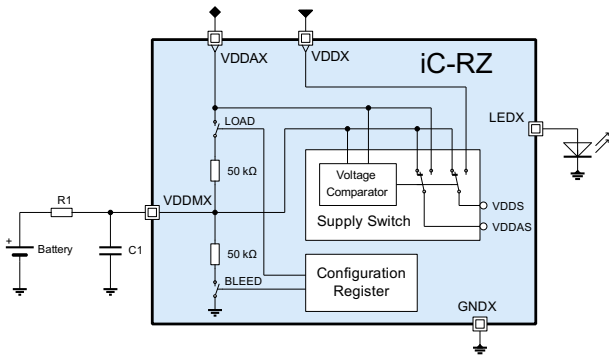


Figure 43: Circuit example for iC-RZ battery supply

DIGITAL INDEX PULSE (CC)

The Control Channel can be configured to generate an index pulse (Z index) at the output pin MO1.

Control Channel	
Index Pulse output configured with CFG10/11	
CFG10/11	Z index pulse output
11 xx[1] else	at pin MO1 at pin MO1 no index pulse
Note	[1] x = pin open or set to 2.5V (=VIO1/2) See Table 17 for a summary of Control Channel features configured with the CFG10 and CFG11 pins

Table 75: Z index pulse output

The random track photodiodes are evaluated and the resulting absolute position is taken to generate the Z index pulse. The generation of the index pulse is independent of the auxiliary sine/cosine signals at pins PSIN, NSIN, PCOS and NCOS.

If the mechanical alignment of iC-RZ is ideal, the Z index pulse rises at a positive zero crossing of the cosine signal (PCOS) and falls at the next positive zero crossing. Hence the pulse width is equal to one period of the cosine signals (see Figure 44).

There is no synchronization to the sine/cosine signals, so the actual phase of the index pulse depends on the mechanical alignment.

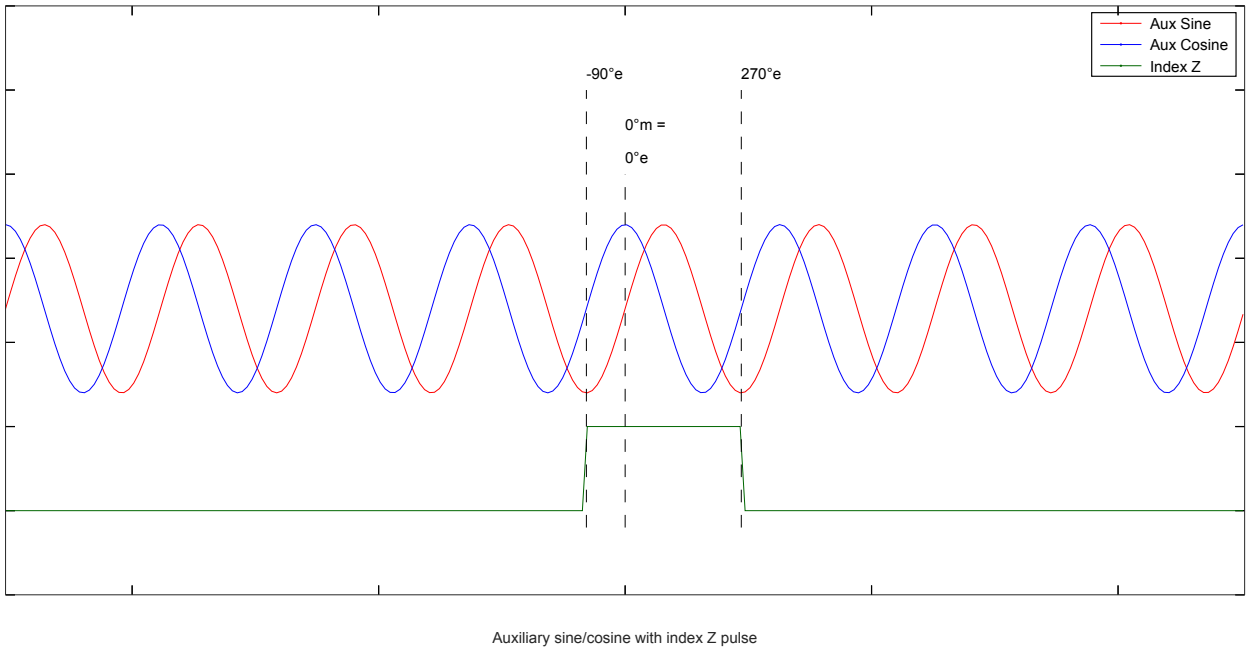


Figure 44: Z index pulse and sine/cosine track
°m = with reference to one mechanical revolution, °e = with reference to one electrical period

TEMPERATURE SENSOR (SC)

The value of the internal digital 8-bit temperature sensor can be read by BiSS or SPI register communication. The 8 bits of data represent a temperature in the range of -64 °C to 191 °C (see Table 76).

Safety Channel	
TEMP(7:0) Addr. 0x73; bit 7:0	
Code	Temperature
0x00	-64 °C
0x01	-63 °C
...	...
0x18	-40 °C
...	...
0x40	0 °C
...	...
0x54	20 °C
...	...
0xA4	100 °C
...	...
0xFF	191 °C

Table 76: Temperature Value

Its offset is calibrated using the parameter OTEMP (see Table 77).

Safety Channel	
OTEMP(5:0) Addr. 0x16; bit 5:0	
Code	Temperature Correction
0x00	0 °C
0x01	1 °C
...	
0x0F	15 °C
0x10	-48 °C
0x11	-47 °C
...	
0x3F	-1 °C

Table 77: Temperature Offset Data

A continuous internal temperature monitoring is possible. A warning and error threshold can be programmed for this purpose. The message is generated if the temperature is higher than the threshold value.

Safety Channel	
TERR(7:0) Addr. 0x18; bit 7:0	
TWARN(7:0) Addr. 0x17; bit 7:0	
Code	Temperature
0x00	-64 °C
0x01	-63 °C
...	...
0x18	-40 °C
...	...
0x40	0 °C
...	...
0xA4	100 °C
...	...
0xFF	191 °C

Table 78: Temperature Error/Warning Threshold

To switch from a overtemperature warning to an undertemperature warning, the polarity of the warning message can be selected.

Safety Channel	
TWARNSW Addr. 0x16; bit 6	
Code	Temp
0	Overtemperature warning
1	Undertemperature warning

Table 79: Undertemperature Warning Selection

DIAGNOSTICS CC

The iC-RZ Control Channel provides various diagnostic features using an error/warning bit and several status registers. The status information can be observed using the following methods:

- Status registers (addr. 0x70 to 0x72)
- nE/nW bits in BiSS protocol
- Output pin ADIOK1

Amplifier Limit Monitor
All optical amplifiers in the Control Channel, which are involved in the position generation, contain limit monitors to detect an output saturation (upper limit reached). Amplifier errors EAMPA, EAMP24, EAMPR are visible in STATUS2_CC. An incorrect operating point of the random code evaluation is messaged by ERL, also visible in STATUS2_CC.

Sin/Cos DC Monitor
The DC level of the 1024 CPR sin/cos signals is observed by an appropriate monitoring circuit, in order to detect a low LED illumination. In this case, status bit EDC24 is set (STATUS2_CC).

Interpolator Plausibility Check
The comparator code of the sine-to-digital converter is monitored. If the code is not feasible, because of erroneous sine/cosine signals or comparator errors, status bit EINT is set (STATUS1_CC). This check is triggered by a position data request only.
Note: If the 1024 sin/cos track signals get a too low amplitude, this can lead to an invalid converter code and thus the status bit EINT is set. (see Elec. Char. 806).

PRC Plausibility Check
The singleturn position of the 10-bit random track is generated synchronously with the internal system clock. With each clock pulse, the newly generated data is compared with the previous value. The comparison is valid within 0, +1 or -1 difference. In addition, the synchronicity of the 10-bit singleturn position to the interpolator is continuously monitored. If one of the diagnostic functions fails, STATUS1_CC bit EST will be set.

Multiturn Interface Protocol

The multiturn interface checks the following conditions while reading the external MT data:

1. MI1 line is 1, right before the first MO1 clock pulse. It verifies that the previous frame was correctly finished and detects if MI1 is stuck-at-zero.
2. MI1 line is 0, right after the last MO1 clock pulse (Stop-Zero). Verifies correct timeout and protocol length. Detects if MI1 is stuck-at-one.

If these conditions are not met, STATUS1_CC bit ESSI is set.

The error bits of the multiturn protocol are mapped to EB3..0 in STATUS1_CC (1 = error active).

Multiturn Plausibility Check
The incoming data from the multiturn interface is compared with its previous data. The comparison is valid within 0, +1 or -1 difference. In addition, the synchronicity of the multiturn position to the 10-bit singleturn position is continuously monitored. If one of the diagnostic functions fails, STATUS1_CC bit ERC is set.

24-bit Revolution Counter
If the internal 24-bit revolution counter is used to count the revolutions (see chapter MULTITURN FUNCTIONS), a reset of the counter can be seen with $EPDN_L$ status bit in the STATUS2_CPW. An erroneous evaluation of the random code track can be seen with ERL_L.

If the battery-buffered revolution counter is used, the status bits $EPDN_L$ and ERL_L are battery-buffered (VDDM1) and evaluated at power-on. In supplied mode, only the ERL_L is used to detect an erroneous revolution counter. If enabled with EMASK_CC, the latched status information is used for the BiSS nE bit. To reset the status information of these bits, the command **SCLEAR** has to be executed.

Configuration
The configuration pins CFG11/CFG10 are sampled on startup and the Control Channel is configured according to Table 17. During operation, the configuration pins are checked against the startup configuration. If the current logic levels of the configuration pins differ from the logic levels on startup, status bit ECP is set.

The configuration is write-protected after startup. The write protection can be disabled using the CMD_CC = **RPL_RESET** and re-activated with CMD_CC = **RPL_SET_RO**. The current protection status is shown by status bit ENRPCFG in STATUS3_CC.

Internal Test Modes

If an internal test mode (TEST_CC≠0x00) is activated, it is reported with bit TEST, STATUS3_CC.

Status Registers

The following tables describe the status register mapping. For the status bits marked with $_L$ the relevant bit will be set in case of an error and maintained until the command **SCLEAR** is executed.

Control Channel		
STATUS1_CC	Addr. 0x70; bit 7:0	
Bit	Name	Function
7	$EB3_L$	MT interface error bit 3
6	$EB2_L$	MT interface error bit 2
5	$EB1_L$	MT interface error bit 1
4	$EB0_L$	MT interface error bit 0
3	$ESSI_L$	MT SSI protocol error
2	ERC_L	RC error
1	EST_L	ST error (random)
0	$EINT_L$	Converter code check error
Note	$_L$ = latched information, cleared by command SCLEAR; Error indication logic: 1 = true, 0 = false	

Table 80: Status byte 1: Control Channel

Control Channel		
STATUS2_CC	Addr. 0x71; bit 7:0	
Bit	Name	Function
7	$EDC24_L$	1024 sin/cos track DC level error
6	$ELEDC_L$	LED control error (see LED CONTROL (CC))
5	$EAMPA_L$	Auxiliary sin/cos track amplifier error
4	$EAMP24_L$	1024 sin/cos track amplifier error
3	$EAMPR_L$	Random track amplifier error
2	0	not used
1	$EPDN_L$	Power-down error VDDM1
0	ERL_L	Random logic error
Note	$_L$ = latched information, cleared by command SCLEAR; Error indication logic: 1 = true, 0 = false	

Table 81: Status byte 2: Control Channel

Control Channel		
STATUS3_CC	Addr. 0x72; bit 7:0	
Bit	Name	Function
7	$EMTSYNC_L$	Internal MT sync error
6	$ESTSYNC_L$	Internal ST sync error
5	IFFOR	Interface forced to use BiSS protocol
4	WFOR	Warning forced by command: CMD_CC = FORCE_WRN
3	EFOR	Error forced by command: CMD_CC = FORCE_ERR
2	ENRPCFG	Register protection config.
1	ECP_L	Error CFG11/CFG10 pins
0	TEST	Test mode active (TEST_CC≠0x00)
Note	$_L$ = latched information, cleared by command SCLEAR; Error indication logic: 1 = true, 0 = false	

Table 82: Status byte 3: Control Channel

The different status information of the multiturn part for the BiSS nE/nW bit are summarized in the status information EMT. Initially, the status EMT is defined along with the pin-configured MT configuration from CFG11 and CFG10, and is updated if changes are programmed.

Control Channel		
EMT bit configuration: dependence on pins CFG11/10		
CFG11	CFG10	EMT
0	0	0
0	1	EB3..0 or ESSI or ERC_C
0	x	EB3..0 or ESSI or ERC_C
1	0	EB3..0 or ESSI or ERC_C
1	x	EB3..0 or ESSI or ERC_C
1	1	$EPDN_L$ or ERL_L or ERC_C
x	0	EB3..0 or ESSI or ERC_C
x	1	EB3..0 or ESSI or ERC_C
x	x	ERC_C
Note	x = pin open or set to 2.5V (=VIO1/2) See Table 17 for a summary of Control Channel features configured with the CFG10 and CFG11 pins. $_C$ = captured information for BiSS nE bit, cleared with the next BiSS communication. $_L$ = latched information, cleared by command SCLEAR	

Table 83: EMT generation for nE/nW bit

BiSS Error bit nE

The status information setting the nE bit in the BiSS protocol can be selected using the EMASK_CC register.

Control Channel			
EMASK_CC	Addr. 0x19; bit 7:0		RW
Bit	Name	Default	Masking
7	0	0	not used
6	EMERL	1	ERL
5	EMDC24	1	EDC24
4	EMINT	1	EINT
3	EMLEDC	0	ELEDC
2	EMST	1	EST_C
1	EMMT	1	EMT (see Table 83)
0	EMAMP	1	EAMPA or EAMP24
Note	$_C$ = captured information, cleared with the next BiSS communication. Encoding of bit 7...0: 0 = message disabled, 1 = message enabled		

Table 84: Error Masking

The status information which is active at the current position data request and which is configured with EMASK_CC are used for the nE bit. A reset of the status information is not required. One exception is the status of the Plausibility Check (EST_C and ERC_C, see EMT). The status information EST_C and ERC_C are captured and are reset with the next BiSS communication.

BiSS Warning bit nW

The status information setting the nW bit in the BiSS protocol can be selected using the WMASK_CC and NWRN_ECP registers.

Control Channel			
WMASK_CC	Addr. 0x1A; bit 7:0		RW
Bit	Name	Default	Masking
7	0	0	-
6	WMERL	1	ERL_L
5	WMDC24	1	$EDC24_L$
4	WMINT	1	$EINT_L$
3	WMLEDC	1	$ELEDC_L$
2	WMST	1	EST_L
1	WMMT	1	EMT_L (see Table 83)
0	WMAMP	1	$EAMPA_L$ or $EAMP24_L$
Note	$_L$ = latched information, cleared by command SCLEAR Encoding of bit 7...0: 0 = message disabled, 1 = message enabled		

Table 85: Warning Masking

The messaging of ECP_L on the warning bit can be deactivated with NWRN_ECP.

Control Channel	
NWRN_ECP	Addr. 0x13; bit 0
Code	Description
0	ECP_L messaging on nW enabled
1	ECP_L messaging on nW disabled

Table 86: Warning Bit w/o ECP_L Status

If a latched status message, marked with $_L$, is causing the BiSS nW bit to be set, the command **SCLEAR** must be executed (see Table 98) to reset the BiSS nW bit.

Pin ADIOK1

To signal a valid startup to an external device, the open-drain output pin ADIOK1 can be used. An external pull-up resistor is recommended.

If no MT interface is used, the position can be read by the BiSS interface after a valid ST position is generated. Otherwise, the ADIOK1 pin is set to high after a correct MT SSI communication or after the timeout for reading a correct MT value has expired (see chapter STARTUP PROCESS).

Control Channel	
Pin ADIOK configured with CFG10/11	
CFG10/11	ADIOK1
00	ADIOK = ST position ok
11	ADIOK = ST position ok
xx	ADIOK = ST position ok
else	ADIOK = hi after MT read ok
Note	x = pin open or set to 2.5V (=VIO1/2) See Table 17 for a summary of control channel features configured with the CFG10 and CFG11 pins.

Table 87: ADIOK1 Messaging

DIAGNOSTICS SC

The status of the Safety Channel can be observed using the following methods:

- Status register (addr. 0x70 to 0x72 and 0x74)
- TEMP register (addr. 0x73) see chapter TEMPERATURE SENSOR (SC)
- nE/nW bit in BiSS/EXTSSI and SPI protocol
- Pin NRES2

Amplifier Limit Monitor

All optical amplifiers in the Safety Channel, which are involved in the position generation, contain limit monitors to detect an output saturation (upper limit reached). Amplifier errors EAMP24, EAMPR are reported in STATUS2_SC. An incorrect operating point of the random code evaluation is messaged by ERL, also visible in STATUS2_SC.

Sin/Cos AC Monitor

The amplitudes of the 1024 CPR sin/cos signals are monitored by an internal $\sin^2$ + $\cos^2$ monitor circuit. If the limits for maximum or minimum amplitude are exceeded, status bits EMAX resp. EMIN are set in STATUS2_SC. With parameter AMNR, the monitor limits can be configured to a wide or a narrow range.

Safety Channel	
AMNR	Addr. 0x16; bit 7
Code	Function
0	Wide range
1	Narrow range (recommended setting)
Note	For limits see Elec. Char. A01, A02

Table 88: Amplitude Monitoring Range

Interpolator Plausibility Check

The comparator code of the sine-to-digital converter is monitored. If the code is not feasible, because of erroneous sine/cosine signals or comparator errors, status bit EINT is set in STATUS1_SC. This check is triggered by a position data request only.
Note: If the 1024 sin/cos track signals get a too low amplitude, this can lead to an invalid converter code and thus the status bit EINT is set. (see Elec. Char. 806).

PRC Plausibility Check

The singleturn position of the 10-bit random track is generated synchronously with the internal system clock. With each clock pulse, the newly generated data is compared with the previous value. The comparison is valid within 0, +1 or -1 difference. In addition, the synchronicity of the 10-bit singleturn position to the interpolator is continuously monitored. If one of the diagnostic functions fails, STATUS1_SC bit EST will be set.

Multiturn Interface Protocol

The multiturn interface checks the following conditions while reading the external MT data:

1. MI2 line is 1, right before the first MO2 clock pulse. It verifies that the previous frame was correctly finished and detects if MI2 is stuck-at-zero.
2. MI2 line is 0, right after the last MO2 clock pulse (Stop-Zero). Verifies correct timeout and protocol length. Detects if MI2 is stuck-at-one.

If these conditions are not met, STATUS1_SC bit ESSI is set.

The error bits of the multiturn protocol are mapped to EB3..0 in STATUS1_SC (1 = error active).

Multiturn Plausibility Check

The incoming data from the multiturn interface is compared with its previous data. The comparison is valid within 0, +1 or -1 difference. In addition, the synchronicity of the multiturn position to the 10-bit singleturn position is continuously monitored. If one of the diagnostic functions fails, STATUS1_SC bit ERC is set.

24-bit Revolution Counter

If the internal 24-bit revolution counter is used to count the revolutions (see chapter MULTITURN FUNCTIONS), a reset of the counter can be seen with $EPDN_L$ status bit in the STATUS2_SC. An erroneous evaluation of the random code track can be seen with ERL_L.

If the battery-buffered revolution counter is used, the status bits $EPDN_L$ and ERL_L are battery-buffered (VDDM2) and evaluated at power-on. In supplied mode, only the ERL_L is used to detect an erroneous revolution counter. If enabled with EMASK_SC, the latched status information is used for the BiSS/EXTSSI/SPI nE bit. To reset the status information of these bits, the command **SCLEAR** has to be executed.

Temperature Monitor

The internal temperature sensor can be used to monitor the chip temperature. The temperature value TEMP can be read (see Table 76).

An overtemperature error is signaled by bit ETEMP and an over or undertemperature warning by bit WTEMP (both in STATUS3_SC). For detailed information regarding the temperature sensor see chapter TEMPERATURE SENSOR (SC) page 58.

Configuration
If no EEPROM is detected at startup, status bit NOEPR (STATUS3_SC) is set. I2C communication problems, e.g. no slave acknowledge, are signaled on status bit EI2C (see Table 92).

The internal configuration and output format settings are secured with a CRC. The CRC check is executed automatically at startup after reading the EEPROM, and continuously during normal operation.

During normal operation it is done continuously. An erroneous CRC is reported with status bit ECRC (STATUS3_SC). Status bits ECRC_CFG and ECRC_OFF can be used to identify the configuration area(s) with the incorrect CRC (STATUS4_SC).

A register protection allows to protect the existing configuration from overwriting. The current protection status is shown by status bits ENRPCFG and ENRPOFF in STATUS3_SC.

The battery-buffered configuration value TSLEEP_SC is checked at startup with the value read from EEPROM. If the values are non-identical, the status bit ETSL is set. ETSL can be reset by writing a new TSLEEP_SC value using the serial interface.

For the initial CRC check after startup, the value read from the EEPROM is taken. The battery-buffered TSLEEP_SC value is taken for the continuous CRC check during normal operation.

Internal Test Modes
If an internal test mode (TEST_SC≠0x00) is activated, this is reported on bit TEST and visible in STATUS3_SC.

Status Registers
The following tables describe the status register mapping. For all status bits marked with $_L$, the relevant bits will be set in case of an error and maintained until the command **SCLEAR** is executed (see Table 101).

Safety Channel		
STATUS1_SC	Addr. 0x70; bit 7:0	
Bit	Name	Function
7	$EB3_L$	MT interface error bit 3
6	$EB2_L$	MT interface error bit 2
5	$EB1_L$	MT interface error bit 1
4	$EB0_L$	MT interface error bit 0
3	$ESSI_L$	MT SSI protocol error
2	ERC_L	RC error
1	EST_L	ST error (random)
0	$EINT_L$	Converter code check error
Note	$_L$ = latched information, cleared by command SCLEAR Error indication logic: 1 = true, 0 = false	

Table 89: Status byte 1: Safety Channel

Safety Channel		
STATUS2_SC	Addr. 0x71; bit 7:0	
Bit	Name	Function
7	$EMIN_L$	Minimum amplitude error
6	$EMAX_L$	Maximum amplitude error
5	0	not used
4	$EAMP24_L$	1024 sin/cos track amplifier error
3	$EAMPR_L$	Random track amplifier error
2	0	not used
1	$EPDN_L$	Power-down error VDDM2
0	ERL_L	Random logic error
Note	$_L$ = latched information, cleared by command SCLEAR Error indication logic: 1 = true, 0 = false	

Table 90: Status byte 2: Safety Channel

Safety Channel		
STATUS3_SC	Addr. 0x72; bit 7:0	
Bit	Name	Function
7	NOEPR	No EEPROM
6	ENRPCFG	Register Protection Configuration
5	ENRPOFF	Register Protection Offset
4	$ETEMP_L$	Temperature error
3	$WTEMP_L$	Temperature warning
2	ETSL	TSLEEP value error
1	ECRC	CRC check error
0	TEST	Test mode active (TEST_SC≠0x00)
Note	$_L$ = latched information, cleared by command SCLEAR Error indication logic: 1 = true, 0 = false	

Table 91: Status byte 3: Safety Channel

Safety Channel		
STATUS4_SC	Addr. 0x74; bit 7:0	
Bit	Name	Function
7	$EMTSYNC_L$	Internal MT Sync Error
6	$ESTSYNC_L$	Internal ST Sync Error
5	IFFOR	Interface forced to use BiSS protocol
4	WFOR	Warning forced with command CMD_SC = FORCE_WRN
3	EFOR	Error forced with command CMD_SC = FORCE_ERR
2	$EI2C_L$	Communication error I2C
1	ECRC_OFF	CRC check error offset area
0	ECRC_CFG	CRC check error configuration area
Note	$_L$ = latched information, cleared by command SCLEAR Error indication logic: 1 = true, 0 = false	

Table 92: Status byte 4: Safety Channel

Safety Channel	
EMT bit generation: dependence on MODE_MT_SC	
Value	EMT reports
No multiturn	
0x6	0
Internal revolution counter	
0xE	$EPDN_L$ or ERL_L or ERC[1]
0xF	ERC[1]
MT interface	
else	EB3..0 or ESSI or ERC[1]
Note	[1] Latched or non-latched status information can be selected with ENESTL (see Table 95) $_L$ = latched information, cleared by command SCLEAR Error indication logic: 1 = true, 0 = false MODE_MT_SC see Table 65, page 53

Table 93: EMT generation for nE/nW bit

BiSS, EXTSSI, SPI: Error and Warning bits nE/nW
The status information setting the nE bit in the serial interface protocol can be selected using the EMASK_SC register.

Safety Channel			
EMASK_SC	Addr. 0x19; bit 7:0		RW
Bit	Name	Default	Masking
7	EMTEMP	1	ETEMP
6	EMERL	1	ERL
5	0	0	-
4	EMINT	1	EINT
3	EMCRC	1	ECRC
2	EMST	1	EST[1]
1	EMMT	1	EMT (see Table 93)
0	EMLED	1	EAMP24 or EMAX or EMIN
Note	[1] Latched or non-latched status information can be selected with ENESTL (see Table 95) Bit coding: 0 = message disabled, 1 = message enabled		

Table 94: Error Masking

The status information which is active at the current position data request and which is configured with EMASK_SC are used for the nE bit. A reset of the status information is not required.
An exception is the status of the Plausibility Check (EST and ERC). The used status information can be selected with ENESTL (see Table 95). With ENESTL = 1 the command **SCLEAR** is required to reset the nE bit.

Safety Channel	
ENESTL	Addr. 0x13; bit 0
Value	Function
0	The current, non-latched values of EST and ERC are used
1	The latched values EST_L and ERC_L are used

Table 95: Error Bit on Latched Status

For the nW bit in the BiSS, EXTSSI, and SPI protocol, the triggering status information can be selected using the WMASK_SC register.

Safety Channel			
WMASK_SC	Addr. 0x1A; bit 7:0		RW
Bit	Name	Default	Masking
7	WMTEMP	1	$WTEMP_L$
6	WMERL	1	ERL_L
5	0	0	-
4	WMINT	1	$EINT_L$
3	WMCRC	1	$ECRC_L$
2	WMST	1	EST_L
1	WMMT	1	EMT_L (see Table 93)
0	WMLED	1	$EAMP24_L$ or $EMAX_L$ or $EMIN_L$
Note	$_L$ = latched information, cleared by command SCLEAR Encoding of bit 7...0: 0 = message disabled, 1 = message enabled		

Table 96: Warning Masking

For BiSS, EXTSSI, SPI:
For the nW bit, the latched status information is used. If a latched status is causing the nW bit to be set, the command **SCLEAR** must be executed (see Table 101) to reset the nW bit.

Pin NRES2

Safety Channel	
Pin NRES2	
State	Function
0	Power-off State, VDD2<Vth
1	Power-on State, VDD2>Vth
Note	See Elec. Char. 401, 402

Table 97: NRES2 output during power-on

Power-on and power-off states can be observed at pin NRES2.

After power-on, the NRES2 pin can be used as an input pin to issue the **REBOOT** command. The time that the NRES2 pin must be pulled low for the reset command to be recognized internally is specified by Elec. Char. I06 and I07.

COMMANDS

Depending on the data value written to the command registers, the execution of an implemented command is triggered. The following implemented commands can be used to check the status of the system and to set it back to an error-free state.

Control Channel

For the implemented commands of the Control Channel, register address 0x77 is used.

Control Channel		
CMD_CC	Addr. 0x77; bit 7:0	W[1]
Code	Function	Description
0x10	REBOOT	Reboot iC-RZ Control Channel (new startup see chapter STARTUP PROCESS, page 29)
0x11	RESET	Reset digital part (new startup using internal config. data, see chapter STARTUP PROCESS)
0x20	SCLEAR	Reset all status bits in: - STATUS1_CC - STATUS2_CC - STATUS3_CC
0x21	FORCE_ERR	Force nE bit of serial interface to be set
0x22	UNFORCE_ERR	Release forced nE bit of serial interface
0x23	FORCE_WRN	Force nW bit of serial interface to be set
0x24	UNFORCE_WRN	Release forced nW bit of serial interface
0xA1	RPL_SET_RO	Set configuration register access to read only (see chapter REGISTER ACCESS, page 45)
0xA3	RPL_RESET	Remove write protection for register access (see chapter REGISTER ACCESS, page 45)
0xC0	UNFORCE_IF[2]	Serial interface uses default protocol BiSS
0xC1	FORCE_BISS[2]	Force the serial interface to BiSS protocol
0xE1	CHIP_REV	Returns the CHIP REVISION in the CMD_STAT_CC register
Note	[1] Read returns 0x00 [2] No function	

Table 98: BiSS commands: Control Channel

The **RESET** command restarts the internal position data generation unit for the ST and MT data. No position data is available while the restart of the position data generation unit is in progress. In this case the output position data is set to 0 and the nE/nW bit is active = 0. The position data is available after a successful start up of the position data generation (see chapter STARTUP PROCESS).

REBOOT and **RESET**:
If no ST data can be obtained after restarting the position data generation, e.g. due to an illumination error, the output remains permanently in error state: *position data returns 0 and nE/nW bits are active*.

After executing the **CHIP_REV** command, the chip revision can be read from the register CMD_STAT_CC.

Control Channel	
CMD_STAT_CC	Addr. 0x76; bit 7:0
CMD_CC	Return value
CHIP_REV	CHIP REVISION (see Table 100)
others	0x00

Table 99: Command Status iC-RZ Control Channel

Control Channel	
CHIP REVISION	
Code	Chip revision
0x05	iC-RZ2648 Y Control Channel
0x06	iC-RZ2648 Y1 Control Channel
0x07	iC-RZ2648 Y2 Control Channel
0x15	iC-RZ2624 Y Control Channel
0x16	iC-RZ2624 Y1 Control Channel
0x17	iC-RZ2624 Y2 Control Channel
0x25	iC-RZ4248 Y Control Channel
0x26	iC-RZ4248 Y1 Control Channel
0x27	reserved iC-RZ4248 Y2 Control Channel
0x35	iC-RZ4224 Y Control Channel
0x36	iC-RZ4224 Y1 Control Channel
0x37	reserved iC-RZ4224 Y2 Control Channel

Table 100: Chip Revision iC-RZ Control Channel

Safety Channel

For the implemented commands of the Safety Channel, register address 0x77 is used.

Safety Channel		
CMD_SC	Addr. 0x77; bit 7:0	W[1]
Code	Function	Description
0x10	REBOOT	Reboot iC-RZ Safety Channel (new startup see chapter STARTUP PROCESS, page 29)
0x11	RESET	Reset digital part (new startup using internal config. data, see chapter STARTUP PROCESS)
0x20	SCLEAR	Reset all status bits in: - STATUS1_SC - STATUS2_SC - STATUS3_SC - STATUS4_SC
0x21	FORCE_ERR	Force nE bit of serial interface to be set
0x22	UNFORCE_ERR	Release forced nE bit of serial interface
0x23	FORCE_WRN	Force nW bit of serial interface to be set
0x24	UNFORCE_WRN	Release forced nW bit of serial interface
0xC0	UNFORCE_IF	Serial interface uses default protocol configured with IF_MODE
0xC1	FORCE_BISS	Force the serial interface to BiSS protocol
0xE1	CHIP_REV	Returns the CHIP REVISION in the CMD_STAT_SC register
Note	[1] Read returns 0x00	

Table 101: BiSS/SPI commands: Safety Channel

The **RESET** command restarts the internal position data generation unit for the ST and MT data. No position data is available while the restart of the position data generation unit is in progress. In this case the output position data is set to 0 and the nE/nW bit is active = 0. The position data is available after a successful startup of the position data generation (see chapter STARTUP PROCESS).

REBOOT and **RESET**:
If no ST data can be obtained after restarting the position data generation, e.g. due to an illumination error, the output remains permanently in error state: *position data returns 0 and nE/nW bits are active*.

After executing the **CHIP_REV** command, the chip revision can be read from the register CMD_STAT_SC.

Safety Channel	
CMD_STAT_SC	Addr. 0x76; bit 7:0
CMD_SC	Return value
CHIP_REV	CHIP REVISION (see Table 103)
others	0x00

Table 102: Command Status iC-RZ Safety Channel

Safety Channel	
CHIP REVISION	
Code	Chip revision
0x0D	iC-RZ2648 Y Safety Channel
0x0E	iC-RZ2648 Y1 Safety Channel
0x0F	iC-RZ2648 Y2 Safety Channel
0x1D	iC-RZ2624 Y Safety Channel
0x1E	iC-RZ2624 Y1 Safety Channel
0x1F	iC-RZ2624 Y2 Safety Channel
0x2D	iC-RZ4248 Y Safety Channel
0x2E	iC-RZ4248 Y1 Safety Channel
0x2F	reserved iC-RZ4248 Y2 Safety Channel
0x3D	iC-RZ4224 Y Safety Channel
0x3E	iC-RZ4224 Y1 Safety Channel
0x3F	reserved iC-RZ4224 Y2 Safety Channel

Table 103: Chip Revision iC-RZ Safety Channel

ALIGNMENT

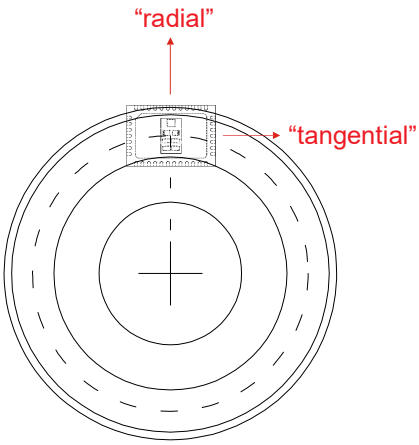


Figure 45: Definition of displacement

For alignment of the sensor to the code disc, internal photodiode signals can be output to pins. To activate the alignment mode the register address 0x30 is used. The definition of radial and tangential displacement is shown in Figure 45.

Control Channel
The internal signals of the Control Channel can only be used to align tangential displacement.
Following diagram shows the signals for an ideal alignment.

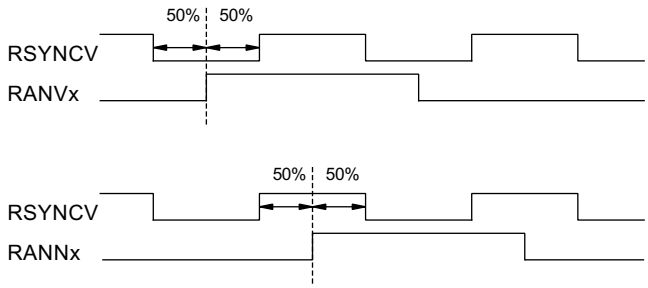


Figure 46: Signals for ideal tangential alignment

The pin assignment during alignment modes is shown in Table 104.

Control Channel						
Pin assignment						
TEST_CC	Description	MO1	MI1	CFG10	CFG11	SLO1
0x00	Normal Mode					
0x03	Sin/cos signals of incremental track with 1024 CPR	PS*	NS*	NC*	PC*	
0x07	PRC track Comparator Signals (tangential alignment)	RANVx		(SEL0***)	RANNx**	RSYNCV
	* Pins must be high impedance for measurement (Internal output impedance $R_{out} \approx 2.5\,k\Omega$) ** CFG11 must be high impedance for measurement of RANNx (see Elec. Char. O01 - O04) *** *SEL0* = 0: SLO1 = SLO, *SEL0* = 1: SLO1 = RSYNCV					

Table 104: Test Mode Selection (CC) and Signal Assignment

In the mode *PRC track Comparator Signals* (TEST_CC = 0x07), the random track test signal to be output is selected using register SELRND_CC.

Control Channel	
SELRND_CC Addr. 0x31; bit 3:0	
Code	Function
0x00	RANV0 / RANN0
...	...
0x09	RANV9 / RANN9
others	not used

Table 105: Random Track Selection (CC)

Safety Channel

The internal signals of the Safety Channel can be used for tangential and radial alignment.

The pin assignment during alignment modes is shown in Table 106. The signals for an ideal tangential alignment are shown in Figure 46.

Safety Channel								
Pin assignment								
TEST_SC	Description	MO2	MI2	SCL2	SDA2	NCS	SDI2	SDO2
0x00	Normal Mode							
0x03	Sin/cos signals of incremental track with 1024 CPR	NC*	PC*			NS*	(SEL0**)	PS*
0x07	PRC track Comparator Signals (tangential alignment)	RSYNCV		RANVx	RANNx			
0x19	Alignment Mode Radial	DJL*	-			-	(SEL0**)	DJH*
	* Pins must be high impedance for measurement (Internal output impedance $R_{out} \approx 2.5\,k\Omega$) **SEL0=0 → SDO2=SDO2, SEL0=1 → Test Signal							

Table 106: Test Mode Selection (SC) and Signal Assignment

In the mode *PRC track Comparator Signals* (TEST_SC = 0x07), the random track test signal to be output is selected using register SELRND_SC.

Safety Channel	
SELRND_SC Addr. 0x31; bit 3:0	
Code	Function
0x00 ... 0x09	RANV0 / RANN0 ... RANV9 / RANN9
others	not used

Table 107: Random Track Selection (SC)

An alignment of the sensor to the code disc in radial direction can be done using test mode *Alignment Mode Radial* (TEST_SC = 0x19) of the Safety Channel. In this test mode the signals of the alignment diodes DJH, DJL (see Figure 47) are output at pins MO2 and SDO2. The radial track position is exact when the voltages of the two pins are more or less equal over one revolution.

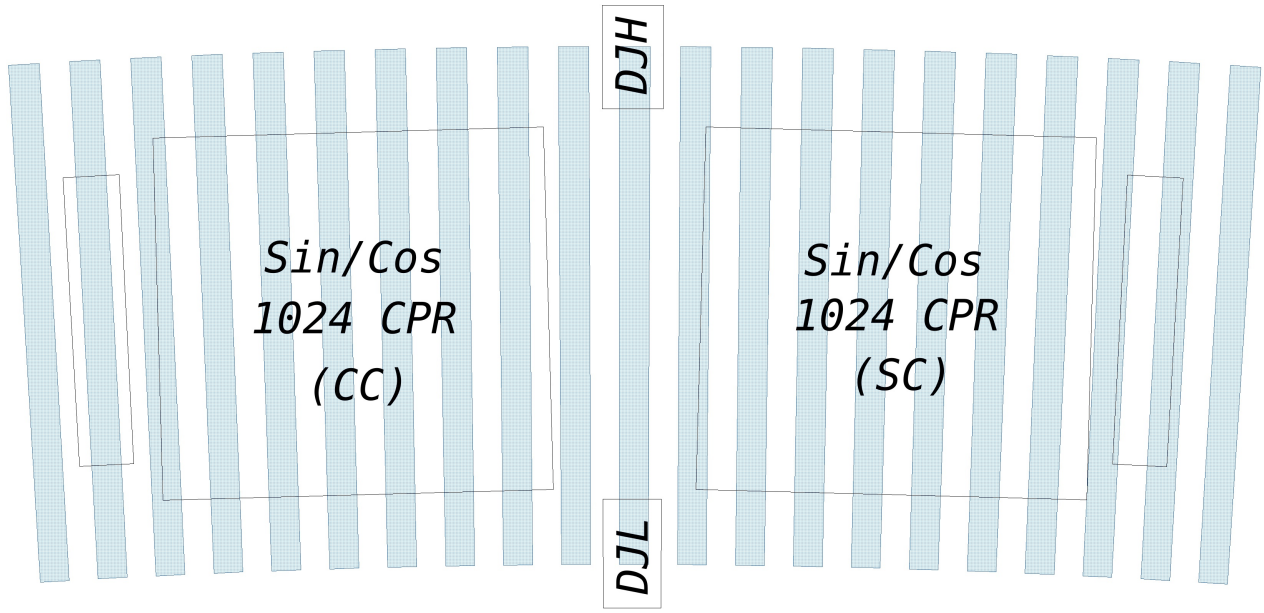


Figure 47: Alignment diodes DJH, DJL for radial alignment

DESIGN REVIEW: Notes On Chip Functions

iC-RZ Y1		
No.	Function, parameter/code	Description and application notes
1	5-bit interpolator: Elec. Char. 806	If the 1024 sin/cos track delivers a signal amplitude of less than 300 mV at startup in standstill (while turning on the LED), this can lead to an invalid converter code and a set status bit EINT. To achieve a signal amplitude of more than 300 mV at startup, using iC-RZ's internal LED control (output LEDC) is recommended.

Table 108: Notes on chip functions regarding iC-RZ, chip revision Y1

iC-RZ Y2		
No.	Function, parameter/code	Description and application notes
		None at time of release.

Table 109: Notes on chip functions regarding iC-RZ, chip revision Y2

REVISION HISTORY

Rel.	Rel. Date[2]	Chapter	Modification	Page
A1	2019-12-09	All	Initial Release	all

Rel.	Rel. Date[2]	Chapter	Modification	Page
B1	2020-11-12	DESCRIPTION	Note box added	2
		PACKAGING INFORMATION	Package dimension figures updated for footnote (pages 6, 8), AOI criteria and figures added (pages 7, 9)	6ff
		ABSOLUTE MAXIMUM RATINGS	Item G006: correction to VDDA+0.3V	10
		ELECTRICAL CHARACTERISTICS	Item 106: correction of condition to EAMPA Item E02: condition and limit added Item 107, K01, L06, O07: added as new items Item O06: correction of formula under conditions	11ff
		OPERATING REQUIREM.: BiSS	Update of BiSS and SSI timing specifications, Figure 2 added	16
		OPERATING REQUIREM.: SPI	Items I112, I113, I115: update of condition Update of listing order	18
		OPERATING REQ. MT Interface	Update of listing order	19
		CONFIG. PARAMETERS	Section added, parameter name changes	22
		PHOTODIODES	Update of description	27
		STARTUP PROCESS	Text corrections, update of Figures 14, 15, 16, 17 Table 14: footnote added Info box added (page 29) Configuration of Control Channel: description added on pin configuration	29ff
		SERIAL I/O INTERFACES	Info text updated, second info on BiSS chain added	35
		BiSS INTERFACE	Tables 25 and 26 added, info box added (page 37)	36ff
		SPI INTERFACE (SC)	Table 35: correction of note for 0x5, Table 36: footnote added, info box added (page 44)	39ff
		SYNCHRONIZATION LOGIC	Description added on multiturn synchronization	48
		MULTITURN FUNCTIONS	Tables 64, 68: notes moved into table Tables 63, 67, 69: notes added Internal Rev. Counter (battery powered): section updated, info and warning notes added on LED1/2 wiring Tables 71, 72: change of title	50ff
		COMMANDS	Update of warning text for CC and SC	66, 67
		ALIGNMENT	Name/description change for mode 0x07	68, 69
		DESIGN REVIEW: Notes On Chip Functions	Note 1 on RZ Y1 added	70

[2] Release Date format: *YYYY-MM-DD*

ORDERING INFORMATION

Type	Package	Order Designation
iC-RZ2624	38-pin optoQFN, 7 mm x 5 mm, thickness 1 mm RoHS compliant	iC-RZ2624 oQFN38-7x5
iC-RZ2648	38-pin optoQFN, 7 mm x 5 mm, thickness 1 mm RoHS compliant	iC-RZ2648 oQFN38-7x5
iC-RZ4224	38-pin optoQFN, 7 mm x 5 mm, thickness 1 mm RoHS compliant	iC-RZ4224 oQFN38-7x5
iC-RZ4248	38-pin optoQFN, 7 mm x 5 mm, thickness 1 mm RoHS compliant	iC-RZ4248 oQFN38-7x5
Code Disc	Glass disc 1.0 mm, suitable for iC-RZ2624	RZ01S 26-1024
Code Disc	Glass disc 1.0 mm, suitable for iC-RZ2648	RZ02S 26-2048
Code Disc	Glass disc 1.0 mm, suitable for iC-RZ4224	RZ05S 42-1024
Code Disc	Glass disc 1.0 mm, suitable for iC-RZ4248	RZ06S 42-2048

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