

iC-MU MAGNETIC OFF-AXIS POSITION ENCODER - POLE WIDTH 1.28MM



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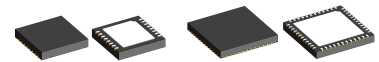
FEATURES

- ◆ Integrated Hall sensors for two-track scanning
- ◆ Hall sensors optimized for 1.28 mm pole width (master track)
- ◆ Signal conditioning for offset, amplitude, and phase
- ◆ Sine/digital real-time conversion with 12-bit resolution (14-bit filtered)
- ◆ 16, 32, or 64 pole pairs per measurement distance
- ◆ 2-track nonius absolute value calculation up to 18, 19 or 20 bits for 16, 32 or 64 master pole pairs
- ◆ Enlargement of measurement distance with second iC-MU
- ◆ Synchronization of external multiturn systems
- ◆ Configuration from an external EEPROM using a multimaster I2C interface
- ◆ Microcontroller-compatible serial interface (SPI, BiSS, SSI)
- ◆ Incremental quadrature signals with an index (ABZ)
- ◆ FlexCount®: scalable resolution from 1 up to 65536 CPR
- ◆ Commutation signals for motors from 1 up to 16 pole pairs (UVW)

APPLICATIONS

- ◆ Rotative absolute encoders
- ◆ Linear absolute scales
- ◆ Singleturn and multiturn encoders
- ◆ Motor feedback encoders
- ◆ BLDC motor commutation
- ◆ Hollow shaft encoder
- ◆ Multi-axis measurement systems

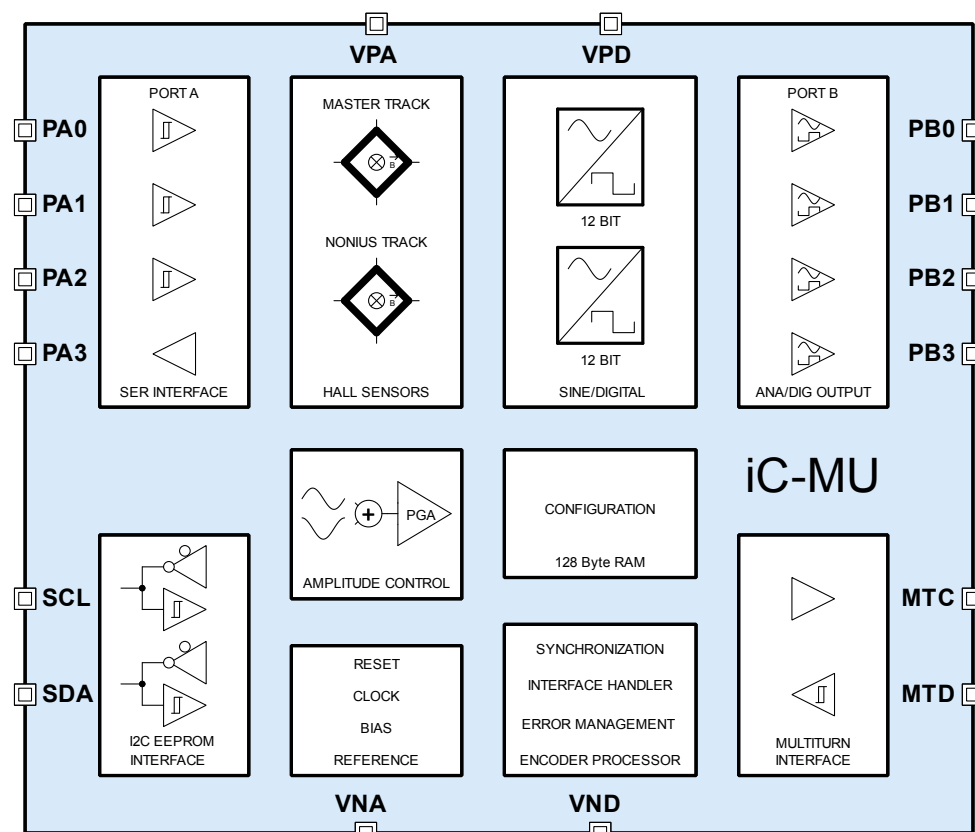
PACKAGES



DFN16
5 mm x 5 mm x 0.9 mm
RoHS compliant

QFN48
7 mm x 7 mm x 0.9 mm
RoHS compliant

BLOCK DIAGRAM



DESCRIPTION

iC-MU is used for magnetic off-axis position definition with integrated Hall sensors. By scanning two separate channels i.e. the master and nonius track the device can log an absolute position within one mechanical revolution. The chip conditions the sensor signals and compensates for typical signal errors.

The internal 12-bit sine/digital converters generate two position words that supply high-precision position data within one sine-period. The integrated nonius calculation engine calculates the absolute position within one mechanical revolution and synchronizes this with the master track position word. Position data can be transmitted serially, incrementally, or analog through two ports in various modes of operation. Commutation signals for brushless DC (BLDC) motors with up to 16 pole pairs are derived from the absolute position and supplied through a 3-pin interface.

During startup the device loads a CRC-protected configuration from an external EEPROM.

After the device has been reset an optional external multiturn is read in an synchronized with the internal position data. During operation the position is cyclically checked.

Note: Parameters defined in the datasheet represent supplier's attentive tests and validations, but - by principle - do not imply any warranty or guarantee as to their accuracy, completeness or correctness under all application conditions. In particular, setup conditions, register settings and power-up have to be thoroughly validated by the user within his specific application environment and requirements (system responsibility).

The performance of iC-MU in application is impacted by system conditions like quality of the magnetic target and its adjustment, field strength and stray fields, temperature and mechanical stress and initial calibration.

iC-MU is realized in two alternative leadless plastic packages DFN16-5x5 and QFN48-7x7. The DFN package occupies less board space and picks up less package stress on board. The double sized QFN package shows slightly lower Rth suited for increased operation temperature and sets higher demands for system conditions.

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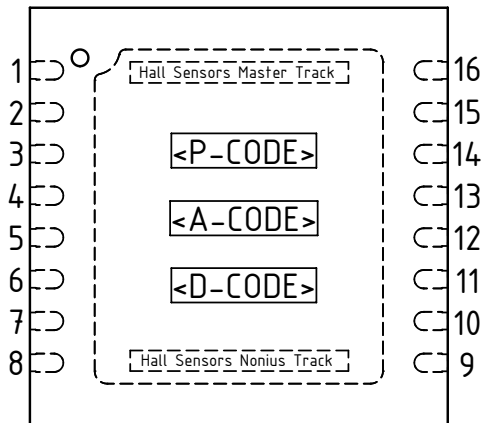


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PACKAGING INFORMATION

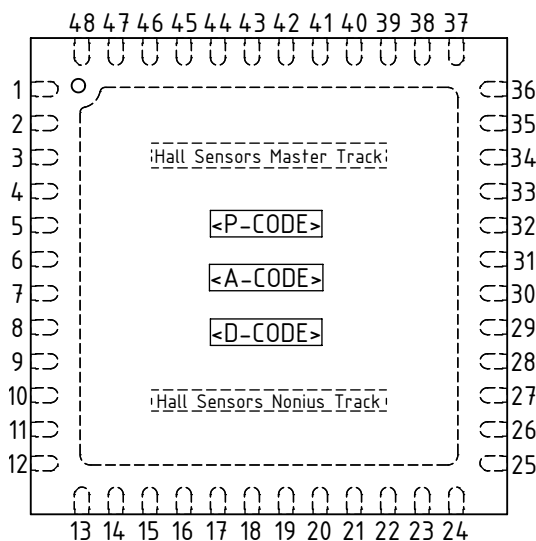
PIN CONFIGURATION DFN16-5x5
(topview)



PIN FUNCTIONS
No. Name Function

| | | |
|----|-------------------|---|
| 1 | SCL | EEPROM interface, clock |
| 2 | SDA | EEPROM interface, data |
| 3 | VPA | +4.5V...+5.5V analog supply voltage |
| 4 | VNA ¹⁾ | Analog Ground |
| 5 | PB0 | Port B, Pin 0: Digital I/O, analog output |
| 6 | PB1 | Port B, Pin 1: Digital I/O, analog output |
| 7 | PB2 | Port B, Pin 2: Digital I/O, analog output |
| 8 | PB3 | Port B, Pin 3: Digital I/O, analog output |
| 9 | PA3 | Port A, Pin 3: Digital I/O |
| 10 | PA2 | Port A, Pin 2: Digital I/O |
| 11 | PA1 | Port A, Pin 1: Digital I/O |
| 12 | PA0 | Port A, Pin 0: Digital I/O |
| 13 | VND ¹⁾ | Digital ground |
| 14 | VPD | +4.5V...+5.5V digital supply voltage |
| 15 | MTD | Multiturn interface, data input |
| 16 | MTC | Multiturn interface, clock output |
| | BP ²⁾ | Backside Pad |

PIN CONFIGURATION QFN48-7x7⁴⁾
(topview)



PIN FUNCTIONS
No. Name Function

| | | |
|-------|-------------------|---|
| 1-2 | n.c. | not connected |
| 3 | SCL | EEPROM interface, clock |
| 4 | SDA | EEPROM interface, data |
| 5 | VPA | +4.5V...+5.5V analog supply voltage |
| 6 | VNA ¹⁾ | Analog Ground |
| 7 | PB0 | Port B, Pin 0: Digital I/O, analog output |
| 8 | PB1 | Port B, Pin 1: Digital I/O, analog output |
| 9 | PB2 | Port B, Pin 2: Digital I/O, analog output |
| 10 | PB3 | Port B, Pin 3: Digital I/O, analog output |
| 11-26 | n.c. | not connected |
| 27 | PA3 | Port A, Pin 3: Digital I/O |
| 28 | PA2 | Port A, Pin 2: Digital I/O |
| 29 | PA1 | Port A, Pin 1: Digital I/O |
| 30 | PA0 | Port A, Pin 0: Digital I/O |
| 31 | VND ¹⁾ | Digital ground |
| 32 | VPD | +4.5V...+5.5V digital supply voltage |
| 33 | MTD | Multiturn interface, data input |
| 34 | MTC | Multiturn interface, clock output |
| 35-48 | n.c. | not connected |
| | BP ²⁾ | Backside Pad |

IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes), <D-CODE> = date code (subject to changes);

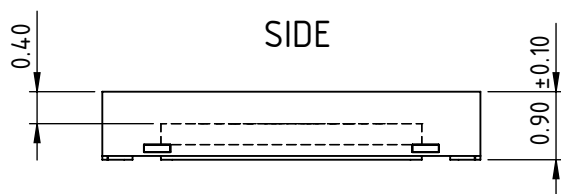
1) Analog (VNA) and digital grounds (VND) have to be connected low ohmic on the PCB.

2) The backside pad on the underside of the package should be appropriately connected to VNA/VND for better heat dissipation (ground plane).

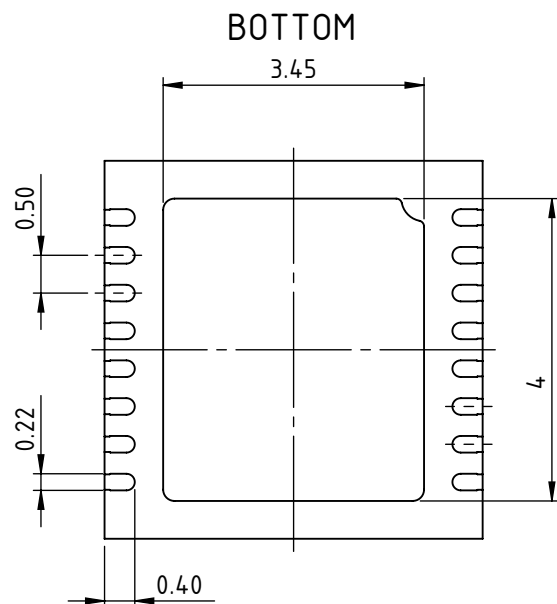
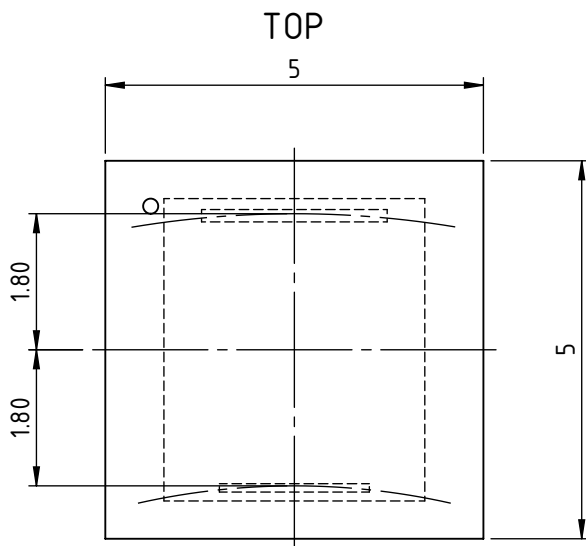
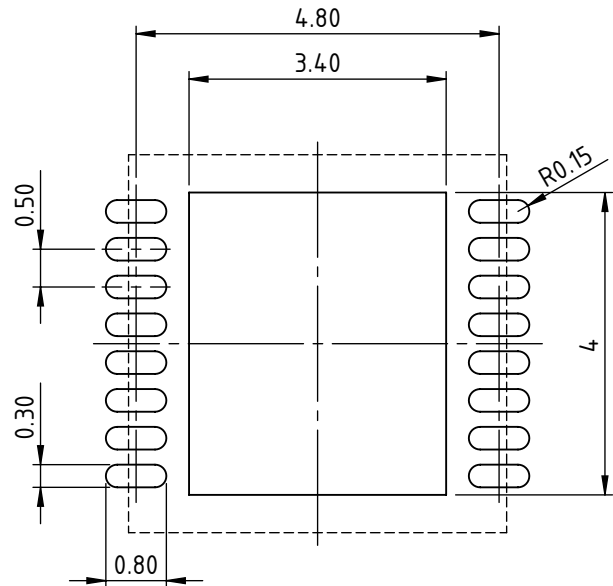
3) Only the Pin 1 mark on the front or reverse is determinative for package orientation (<P-CODE>, <A-CODE>, <D-CODE> are subject to change).

4) Please also see Design Review item No. 7.

PACKAGE DIMENSIONS DFN16-5x5

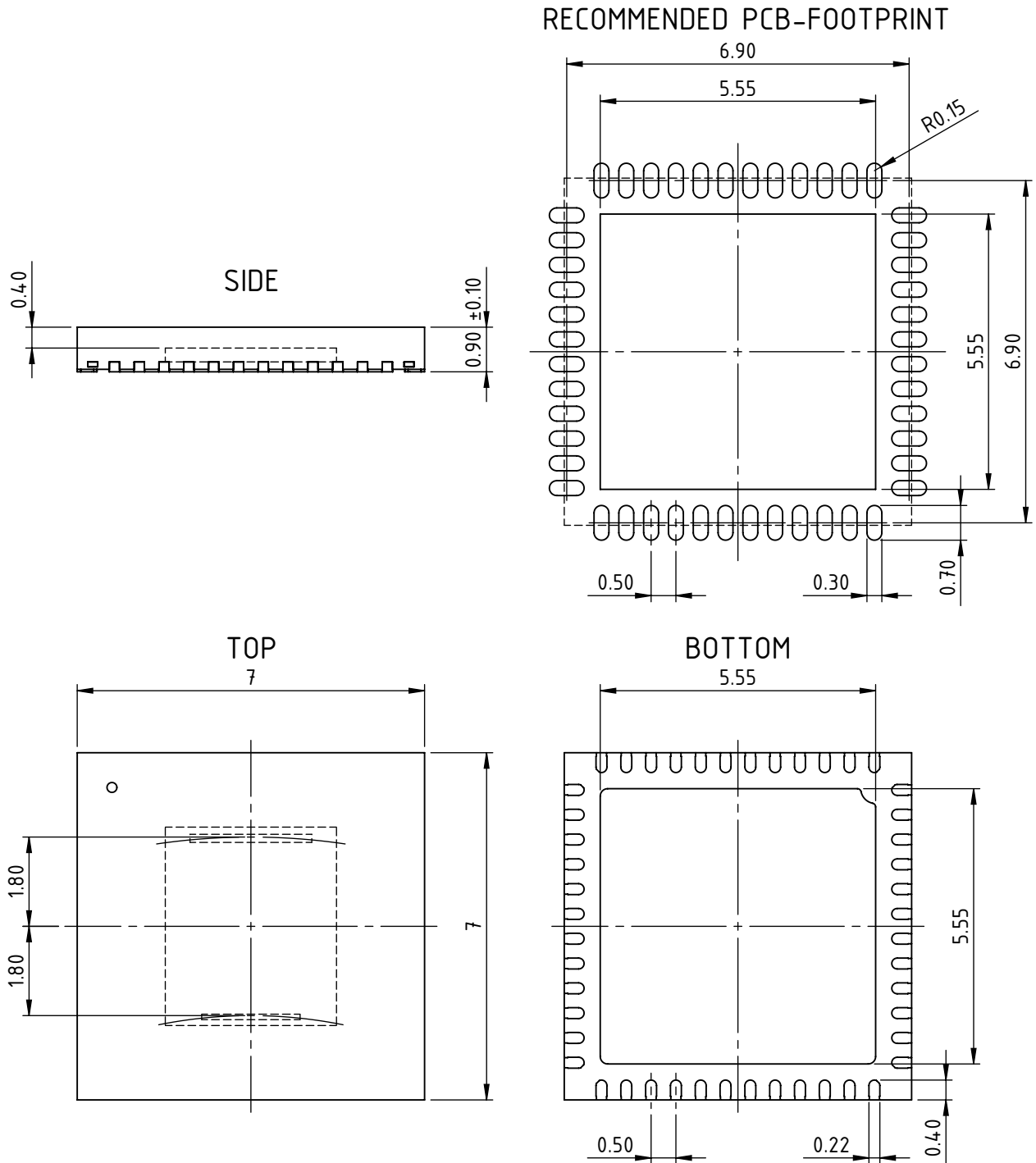


RECOMMENDED PCB-FOOTPRINT



All dimensions given in mm. Tolerances of form and position according to JEDEC MO-229.
Positional tolerance of sensor pattern: $\pm 0.10\text{mm}$ / $\pm 1^\circ$ (with respect to center of backside pad).

PACKAGE DIMENSIONS QFN48-7x7*



All dimensions given in mm. Tolerances of form and position according to JEDEC MO-220.
Positional tolerance of sensor pattern: ±0.10mm / ±1° (with respect to center of backside pad).

drb_qfn48-7x7-2_mu_y2_pack_1, 8:1

*) Please also see Design Review item No. 7.

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ABSOLUTE MAXIMUM RATINGS

Maximum ratings do not constitute permissible operating conditions; functionality is not guaranteed. Exceeding the maximum ratings can damage the device

| Item No. | Symbol | Parameter | Conditions | Min. | | Max. | | Unit |
|----------|--------|--------------------------------|---|-------------|--|-----------|--|--------------|
| | | | | | | | | |
| G001 | V() | Voltage at VPA, VPD | | -0.3 | | 6 | | V |
| G002 | I() | Current in VPA | | -10 | | 20 | | mA |
| G003 | I() | Current in VPD | | -10 | | 100 | | mA |
| G004 | V() | Voltage at all pins except VPD | | -0.3 | | VPD+0.3 | | V |
| G005 | I() | Current in all I/O pins | DC current Pulse width < 10 μ s | -10 -100 | | 10 100 | | mA mA |
| G006 | Vd() | ESD Susceptibility at all pins | HBM, 100 pF discharged through 1.5 k Ω | | | 2 | | kV |
| G007 | Ptot | Permissible Power Dissipation | | | | 400 | | mW |
| G008 | Tj | Chip-Temperature | | -40 | | 150 | | $^{\circ}$ C |
| G009 | Ts | Storage Temperature Range | | -40 | | 150 | | $^{\circ}$ C |

THERMAL DATA

Operating conditions: VPA = VPD = 5V \pm 10%

| Item No. | Symbol | Parameter | Conditions | Min. | | | Max. | | | Unit |
|----------|--------|---|--------------------------------------|------------|------|--|------------|--|------------------------------|------|
| | | | | | Typ. | | | | | |
| T01 | Ta* | Operating Ambient Temperature Range | DFN16-5x5 QFN48-7x7 | -40 -40 | | | 110 115 | | $^{\circ}$ C $^{\circ}$ C | |
| T02 | Rthja | Thermal Resistance Chip to Ambient DFN16 | DFN16-5x5 on PCB according to JESD51 | | 40 | | | | K/W | |
| T03 | Rthja | Thermal Resistance Chip to Ambient QFN48 | QFN48-7x7 on PCB according to JESD51 | | 30 | | | | K/W | |

*) Please also see Design Review item No. 7.

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ELECTRICAL CHARACTERISTICS

Operating conditions: VPD = VPA = 5 V ±10%, Tj = -40...125°C, IBP calibrated to 200 µA, reference is VNA = VND, unless otherwise stated

| Item No. | Symbol | Parameter | Conditions | | | | Unit |
|---|-------------|--|---|--------------|----------------------------|------------------------|-------------------|
| | | | | Min. | Typ. | Max. | |
| Total Device | | | | | | | |
| 101 | V(VPA, VPD) | Permissible Supply Voltage | VPA = VPD | 4.5 | 5 | 5.5 | V |
| 103 | I(VPA) | Analog Supply Current in VPA | | 8 | 13 | 16 | mA |
| 104 | I(VPD) | Digital Supply Current in VPD | | 20 | 40 | 65 | mA |
| 105 | Vc(hi) | Clamp Voltage hi at all pins | Vc(hi) = V() - V(VPD), I() = +1 mA | 0.3 | | 1.6 | V |
| 106 | Vc(lo) | Clamp Voltage lo at all pins | I() = -1 mA | -1.6 | | -0.3 | V |
| 107 | ton() | Power-Up Time | VPD > 4 V, EEPROM Data valid after first I ² C read in | | 20 | | ms |
| 108 | ΔV/Δt | Power-Up Slew Rate at VPA = VPD | V() = 3.0 V → 4.5 V | 50 | | | V/s |
| 109 | CVPA, CVPD | Required Backup Capacitors at VPA, VPD | placed near by pin, recommended low ESR | | 100 | | nF |
| Hall Sensors | | | | | | | |
| 201 | Hext | Operating Magnetic Field Strength | at surface of chip | 15 | | 100 | kA/m |
| 202 | f() | Operating Magnetic Field Frequency | | | | 7 | kHz |
| 203 | rpm | Permissible Rotation of Pole Wheel with FRQ_CNV=lo | 16 pole pairs 32 pole pairs 64 pole pairs (note: for incremental part see table 80) | | | 24000 12000 6000 | rpm rpm rpm |
| 204 | vmax | Permissible Movement Speed | | | | 17 | m/s |
| 205 | hpac | Sensor-to-Package-Surface Distance | | | 400 | | µm |
| Assembly Tolerances | | | | | | | |
| 301 | TOLrad | Permissible Radial Displacement | | | | 0.5 | mm |
| 302 | TOLtan | Permissible Tangential Displacement | | | | 0.5 | mm |
| 303 | WOBrad | Permissible Eccentricity of Code Disc | MPC = 0x4 MPC = 0x5, 0x6 | | | 0.06 0.1 | mm mm |
| Bias Current Source, Reference Voltage, Power On Reset, Clock Oscillator | | | | | | | |
| 401 | Vbg | Bandgap Voltage | TEST = 0x1F | 1.18 | 1.24 | 1.36 | V |
| 402 | Vref | Reference Voltage | TEST = 0x1F | 45 | 50 | 55 | %VPA |
| 403 | IBM | Reference Current | CIBM = 0x0 CIBM = 0xF IBM calibrated | -370 -220 | -200 | -100 -180 | µA µA µA |
| 404 | VPDon | Turn-on Threshold VPD (Power-On Release) | increasing voltage at V(VPD) | 3.65 | 3.9 | 4.3 | V |
| 405 | VPDoff | Turn-off Threshold VPD (Power-Down Reset) | decreasing voltage at V(VPD) | 3 | 3.5 | 3.8 | V |
| 406 | VPDhys | Hysteresis | VPDhys = VPDon - VPDoff | 0.3 | | | V |
| 407 | fosc | Clock Frequency | TEST=0x26, fosc = 64*f(HCLK), IBM aligned | 22 | 26 | 32 | MHz |
| 408 | tchk | Max. Time For Internal Cyclic Checks | NCHK_NON = 0x0, CHK_MT = 0x1, NCHK_CRC = 0x0, MODE_MT = 0xF (18 bit), SBL_MT = 0x3 (4 bit), ESSI_MT = 0x1 (Error bit) | | | 6 | ms |
| Signal Conditioning Master and Nonius Track (x = M, N) | | | | | | | |
| 501 | GC | Adjustable Gain Range | GC_x = 0x0 GC_x = 0x1 GC_x = 0x2 GC_x = 0x3 | | 4.4 7.7 12.4 20.6 | | |
| 502 | GF | Adjustable Fine Gain Range | GF_x = 0x00 GF_x = 0x20 GF_x = 0x3F | | 1 4.4 19 | | |

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ELECTRICAL CHARACTERISTICS

Operating conditions: VPD = VPA = 5 V ±10%, Tj = -40...125°C, IBP calibrated to 200 µA, reference is VNA = VND, unless otherwise stated

| Item No. | Symbol | Parameter | Conditions | | | | Unit |
|--|-------------|---|---|-------|---------------|----------------|-------------------|
| | | | | Min. | Typ. | Max. | |
| 503 | GX | Adjustable Gain(SIN)/Gain(COS) | GX_x = 0x00 GX_x = 0x3F GX_x = 0x7F | 9 | 0 10 -9 | -8.5 | % % % |
| 504 | VOS | Adjustable Offset Calibration | VOS_x = 0x3F VOS_x = 0x7F | 60 | 70 -70 | -60 | mV mV |
| 505 | PHM | Adjustable Phase Calibration Master Track | PH_M = 0x3F PH_M = 0x7F | 6 | 7 -7 | -6 | ° ° |
| 506 | PHN | Adjustable Phase Calibration Nonius Track | PH_N = 0x3F PH_N = 0x7F | 11.25 | 13 -13 | -11.25 | ° ° |
| 507 | VampI | Signal Level Controller | chip internally, VampI = Vpp(PSINx)+Vpp(NSINx), ENAC = 1 | 3.2 | 4 | 4.8 | Vpp |
| 508 | Vae(lo) | Signal Monitoring Threshold lo | Vae(lo) = Vpp(PSINx)+Vpp(NSINx) | 1.2 | | 2.8 | Vpp |
| 509 | Vae(hi) | Signal Monitoring Threshold hi | Vae(hi) = Vpp(PSINx)+VPP(NSINx) | 4.9 | | 6.3 | Vpp |
| 510 | t(ana) | Latency of analog signal path | | | 11 | | µs |
| Sine-To-Digital Conversion | | | | | | | |
| 601 | AAabs | Absolute Angular Accuracy | ideal input signals, reference to 12 Bit of sine period | | | 2 | LSB |
| 602 | AArel | Relative Angular Accuracy | FILT = 0x2 FILT = 0x6 ideal input signals, reference to 12 Bit of sine period, f = 1 KHz | | | 2 1/4 | LSB LSB |
| Nonius Calculation | | | | | | | |
| 701 | Pnon | Permissible Track deviation Master vs. Nonius | 16 periods, MPC = 0x4 32 periods, MPC = 0x5 64 periods, MPC = 0x6 referenced to 360° of Master sine period | | | 10 5 2.5 | DEG DEG DEG |
| Digital Output Port PA1..3, MTC, SCL, SDA | | | | | | | |
| 801 | Vs(hi) | Saturation Voltage hi Pins PA1..3, MTC | Vs(hi) = V(VPD) - V(), I() = -4 mA | | | 0.4 | V |
| 802 | Vs(lo) | Saturation Voltage lo | I() = 4 mA versus VND | | | 0.4 | V |
| 803 | Isc(hi) | Short-Circuit Current hi Pins PA1..3, MTC | V() = V(VND), 25 °C | -90 | -50 | | mA |
| 804 | Isc(lo) | Short-Circuit Current lo | V() = V(VPD), 25 °C | | 50 | 90 | mA |
| 805 | tr() | Rise Time | CL = 50 pF | | | 60 | ns |
| 806 | tf() | Fall Time | CL = 50 pF | | | 60 | ns |
| 807 | Iik(PA3) | Leakage Current at PA3 | MODEA=0, PA0 = hi | -5 | | 5 | µA |
| 808 | fclk(SCL) | Frequency at SCL | normal mode during start-up | | 80 70 | | kHz kHz |
| Digital Input Port PA0..2, MTD, SCL, SDA | | | | | | | |
| 901 | Vt(hi) | Threshold Voltage hi | | | | 2 | V |
| 902 | Vt(lo) | Threshold Voltage lo | | 0.8 | | | V |
| 903 | Vt(hys) | Hysteresis | Vt(hys) = Vt(hi) - Vt(lo) | 150 | | | mV |
| 904 | Ipu() | Pull-Up Current Pins PA0..2, MTD | V() = 0 V ... V(VPD)-1 V | -60 | -30 | -6 | µA |
| 905 | Ipu() | Pull-Up Current Pins SCL, SDA | V() = 0 V ... V(VPD)-1 V | -800 | -300 | -80 | µA |
| 906 | f() | Permissible Input Frequency | | | | 10 | MHz |
| Analog/Digital Output Port PB0..3 | | | | | | | |
| A01 | I(buf) | Analog Driver Current | | -1 | | 1 | mA |
| A02 | fg(ana) | Analog Bandwidth | | | 100 | | kHz |
| A03 | Isc(hi,ana) | Analog Short-Circuit Current hi | V() = V(VND) | | | -1.4 | mA |
| A04 | Isc(lo,ana) | Analog Short-Circuit Current lo | V() = V(VPD) | 1.5 | | | mA |
| A05 | Rout(,ana) | Output Resistor, Analog Mode | I() = 1 mA | | | 500 | Ω |
| A06 | Vs(hi,dig) | Digital Saturation Voltage hi | Vs() = V(VPD) - V(), I() = -4 mA | | | 0.5 | V |
| A07 | Vs(lo,dig) | Digital Saturation Voltage lo | I() = 4 mA | | | 0.5 | V |

ELECTRICAL CHARACTERISTICS

Operating conditions: VPD = VPA = 5 V ±10%, Tj = -40...125°C, IBP calibrated to 200 µA, reference is VNA = VND, unless otherwise stated

| Item No. | Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|----------|-------------|--------------------------|--|------|------|------|------|
| | | | | | | | |
| A08 | Isc(hi,dig) | Short-Circuit Current hi | V() = V(VPD) | -60 | -35 | | mA |
| A09 | Isc(lo,dig) | Short-Circuit Current lo | V() = V(VND) | | 45 | 70 | mA |
| A10 | tr() | Rise Time | CL = 50 pF | | | 50 | ns |
| A11 | tf() | Fall Time | CL = 50 pF | | | 50 | ns |
| A12 | Ipu(PB3) | Pull-Up Current | V() = 0 V...V(VPD) - 1 V, MODEB = 0x0..0x3 | -60 | -30 | -6 | µA |
| A13 | Iik() | Leakage Current | MODEB = 0x7 | -5 | | 5 | µA |

OPERATING REQUIREMENTS: Multiturn Interface

| Item No. | Symbol | Parameter | Conditions | Min. | Max. | Unit |
|---------------------------------------|--------------------|--|------------|------|------|------|
| | | | | | | |
| Multiturn Interface (Figure 1) | | | | | | |
| I001 | t _{MTC} | Clock Period | | 6.4 | | µs |
| I002 | t _{sMD} | Setup Time: Data valid before MTC hi→lo | | 50 | | ns |
| I003 | t _{hMD} | Hold Time: Data stable after MTC hi→lo | | 50 | | ns |
| I004 | t _{tos} | Timeout | | 20 | | µs |
| I005 | t _{cycle} | Cycle Time | CHK_MT=1 | 1 | 5 | ms |

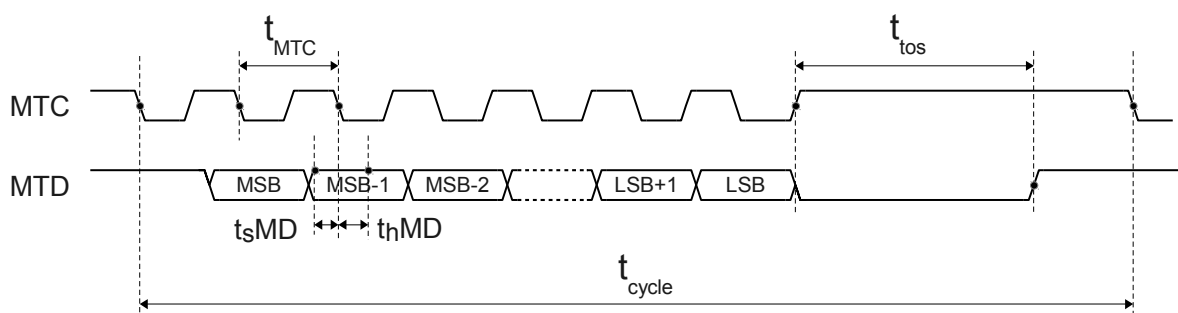


Figure 1: Timing multiturn interface, MODE_MT/=0

OPERATING REQUIREMENTS: I/O Interface

| Item No. | Symbol | Parameter | Conditions | Timing | | Unit |
|--|------------|---|------------------------------|---------------------|---------------------------------|------|
| | | | | Min. | Max. | |
| SPI-Interface (Figure 2) | | | | | | |
| I101 | t_{C1} | Permissible Clock Period | see Elec. Char. No.: 906 | 1/f() | | ns |
| I102 | t_{W1} | Wait Time: between NCS lo \rightarrow hi and NCS hi \rightarrow lo | | 500 | | ns |
| I103 | t_{S1} | Setup Time: NCS lo before SCLK lo \rightarrow hi | | 50 | | ns |
| I104 | t_{P1} | Propagation Delay: MISO stable after NCS hi \rightarrow lo | | | 50 | ns |
| I105 | t_{P2} | Propagation Delay: MISO high impedance after NCS lo \rightarrow hi | MODEA = 0x00 | 30 | | ns |
| I106 | t_{H1} | Hold Time: NCS lo after SCLK lo \rightarrow hi | valid for SPI mode 3 | 30 | | ns |
| I107 | t_{H3} | Hold Time: NCS lo after SCLK hi \rightarrow lo | valid for SPI mode 0 | 50 | | ns |
| I108 | t_{S2} | Setup Time: MOSI stable before SCLK lo \rightarrow hi | | 30 | | ns |
| I109 | t_{H2} | Hold Time: MOSI stable after SCLK lo \rightarrow hi | | 30 | | ns |
| I110 | t_{P3} | Propagation Delay: MISO stable after MOSI change | mode: repeating MOSI on MISO | | 50 | ns |
| I111 | t_{P4} | Propagation Delay: MISO stable after SCLK hi \rightarrow lo | mode: sending data MISO | 30 | | ns |
| I112 | t_{W2} | Wait Time: SCLK stable after NCS lo \rightarrow hi | | 500 | | ns |
| I113 | t_{L1} | Clock Signal lo Level Duration | | 25 | | ns |
| I114 | t_{L2} | Clock Signal hi Level Duration | | 25 | | ns |
| BiSS-Interface (Figure 3, Figure 4) | | | | | | |
| I115 | t_{tos} | Timeout adaptive | typ. t_{init} | $1.5 \cdot t_{MAS}$ | $1.5 \cdot t_{MAS} + 8/f_{osc}$ | ns |
| I116 | t_{MAS} | Permissible Clock Period | | 200 | | ns |
| I117 | t_{MASh} | Clock Signal Hi Level Duration | | 100 | t_{tos} | ns |
| I118 | t_{MASl} | Clock Signal Lo Level Duration | | 100 | | ns |
| SSI-Interface (Figure 5, Figure 6) | | | | | | |
| I119 | t_{tos} | Timeout adaptive | typ. t_{init} | $1.5 \cdot t_{MAS}$ | $1.5 \cdot t_{MAS} + 8/f_{osc}$ | |
| I120 | t_{MAS} | Permissible Clock Period | | 250 | | ns |
| I121 | t_{MASh} | Clock Signal Hi Level Duration | | 125 | t_{tos} | ns |
| I122 | t_{MASl} | Clock Signal Lo Level Duration | | 125 | | ns |

Timing SPI

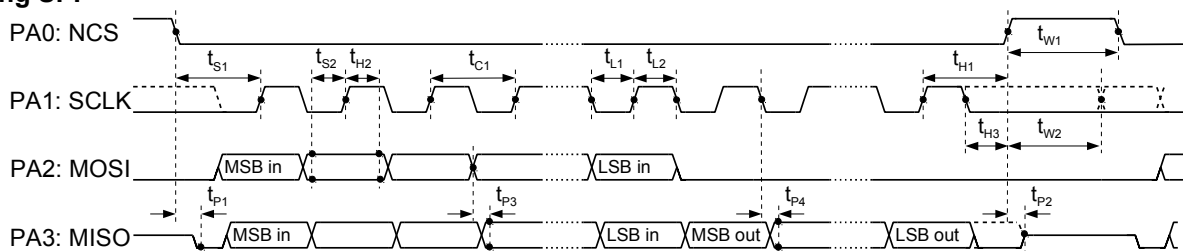


Figure 2: Timing SPI interface

PRINCIPLE OF MEASUREMENT

An absolute position measuring system consists of a magnetized code carrier and an iC-MU which integrates Hall sensors for signal scanning, signal conditioning, and interpolation in one single device. iC-MU can be used in rotative and linear measurement systems.

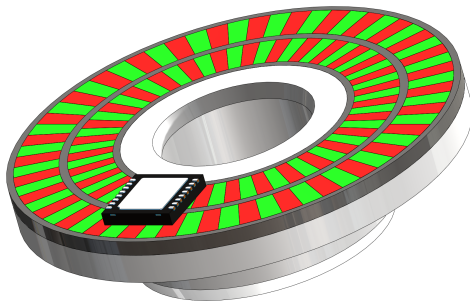


Figure 7: Rotative position measurement system

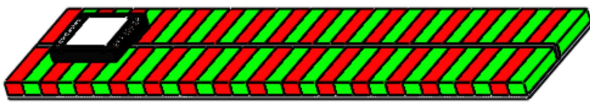


Figure 8: Linear position measurement system

Rotative measuring system

The magnetic code carrier consists of two magnetic encoder tracks. The outer track comprises an even number of alternately magnetized poles and is used for high-precision position definition. This is thus called the master track. The second inside track has one pole pair less than the outer track and is thus referred to as the nonius track. This track is used to calculate an absolute position within one revolution of the pole disc. To this end, the difference in angle between the two tracks is calculated.

| Number of pole pairs | | 16 | 32 | 64 |
|---------------------------------|-------|-------|-------|-------|
| Maximum resolution per rotation | [bit] | 18 | 19 | 20 |
| Master track diameter | [mm] | 13.04 | 26.08 | 52.15 |
| Chip center to axis center | [mm] | 4.72 | 11.24 | 24.28 |
| Nonius track diameter | [mm] | 5.84 | 18.88 | 44.95 |
| Master track pole width | [mm] | 1.28 | 1.28 | 1.28 |
| Nonius track pole width | [mm] | 0.61 | 0.96 | 1.12 |

Table 6: Pole disc dimensions in mm for rotative systems

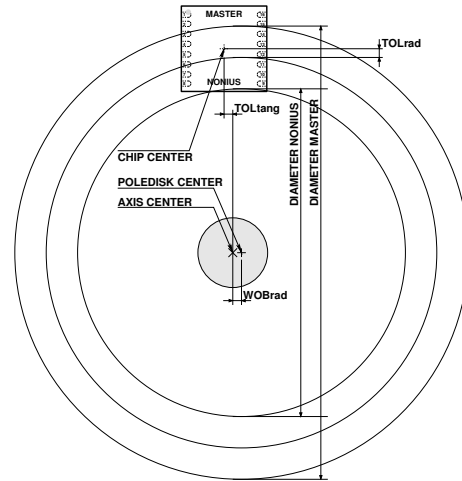


Figure 9: Definition of system measurements

The Hall sensors of iC-MU span one pole pair of the code carrier. The pole width of the master track is defined by the distance of the Hall sensors and is 1.28 mm. The position of the sensors on the upper chip edge has been optimized for 32 pole pairs. Accordingly, the Hall sensors generate a periodic sine and cosine signal with a cycle length of 2.56 mm. The scan diameter can be computed from the number of pole pairs. The diameter of the pole disc although depends on other mechanical requirements and should be approx. 3 mm greater than the scan diameter. A specific diameter for the master and nonius tracks is derived depending on the number of configured pole pairs.

The distance between the hall sensors of the nonius track and the master track is stipulated as being 3.6 mm by the evaluation device. The scan diameters of the nonius track can be seen in Table 6.

Linear measuring system

With a linear nonius system the pole width of the master track is also 1.28 mm. The pole width of the nonius track is defined by the number of pole pairs with

$$p_{\text{nonius}} = 1.28 \text{ mm} * \frac{\text{number of poles}_{\text{master}}}{\text{number of poles}_{\text{nonius}}}$$

| Number of pole pairs | | 16 | 32 | 64 |
|---|-------|-------|-------|--------|
| Maximum resolution with regard to absolute measurement length | [bit] | 18 | 19 | 20 |
| Absolute measurement length | [mm] | 40.96 | 81.92 | 163.84 |
| Master track pole width | [mm] | 1.28 | 1.28 | 1.28 |
| Nonius track pole width | [mm] | 1.365 | 1.321 | 1.300 |

Table 7: Linear scales, pole widths in mm

CONFIGURATION PARAMETERS

Analog parameters (valid for all channels)

CIBM: Bias current settings (p. 20)
ENAC: Amplitude control unit activation (p. 21)

Signal conditioning

GC_M: Master gain range selection (p. 20)
GF_M: Master gain (p. 20)
GX_M: Master cosine signal gain adjustment (p. 20)
VOSS_M: Master sine offset adjustment (p. 21)
VOSC_M: Master cosine offset adjustment (p. 21)
PH_M: Master phase adjustment (p. 21)
GC_N: Nonius gain range selection (p. 20)
GF_N: Nonius gain (p. 20)
GX_N: Nonius cosine signal gain adjustment (p. 20)
VOSS_N: Nonius sine offset adjustment (p. 21)
VOSC_N: Nonius cosine offset adjustment (p. 21)
PH_N: Nonius phase adjustment (p. 22)

Digital parameters

TEST: Adjustment modes/iC-Haus test modes (p. 23)
CRC16: EEPROM configuration data checksum (p. 25)
CRC8: EEPROM offset and preset data checksum (p. 26)
NCHK_CRC: Cyclic check of CRC16 and CRC8 (p. 26)
BANKSEL: Serial Access: Bank register (p. 52)
RPL: Register Access Control (p. 56)
RPL_RESET: Serial Access: Register for reset register access restriction (p. 56)
EVENT_COUNT: Serial Access: Event counter (p. 61)
HARD_REV: serial address: revision code (p. 55)

Configurable I/O interface

MODEA: I/O port A configuration (p. 29)
MODEB: I/O port B configuration (p. 29)
PA0_CONF: Configurable commands to pin PA0 (p. 63)
ROT_ALL: Direction of rotation (p. 49)
OUT_MSB: Output shift register configuration: MSB used bits (p. 31)
OUT_LSB: Output shift register configuration: LSB used bits (p. 31)
OUT_ZERO: Output shift register configuration: number of zeros inserted after the used bits and before an error/warning (p. 31)
MODE_ST: Data output (p. 30)
GSSI: Gray/binary data format (p. 34)
RSSI: Ring operation (p. 34)

Multiturn interface

MODE_MT: Multiturn mode (p. 44)
SBL_MT: Multiturn synchronization bit length (p. 44)
CHK_MT: Cyclic check of the multiturn value (p. 45)
GET_MT: MT interface daisy chain (p. 47)
ROT_MT: Direction of rotation external multiturn (p. 45)
ESSI_MT: Error Bit external multiturn (p. 45)
SPO_MT: Offset external multiturn (p. 45)

Converter and nonius calculation

FILT: Digital filter settings (p. 40)
MPC: Master period count (p. 40)
LIN: Linear scanning (p. 41)
SPO_x: Offset of nonius to master (x=BASE,0-14) (p. 41)
NCHK_NON: Cyclic check of the nonius value (low active) (p. 42)

Incremental output ABZ, STEP/DIR and CW/CCW

RESABZ: Incremental interface resolution ABZ,STEP-DIR,CW/CCW (p. 48)
LENZ: Index pulse length (p. 49)
INV_A: A/STEP/CW signal inversion (p. 49)
INV_B: B/DIR/CCW signal inversion (p. 49)
INV_Z: Z/NCLR signal inversion (p. 49)
SS_AB: System AB step size (p. 49)
FRQAB: AB output frequency (p. 49)
CHYS_AB: Converter hysteresis (p. 50)
ENIF_AUTO: Incremental interface enable (p. 50)

UVW commutation signals

PPUVW: Number of commutation signal pole pairs (p. 51)
PP60UVW: Commutation signal phase position (p. 51)
OFF_UVW: Commutation signal start angle (p. 51)
OFF_COM: serial address: absolute position offset for UVW calculation engine changed by nonius (p. 51)

Status/command registers and error monitoring

CMD_MU: serial address: command register (p. 60)
STATUS0: serial address: status register 0 (p. 58)
STATUS1: serial address: status register 1 (p. 58)
CFGEW: Error and warning bit configuration (p. 59)
EMTD: Minimum error message duration (p. 59)
ACC_STAT: Output configuration status register (p. 58)
ACRM_RES: Automatic reset with master track amplitude errors (p. 42)

BiSS specific IDs

DEV_ID: Device ID (p. 19)
MFG_ID: Manufacturer ID (p. 19)
EDSBANK: EDSBANK (p. 19)
PROFILE_ID: Profile ID (p. 19)
SERIAL: Serial number (p. 19)

Preset function

OFF_ABZ: Offset Absolute position offset for ABZ
calculation engine (p. 64)
OFF_POS: serial address: absolute position offset
for ABZ calculation engine changed by
nonius/multiturn (p. 64)
PRES_POS: Preset position for ABZ section (p. 64)

REGISTER ASSIGNMENTS (EEPROM)

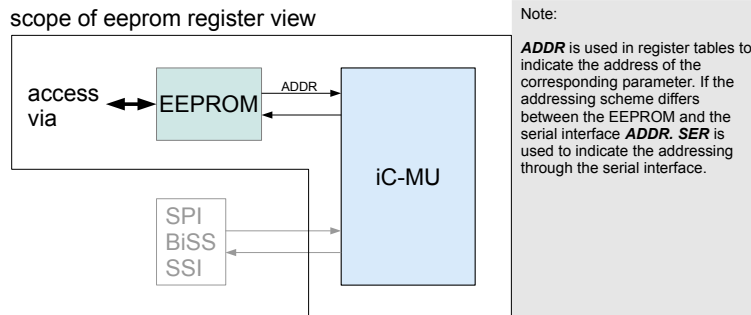


Figure 10: Scope of register mapping EEPROM

Register assignment (EEPROM)

| OVERVIEW | | | | | | | | |
|----------------------------|---------------|------------|--------------|--------------|---------------|-------|-----------|-------|
| Addr | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Signal Conditioning | | | | | | | | |
| 0x00 | GC_M(1:0) | | GF_M(5:0) | | | | | |
| 0x01 | GX_M(6:0) | | | | | | | |
| 0x02 | VOSS_M(6:0) | | | | | | | |
| 0x03 | VOSC_M(6:0) | | | | | | | |
| 0x04 | PH_M(6:0) | | | | | | | |
| 0x05 | ENAC | | | | | | CIBM(3:0) | |
| 0x06 | GC_N(1:0) | | GF_N(5:0) | | | | | |
| 0x07 | GX_N(6:0) | | | | | | | |
| 0x08 | VOSS_N(6:0) | | | | | | | |
| 0x09 | VOSC_N(6:0) | | | | | | | |
| 0x0A | PH_N(6:0) | | | | | | | |
| Digital Parameters | | | | | | | | |
| 0x0B | MODEB(2:0) | | | | MODEA(2:0) | | | |
| 0x0C | CFGEW(7:0) | | | | | | | |
| 0x0D | ACC_STAT | NCHK_CRC | NCHK_NON | ACRM_RES | EMTD(2:0) | | | |
| 0x0E | ESSI_MT(1:0) | | ROT_MT | LIN | FILT(2:0) | | | |
| 0x0F | SPO_MT(3:0) | | | | MPC(3:0) | | | |
| 0x10 | GET_MT | CHK_MT | SBL_MT(1:0) | | MODE_MT(3:0) | | | |
| 0x11 | OUT_ZERO(2:0) | | | OUT_MSB(4:0) | | | | |
| 0x12 | GSSI | RSSI | MODE_ST(1:0) | | OUT_LSB(3:0) | | | |
| 0x13 | RESABZ(7:0) | | | | | | | |
| 0x14 | RESABZ(15:8) | | | | | | | |
| 0x15 | ROT_ALL | SS_AB(1:0) | | ENIF_AUTO | FRQAB(2:0) | | | |
| 0x16 | LENZ(1:0) | | CHYS_AB(1:0) | PP60UVW | INV_A | INV_B | INV_Z | |
| 0x17 | RPL(1:0) | | PPUVW(5:0) | | | | | |
| TEST | | | | | | | | |
| 0x18 | TEST(7:0) | | | | | | | |
| TRACK-OFFSET | | | | | | | | |
| 0x19 | SPO_0(3:0) | | | | SPO_BASE(3:0) | | | |
| 0x1A | SPO_2(3:0) | | | | SPO_1(3:0) | | | |

| OVERVIEW | | | | | | | | |
|--------------------------------|--|---------------------|-------|-------|-------|-------------|-------|-------|
| Addr | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x1B | | SPO_4(3:0) | | | | SPO_3(3:0) | | |
| 0x1C | | SPO_6(3:0) | | | | SPO_5(3:0) | | |
| 0x1D | | SPO_8(3:0) | | | | SPO_7(3:0) | | |
| 0x1E | | SPO_10(3:0) | | | | SPO_9(3:0) | | |
| 0x1F | | SPO_12(3:0) | | | | SPO_11(3:0) | | |
| 0x20 | | SPO_14(3:0) | | | | SPO_13(3:0) | | |
| CRC16 | | | | | | | | |
| 0x21 | | CRC16(15:8) | | | | | | |
| 0x22 | | CRC16(7:0) | | | | | | |
| OFFSET/PRESET | | | | | | | | |
| 0x23 | | OFF_ABZ(3:0) | | | | | | |
| 0x24 | | OFF_ABZ(11:4) | | | | | | |
| 0x25 | | OFF_ABZ(19:12) | | | | | | |
| 0x26 | | OFF_ABZ(27:20) | | | | | | |
| 0x27 | | OFF_ABZ(35:28) | | | | | | |
| 0x28 | | OFF_UVW(3:0) | | | | | | |
| 0x29 | | OFF_UVW(11:4) | | | | | | |
| 0x2A | | PRES_POS(3:0) | | | | | | |
| 0x2B | | PRES_POS(11:4) | | | | | | |
| 0x2C | | PRES_POS(19:12) | | | | | | |
| 0x2D | | PRES_POS(27:20) | | | | | | |
| 0x2E | | PRES_POS(35:28) | | | | | | |
| CRC8 | | | | | | | | |
| 0x2F | | CRC8(7:0) | | | | | | |
| PA0_CONF | | | | | | | | |
| 0x30 | | PA0_CONF(7:0) | | | | | | |
| BiSS Profile and Serial number | | | | | | | | |
| 0x31 | | EDSBANK(7:0) = 0x01 | | | | | | |
| 0x32 | | PROFILE_ID(15:8) | | | | | | |
| 0x33 | | PROFILE_ID(7:0) | | | | | | |
| 0x34 | | SERIAL(31:24) | | | | | | |
| 0x35 | | SERIAL(23:16) | | | | | | |
| 0x36 | | SERIAL(15:8) | | | | | | |
| 0x37 | | SERIAL(7:0) | | | | | | |
| BiSS Identifier | | | | | | | | |
| 0x38 | | DEV_ID(47:40) | | | | | | |
| 0x39 | | DEV_ID(39:32) | | | | | | |
| 0x3A | | DEV_ID(31:24) | | | | | | |
| 0x3B | | DEV_ID(23:16) | | | | | | |
| 0x3C | | DEV_ID(15:8) | | | | | | |
| 0x3D | | DEV_ID(7:0) | | | | | | |
| 0x3E | | MFG_ID(15:8) | | | | | | |
| 0x3F | | MFG_ID(7:0) | | | | | | |
| Notes: | Register assignment for serial access through SPI/BiSS s.p. 52 | | | | | | | |

Table 8: Register assignment (EEPROM)

Special BiSS registers

For further information on parameters, see BiSS Interface Protocol Description (C Mode) www.ichaus.de/product/iC-MU.

| DEV_ID(7:0) | Addr. 0x3D; bit 7:0 |
|----------------------|-------------------------|
| | Addr. SER:0x7D; bit 7:0 |
| DEV_ID(15:8) | Addr. 0x3C; bit 7:0 |
| | Addr. SER:0x7C; bit 7:0 |
| DEV_ID(23:16) | Addr. 0x3B; bit 7:0 |
| | Addr. SER:0x7B; bit 7:0 |
| DEV_ID(31:24) | Addr. 0x3A; bit 7:0 |
| | Addr. SER:0x7A; bit 7:0 |
| DEV_ID(39:32) | Addr. 0x39; bit 7:0 |
| | Addr. SER:0x79; bit 7:0 |
| DEV_ID(47:40) | Addr. 0x38; bit 7:0 |
| | Addr. SER:0x78; bit 7:0 |
| Code | Description |
| 0x000000000000 | DEV_ID |
| ... | |
| 0xFFFFFFFFFFFF | |

Table 9: Device ID

| MFG_ID(7:0) | Addr. 0x3F; bit 7:0 |
|---------------------|-------------------------|
| | Addr. SER:0x7F; bit 7:0 |
| MFG_ID(15:8) | Addr. 0x3E; bit 7:0 |
| | Addr. SER:0x7E; bit 7:0 |
| Code | Description |
| 0x0000 | MFG_ID |
| ... | |
| 0xFFFF | |

Table 10: BiSS Manufacturer ID

| EDSBANK(7:0) | Addr. 0x31; bit 7:0 |
|---------------------|--|
| EDSBANK(7:0) | Addr. SER:0x41; bit 7:0 |
| Code | Description |
| 0x00 | no EDS |
| 0x01 | |
| ... | |
| 0xFFE | EDSBANK pointer to first EDS bank |
| 0xFF | |
| 0xFF | no EDS |
| Note: | |
| | recommended value 0x02, in this case an additional sensor like iC-PVL can use BANK 1 for configuration |

Table 11: EDSBANK: Start of EDS-part

| PROFILE_ID(7:0) | Addr. 0x33; bit 7:0 |
|-------------------------|-------------------------|
| | Addr. SER:0x43; bit 7:0 |
| PROFILE_ID(15:8) | Addr. 0x32; bit 7:0 |
| | Addr. SER:0x42; bit 7:0 |
| Code | Description |
| 0x0000 | PROFILE_ID |
| ... | |
| 0xFFFF | |

Table 12: Profile ID

| SERIAL(7:0) | Addr. 0x37; bit 7:0 |
|----------------------|-------------------------|
| | Addr. SER:0x47; bit 7:0 |
| SERIAL(15:8) | Addr. 0x36; bit 7:0 |
| | Addr. SER:0x46; bit 7:0 |
| SERIAL(23:16) | Addr. 0x35; bit 7:0 |
| | Addr. SER:0x45; bit 7:0 |
| SERIAL(31:24) | Addr. 0x34; bit 7:0 |
| | Addr. SER:0x44; bit 7:0 |
| Code | Description |
| 0x00000000 | SERIAL |
| ... | |
| 0xFFFFFFFF | |

Table 13: Serial number

SIGNAL CONDITIONING FOR MASTER AND NONIUS CHANNELS: x = M,N

Bias current source

The calibration of the bias current source in test mode $TEST=0x1F$ is prerequisite for adherence to the given electrical characteristics and also instrumental in the determination of the chip timing (e.g. SCL clock frequency). For the calibration the current out of pin PB2 into VNA must be measured, and register bits CIBM changed until the current is calibrated to 200 μ A.

| CIBM(3:0) Addr. 0x05; bit 3:0 | |
|-------------------------------|-------------|
| Code | Description |
| 0x0 | -40 % |
| ... | ... |
| 0x8 | 0 % |
| 0x9 | +5 % |
| ... | ... |
| 0xF | +35 % |

Table 14: Calibrating the bias current

Gain settings

iC-MU has signal conditioning features that can compensate for signal and adjustment errors. The Hall signals are amplified in two stages. The gain of both amplification stages is automatically controlled when the bit ENAC is set to '1'. The register bits GC_x and GF_x have no effect. In the case of a deactivated automatic gain control (ENAC='0') the gain must be set manually. First, the approximate field strength range must be selected in which the Hall sensor is to be operated. The first amplifier stage can be programmed in the following ranges:

| GC_M(1:0) Addr. 0x00; bit 7:6 | |
|-------------------------------|-------------|
| GC_N(1:0) Addr. 0x06; bit 7:6 | |
| Code | Coarse gain |
| 0x0 | 4.4 |
| 0x1 | 7.8 |
| 0x2 | 12.4 |
| 0x3 | 20.7 |

Table 15: Selection of the Hall signal amplification range

The second amplifier stage can be varied within a wide range.

| GF_M(5:0) Addr. 0x00; bit 5:0 | |
|-------------------------------|---------------------------------------|
| GF_N(5:0) Addr. 0x06; bit 5:0 | |
| Code | Fine gain |
| 0x00 | 1.000 |
| 0x01 | 1.048 |
| ... | $\exp(\frac{\ln(20)}{64} \cdot GF_x)$ |
| 0x3F | 19.08 |

Table 16: Hall signal amplification

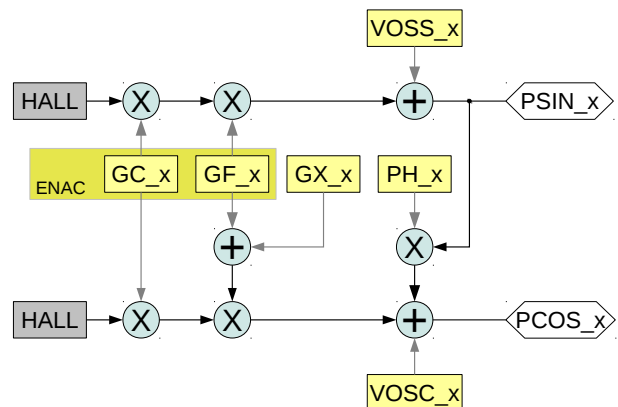


Figure 11: Conditioning of hall voltages

Register GX_x enables the sensitivity of the sine channel in relation to the cosine channel to be corrected. The amplitude of the cosine channel is adapted to the amplitude of the sine channel. The cosine amplitude can be corrected within a range of approx. ± 10 %.

| GX_M(6:0) Addr. 0x01; bit 6:0 | |
|-------------------------------|--|
| GX_N(6:0) Addr. 0x07; bit 6:0 | |
| Code | Description |
| 0x00 | 1.000 |
| 0x01 | 1.0015 |
| ... | $\exp(\frac{\ln(20)}{2048} \cdot GX_x)$ |
| 0x3F | 1.0965 |
| 0x40 | 0.9106 |
| ... | $\exp(-\frac{\ln(20)}{2048} \cdot (128 - GX_x))$ |
| 0x7F | 0.9985 |

Table 17: Cosine gain adjustment

The integrated amplitude control unit can be activated using bit ENAC. In this case the differential signal amplitude is regulated to 2 Vpp; the values of GF_x have no effect here.

| ENAC | | Addr. 0x05; bit 7 |
|------|--|-------------------|
| Code | Description | |
| 0 | Amplitude control not active (<i>constant</i>) | |
| 1 | Amplitude control active ($\sin^2 + \cos^2$) | |

Table 18: Amplitude control unit activation

The current gain set by the amplitude control unit can be read with the parameters ACGAIN_M and ACGAIN_N for the gain range, AFGAIN_M and AFGAIN_N for the gain factor (ref. Table 19 and 20). AFGAIN_M and AFGAIN_N shows coarse steps of the gain factor, but the amplitude control unit uses a finer resolution to control the gain factor.

| ACGAIN_M(1:0) | | Addr. SER:0x2B; bit 4:3 | R |
|---------------|------------|-------------------------|---|
| ACGAIN_N(1:0) | | Addr. SER:0x2F; bit 4:3 | R |
| Code | Gain range | | |
| 0x0 | 4.4 | | |
| 0x1 | 7.8 | | |
| 0x2 | 12.4 | | |
| 0x3 | 20.7 | | |

Table 19: Current gain range of amplitude control unit

| AFGAIN_M(2:0) | | Addr. SER:0x2B; bit 2:0 | R |
|---------------|--|-------------------------|---|
| AFGAIN_N(2:0) | | Addr. SER:0x2F; bit 2:0 | R |
| Code | Description | | |
| 0x0 | 1.00 | | |
| 0x1 | 1.45 | | |
| ... | $\exp\left(\frac{\ln(20)}{8}\right) \cdot AFGAIN_x$ | | |
| 0x7 | 13.75 | | |

Table 20: Current gain factor of amplitude control unit

After startup the gain is increased until the set amplitude is obtained. If the input amplitude is altered by the distance between the magnet and sensor being varied, or if there is a change in the supply voltage or temperature, the gain is automatically adjusted. The conversion of the sine signals into high-resolution quadrature signals thus always takes place at optimum amplitude.

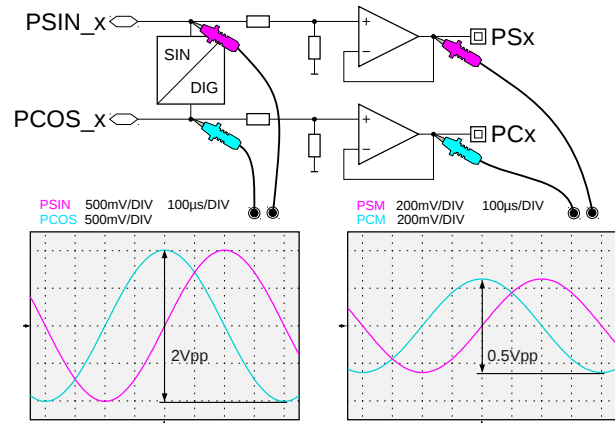


Figure 12: Definition of peak-peak amplitude

Offset compensation

If there is an offset in the sine or cosine signal, possibly caused by a magnet not being precisely adjusted, for instance, this can be corrected by registers VOSS_x and VOSC_x. The output voltage can be shifted in each case by ± 63 mV in order to compensate for the offset.

| VOSS_M(6:0) | | Addr. 0x02; bit 6:0 |
|-------------|-------------|---------------------|
| VOSS_N(6:0) | | Addr. 0x08; bit 6:0 |
| VOSC_M(6:0) | | Addr. 0x03; bit 6:0 |
| VOSC_N(6:0) | | Addr. 0x09; bit 6:0 |
| Code | Description | |
| 0x00 | 0 mV | |
| 0x01 | 1 mV | |
| ... | ... | |
| 0x3F | 63 mV | |
| 0x40 | 0 mV | |
| 0x41 | -1 mV | |
| ... | ... | |
| 0x7F | -63 mV | |

Table 21: Sine and cosine offset adjustment

Phase adjustment

The phase between sine and cosine is adjusted by PH_x (6:0). The compensation range for the master track is approx. $\pm 6^\circ$. The compensation range for the nonius track is nearly twice as large and is approx. $\pm 11.25^\circ$.

| PH_M(6:0) | | Addr. 0x04; bit 6:0 |
|-----------|------------------------------------|---------------------|
| Code | Function | |
| 0x00 | 0° | |
| ... | $+6^\circ \cdot PH_M / 63$ | |
| 0x3F | $+6^\circ$ | |
| 0x40 | 0° | |
| ... | $-6^\circ \cdot (PH_M - 64) / 63$ | |
| 0x7F | -6° | |

Table 22: Master track phase adjustment

| PH_N(6:0) Addr. 0x0A; bit 6:0 | |
|--------------------------------------|-----------------------|
| Code | Function |
| 0x00 | 0° |
| ... | + 11.25°*PH_N/63 |
| 0x3F | + 11.25° |
| 0x40 | 0° |
| ... | - 11.25°*(PH_N-64)/63 |
| 0x7F | - 11.25° |

Table 23: Nonius track phase adjustment

ANALOG SIGNAL CONDITIONING FLOW: x = M,N

For the purpose of signal conditioning iC-MU has several settings that make internal reference values and the amplified Hall voltages of the individual sensors accessible at the outer pins of PORT B for measurement. This allows the settings of the amplifier (GC_x, GF_x), the amplitude ratio of cosine to sine signal (GX_x), and the offset (VOSS_x, VOSC_x) and phase (PH_x) of the master (x = M) and nonius tracks (x = N) to be directly observed on the oscilloscope.

Note:

For an easy installation and setup, the analog and the track offset SPON correction should be done by using the automatic calibration functions of the GUI software (or DLL) available for iC-MU. All necessary steps are described in the iC-MU application note AN3: http://www.ichaus.de/MU_AN3_appnote_en

Test mode can be programmed using register TEST (address 0x18). The individual test modes are listed in Table 24 and 25.

Note:

MODEB must be set to 0x0 before selecting a test mode. In test mode 0x1F (Analog REF) I2C communication is disabled.

| Test Mode output signals | | | | | |
|--------------------------|------|---------|---------|---------|---------|
| Mode | TEST | Pin PB0 | Pin PB1 | Pin PB2 | Pin MTC |
| Normal | 0x00 | | | | |
| Analog REF | 0x1F | VREF | VBG | IBM | - |
| Digital CLK | 0x26 | - | - | - | CLK |

Table 24: Test modes for signal conditioning

1. Conditioning the BIAS current

First of all, the internal bias is set. The BIAS current is adjustable in the range of -40 % to +35% to compensate variations of this current and thus differences in characteristics between different iC-MU (e.g. due to manufacturing variations). The nominal value of 200 µA is measured as a short-circuit current at pin PB2 referenced to VNA in test mode 0x1F.

Additionally various internal reference voltages are available for measuring in this test mode. VREF corresponds to half the supply voltage (typically 2.5 V) and is used as a reference voltage for the hall sensor signals. VBG is the internal bandgap reference (1.25 V)

Alternatively the frequency at Pin MTC can be adjusted to 405 kHz ($\frac{f_{osc}}{64}$, see elec. char. no.: 407) using register value CIBM in test mode 0x26, if an analog measuring of the current is not possible.

| Test mode output signals | | | | | |
|--------------------------|------|---------|---------|---------|---------|
| Mode | TEST | Pin PB0 | Pin PB1 | Pin PB2 | Pin PB3 |
| Normal | 0x00 | | | | |
| Analog Master | 0x01 | PSM | NSM | PCM | NCM |
| Analog CNV_M | 0x03 | PSIN_M | NSIN_M | PCOS_M | NCOS_M |
| Analog Nonius | 0x11 | PSN | NSN | PCN | NCN |
| Analog CNV_N | 0x13 | PSIN_N | NSIN_N | PCOS_N | NCOS_N |

Table 25: Test modes and available output signals

The output signals of the signal path are available as differential signals with a mean voltage of half the supply voltage and can be selected for output according to Table 25.

2. Positioning of the sensor

Next, the sensor should be adjusted in relation to the magnetic code carrier. The value of MPC (Table 54) has to be selected according to the magnetic code carrier. The register values for VOSS_x, VOSC_x, GX_x and PH_x are set to 0. The chip position will now be displaced radially to the magnetic code carrier until the phase shift between the sine and cosine is 90°.

Depending on the mounting of the system it may be necessary to displace iC-MU tangentially to the magnetic code carrier to adjust the amplitude between the sine and cosine signals.

A fine adjustment of the analog signals is made with the registers described in the chapter SIGNAL CONDITIONING FOR MASTER AND NONIUS CHANNELS page 20.

The adjustment should be made in the order:

1. phase
2. amplitude
3. offset

3.a Test modes analog master and analog nonius

In these test modes the amplified, conditioned signals are presented to port B. These signals can be charged with a maximum of 1 mA and should not exceed a differential voltage of 0.5 Vpp.

3.b Test mode CNV_x

In this test mode the sensor signals are present at port B as they are internally for further processing on the interpolator. The achievable interpolation accuracy is determined by the quality of signals PSIN_x/NSIN_x and PCOS_x/NCOS_x and can be influenced in this test mode by adjustment of the gain, amplitude ratio,

offset, and phase. The signals must be tapped at high impedance.

4. Track offset SPON

After the analog adjustment of the master and nonius track the absolute system must be electrically calibrated for maximum adjustment tolerance. See page 41 ff.

EEPROM AND I2C INTERFACE

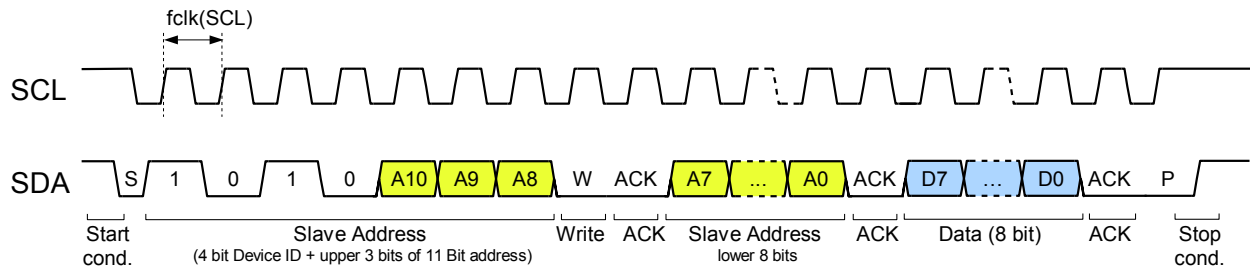


Figure 13: I²C slave addressing for writing a single byte to the EEPROM.

Basic interface features

| I2C Master Performance | |
|-------------------------|---|
| Protocol | Standard I ² C |
| Clock Rate (Output) | 70/80 kHz max. (refer to Elec.Char. 808) |
| Addressing | 11 bit: 8 bit register address plus 3 bit block selection |
| Multi-Master Capability | Yes |

Table 26: I²C interface performance

The multimaster-I2C interface enables read and write access to a serial EEPROM. The basic EEPROM requirements are summarized in Table 27.

EEPROM device requirements

| EEPROM Device Requirements | |
|----------------------------|--|
| Supply Voltage | 2.5 V to 5.5 V (respectively according to VPA/VPD) |
| Power-On Threshold | < 3.6 V (due to Elec.Char. 404) |
| Addressing | 11 bit address max. |
| Device Address | 0x50 ('1010 000' w/o R/W bit), 0xA0 ('1010 0000' with R/W = 0) |
| Page Buffer | Not required |
| Size Min. | 1 Kbit (128x8 bit), type 24C01, for configuration data |
| Size Max. | 16 Kbit (8x 256x8 bit), type 24C16 Size limited due to 11-bit slave addressing. |

Table 27: EEPROM Device Requirements

It is not relevant if the EEPROM's internal page buffer is 8 or 16 bytes. EEPROMs beyond 16 Kbit can not be used as those require a 2 byte address.

ATTENTION: EEPROMs which consider block selection bits as "don't care" should not be used. This can be the case with 8-pin devices, as well as with 5-pin devices not featuring A2, A1, A0 pins.

Be aware of potential conflicts:

If a user tries to access memory beyond the 2 Kbit range, the iC-MU configuration data will be overwritten.

If further I²C slave devices are operated on the same bus, higher device addresses may be occupied.

CRC checksums

The configuration data in the EEPROM in address range 0x00 to 0x20 and 0x30 to 0x3F is secured with a 16 bit CRC (CRC16). The start value for the CRC16 calculation is 1.

| | |
|---------------------|---|
| CRC16(7:0) | Addr. 0x22; bit 7:0 |
| CRC16(15:8) | Addr. 0x21; bit 7:0 |
| CRC16(7:0)* | Addr. SER: 0x80; bit 7:0 |
| CRC16(15:8)* | Addr. SER: 0x81; bit 7:0 |
| Code | Meaning |
| ... | CRC formed with CRC polynomial 0x11021**) |
| Notes: | *) Access only via SPI interface **) $x^{16} + x^{12} + x^5 + 1$, start value 0x1 This is equivalent to CRC-CCITT/CRC-16 |

Table 28: EEPROM data checksum

The offset and preset position for iC-MU's preset sequence is not part of the configuration data area. The data is located in address range 0x23 to 0x2E of the EEPROM and is secured separately with a 8-bit CRC (CRC8). The start value for the CRC8 calculation is 1.

| | |
|--|---|
| CRC8(7:0) Addr. 0x2F; bit 7:0 | |
| CRC8(7:0)* Addr. SER: 0x82; bit 7:0 | |
| Code | Meaning |
| ... | CRC formed with CRC polynomial 0x197**) |
| Notes: | *) Access only via SPI interface **) $x^8 + x^7 + x^4 + x^2 + x^1 + 1$, start value 0x1 |

Table 29: Offset/preset data checksum

| | |
|-----------------------------------|---|
| NCHK_CRC Addr. 0x0D; bit 6 | |
| Code | Meaning |
| 0 | cyclical CRC check of CRC16 and CRC8 |
| 1 | no cyclical CRC check |
| Notes: | For max. duration of the internal cyclic checks see elec. char. no. 408 |

Table 30: Cyclic CRC check

iC-MU calculates CRC8 and CRC16 automatically when writing the configuration to the EEPROM. However, an example of a CRC calculation routine is given in Tab. 31. The serial interface allows to access the CRC8 and CRC16 values only in SPI mode. CRC16 and CRC8 are checked on startup. A cyclic check during operation can be configured with NCHK_CRC. With the command CRC_VER (s. Tab. 104) a CRC check can be explicitly requested. An error is signaled by status bit CRC_ERR.

```

unsigned char ucDataStream = 0;
int iCRC_CRC8Poly = 0x97;
unsigned char ucCRC8;
int i = 0;

ucCRC8 = 1; // start value !!!
for (iReg = 35; iReg<47; iReg ++ )
{
    ucDataStream = ucGetValue(iReg);
    for (i=0; i<=7; i++) {
        if ((ucCRC8 & 0x80) != (ucDataStream & 0x80))
            ucCRC8 = (ucCRC8 << 1) ^ iCRC_CRC8Poly;
        else
            ucCRC8 = (ucCRC8 << 1);
        ucDataStream = ucDataStream << 1;
    }
}
    
```

Table 31: Example of CRC calculation routine using CRC8

STARTUP BEHAVIOR

After switching on the power (power-on reset) iC-MU reads the configuration data out from the EEPROM. If an error occurs during the EEPROM data readout (a CRC error or communication fault with the EEPROM), the current read-in is aborted and restarted. Following a third faulty attempt the read-in process is terminated and the internal iC-MU configuration register initialized as in Tab. 33. The addresses are referenced to the register allocation for an register access through the serial interface s. p. 52.

Note: After the third faulty attempt to read-in the configuration data from the EEPROM the default value of MODEA is set to BiSS or SPI depending on the logic level at pin PA0 (PA0=0 → BiSS, PA0=1 → SPI_{TRI}).

| Pin PA0 | I/O Interface | Data length |
|---------|---------------|---|
| 0 | BiSS | 32 bit (24 bit + 2 bit E/W + 6 bit CRC) |
| 1 | SPI | 24 bit |

Table 32: Default interface depending on PA0

The amplitude control is started after the read-in of the EEPROM. To determine the absolute position a nonius calculation is started. An external multiturn is read-in if configured. If there is an error the multiturn read-in is repeated until no multiturn error occurs. The status bit MT_ERR is set in this case, register communication is possible. The ABZ/UVW-converter is only started if there was no CRC_ERR, EPR_ERR, MT_ERR or MT_CTR error during startup. The startup behaviour is described in Figure 14.

| Default values | | | |
|----------------|---|----------|---|
| Bank | Addr. (serial access) | value | Meaning |
| 0 | 0x05 | 0x88 | Amplitude control active (ENAC=1), CIBM = 0% |
| 0 | 0x0B | 0x02 | PA0=0 → BiSS interface (MODEA=0x2), ABZ Incremental (MODEB=0x0) |
| 0 | | 0x00 | PA0=1 → SPI interface (MODEA=0x0), ABZ Incremental (MODEB=0x0) |
| 0 | 0x0E | 0x06 | FILTER activated |
| 0 | 0x0F | 0x05 | 32 pole pairs master track |
| 0 | 0x10 | 0x00 | no Multiturn, Nonius check active |
| 0 | 0x11 | 0xA5 | 5 bit Nonius information, 5 Zeros added |
| 0 | 0x12 | 0x00 | output with max. resolution |
| 0 | 0x13 | 0xFF | resolution 16384 edges |
| 0 | 0x14 | 0x0F | |
| 0 | 0x15 | 0x13 | up to 12000 rpm (SS_AB=0x1), 266ns minimum edge distance |
| 0 | 0x16 | 0x10 | 90° Index, 0.175° Hysteresis |
| 0 | 0x17 | 0x02 | 1 pole pair commutation |
| - | 0x78 | 0x4D | ≈ M |
| - | 0x79 | 0x55 | ≈ U |
| - | 0x7A | HARD_REV | s. Tab. 94 |
| - | 0x7E | 0x69 | ≈ i |
| - | 0x7F | 0x43 | ≈ C |
| Notes: | all other registers are preset with 0 Register assignment for register access through serial interface s.p. 52 | | |

Table 33: Default configuration without the EEPROM

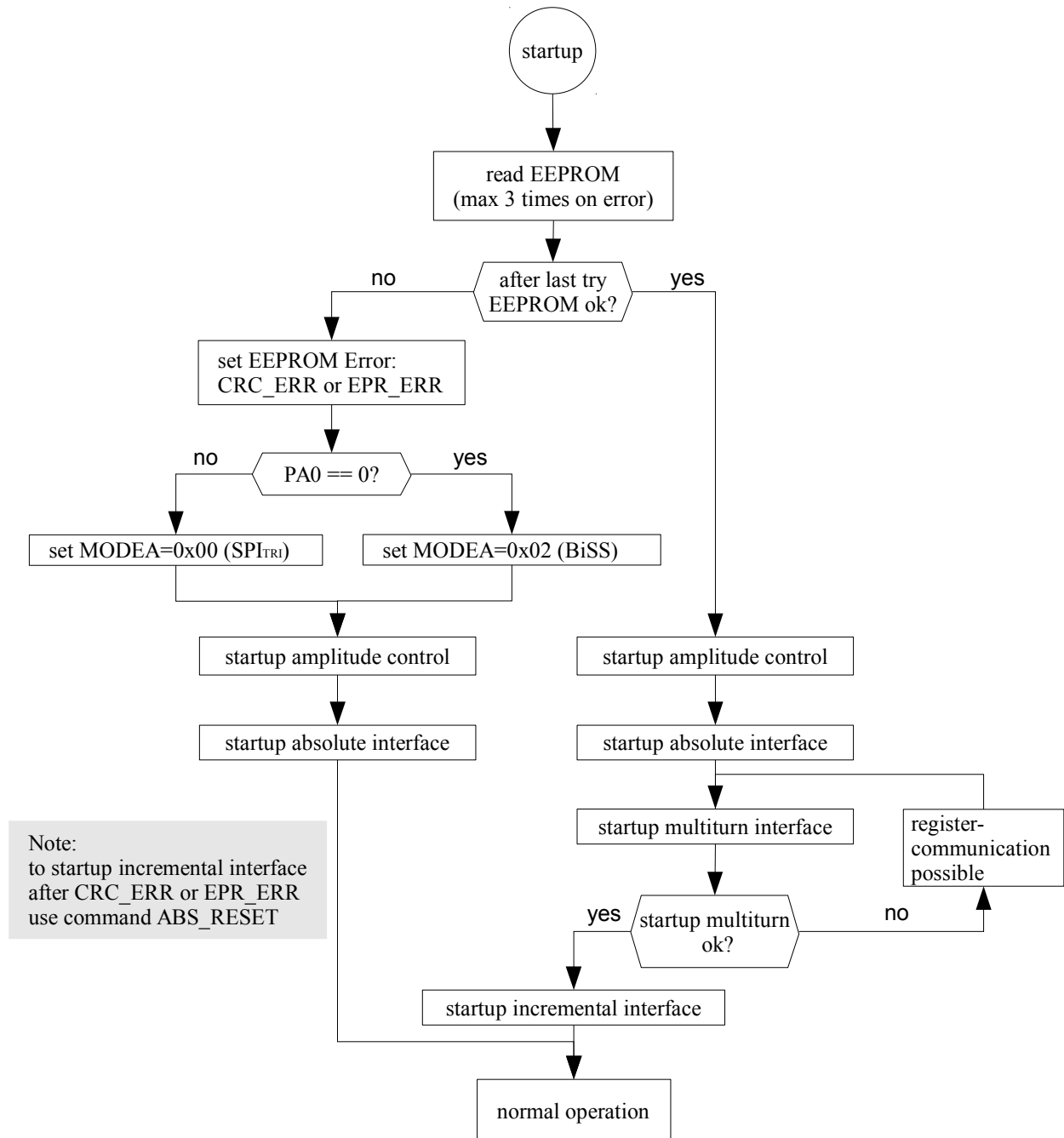


Figure 14: Startup behavior

CONFIGURABLE I/O INTERFACE

Setting the interfaces

iC-MU has several configurable output modes which can be set using parameters MODEA and MODEB. The pins at port A are set with MODEA. The choice of a serial interface at port A has also effect on the output of error and warning bits in the serial protocol see Table 37.

Note:

With an empty EEPROM or after the third faulty attempt to read-in the configuration data from the EEPROM the default value of MODEA is set to BiSS or SPI depending on the logic level at pin PA0 (PA0=0 → BiSS, PA0=1 → SPI_{TRI}).

| MODEA(2:0) Addr. 0x0B; bit 2:0 | | | | | |
|--------------------------------|-------|------|------|------|--------------------|
| Code | PA0 | PA1 | PA2 | PA3 | Function |
| 0x0 | NCS | SCLK | MOSI | MISO | SPI _{TRI} |
| 0x1 | NCS | SCLK | MOSI | MISO | SPI |
| 0x2 | NPRES | MA | SLI | SLO | BiSS |
| 0x3 | NPRES | A | B | Z | ABZ *) |
| 0x4 | NPRES | MA | SLI | SLO | SSI **) |
| 0x5 | NPRES | MA | SLI | SLO | SSI+ERRL |
| 0x6 | NPRES | MA | SLI | SLO | SSI+ERRH |
| 0x7 | NPRES | MA | SLI | SLO | ExtSSI |

Note: *) to save this configuration in the EEPROM see command SWITCH page 60 ff.

**) MT sensor communication not possible (GET_MT = 0)

Table 34: Port A configuration

The pins at port B are set with MODEB.

| MODEB(2:0) Addr. 0x0B; bit 6:4 | | | | | |
|--------------------------------|------|-----|------|------|--------------------|
| Code | PB0 | PB1 | PB2 | PB3 | Function |
| 0x0 | A | B | Z | NER* | ABZ |
| 0x1 | U | V | W | NER* | UVW |
| 0x2 | STEP | DIR | NCLR | NER* | Step/Direction |
| 0x3 | CW | CCW | NCLR | NER* | CW/CCW Incremental |
| 0x4 | NSN | PSN | PCN | NCN | SIN/COS Nonius** |
| 0x5 | NSM | PSM | PCM | NCM | SIN/COS Master** |
| 0x6 | - | - | - | - | reserved |
| 0x7 | - | - | - | - | tristate |

Note: *) Pin PB3 (signal NER) is an open-collector output

**) NSx, PSx, PCx, NCx vs. GND $V_{pk}() = 250\text{ mV}$, $V_{CM}() = V_{PA}/2$

Table 35: Port B configuration

Note:

It is not possible to select ABZ at port A and ABZ, Step/Direction or CW/CCW at port B simultaneously.

In operating modes ABZ, UVW, step/direction, and CW/CCW the position is output incrementally. In setting SIN/COS Master the master track analog signal is switched directly to the analog drivers. The signals of the nonius track are available on the drivers with setting SIN/COS Nonius.

Serial interface
Configuring the data format and data length

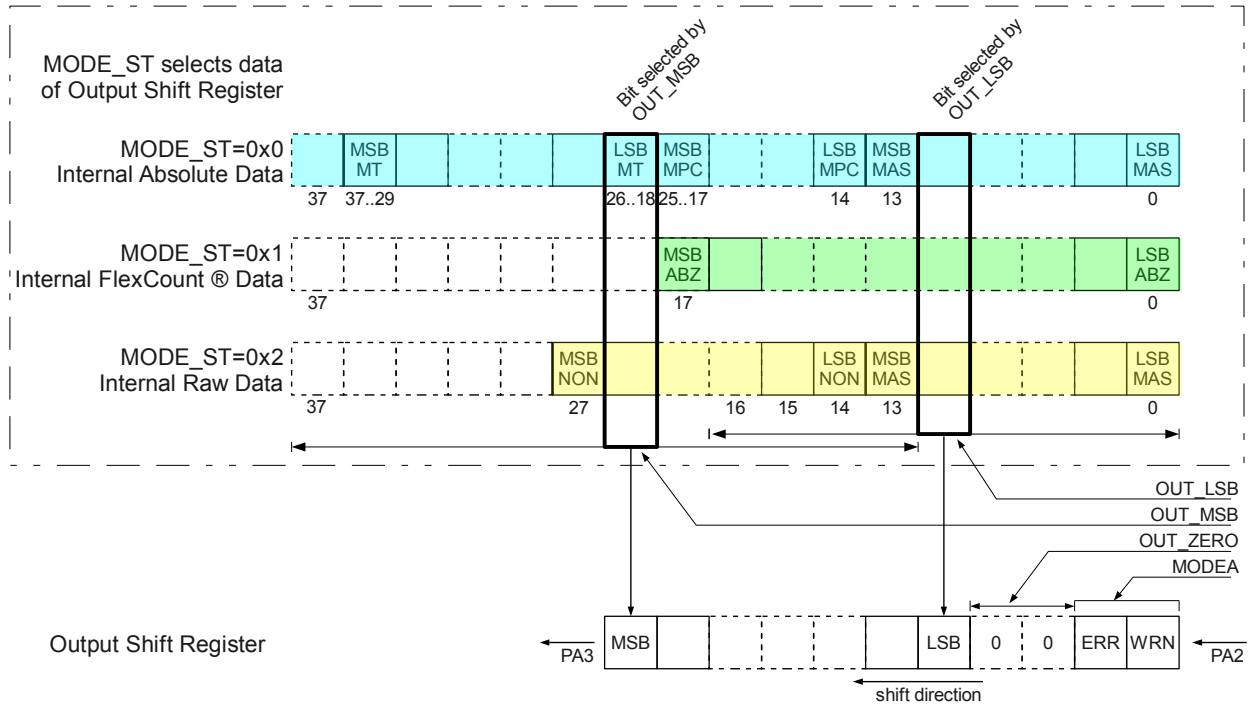


Figure 15: Determining the output data length

The structure of the output shift register is shown in Figure 15. The abbreviation MT stands for the multiturn data, MPC is short for the number of master periods in bit, ABZ for the data whose resolution is specified by the parameter RESABZ (Table 74), NON for the data of the nonius track and MAS for the data of the master track. The numbering of the user data starts at the LSB with zero. OUT_MSB and OUT_LSB determine which part of the user data is output by the output shift register.

MODE_ST selects the type of user data to be output through the output shift register.

| MODE_ST(1:0) Addr. 0x12; bit 5:4 | |
|----------------------------------|--|
| Code | Description |
| 0x0 | output absolute position |
| 0x1 | output position in user resolution*) (FlexCount®) |
| 0x2 | output raw-data of Master- and Nonius track**) |
| 0x3 | reserved |
| Note: | *) resolution defined by RESABZ (Table 74) **) MPC must be ≠ 12 |

Table 36: Selection of output data

The number of output bits is determined by parameters OUT_MSB, OUT_LSB, OUT_ZERO and the error/warning bits (see Figure 15 and Table 37):

Data length = 14 + OUT_MSB - OUT_LSB + OUT_ZERO + optional ERR/WRN (depending on MODEA)

There is an exception for the calculation of the output data length. If parameter MPC=12, OUT_LSB = 0 and OUT_MSB > 0x02 the number of output bits is given by:

data_length_2 = OUT_MSB + OUT_ZERO + ERR/WRN (depending on MODEA) - 2

| MODEA(2:0) Addr. 0x0B; bit 2:0 | | | | |
|--------------------------------|------------|-------------|------------|-------------|
| Function | Error | | Warning | |
| | low active | high active | low active | high active |
| SPI | - | - | - | - |
| BiSS | ✓ | - | ✓ | - |
| SSI | - | - | - | - |
| SSI+ERRL | ✓ | - | - | - |
| SSI+ERRH | - | ✓ | - | - |
| ExtSSI | ✓ | - | ✓ | - |

Table 37: MODEA: error/warning-bit within serial protocols

OUT_MSB configures the bit of the user data which is output as MSB at pin PA3.

| OUT_MSB(4:0) Addr. 0x11; bit 4:0 | |
|---|--------------|
| Code | Description |
| 0x00 | MSB = Bit 13 |
| 0x01 | MSB = Bit 14 |
| ... | ... |
| 0x18 | MSB = Bit 37 |

Table 38: Selection of shift register MSB

OUT_LSB determines the LSB of the user data being output through the output shift register.

| OUT_LSB(3:0) Addr. 0x12; bit 3:0 | | |
|---|---|-----------------------------|
| Code | Condition | Description |
| 0x0 | MPC = 12, OUT_MSB > 0x02 MPC ≠ 12 | LSB = Bit 16 LSB = Bit 0 |
| 0x1 | - | LSB = Bit 1 |
| 0x2 | - | LSB = Bit 2 |
| ... | - | ... |
| 0xD | - | LSB = Bit 13 |
| 0xE | OUT_MSB > 0x00 | LSB = Bit 14 |
| 0xF | OUT_MSB > 0x01 | LSB = Bit 15 |

Table 39: Selection of shift register LSB

With OUT_ZERO additional zeros to be inserted between the user data and the error/warning bit can be

configured. Parameter OUT_ZERO can be used to achieve multiples of 8 bits when sensor data is output through the SPI interface.

| OUT_ZERO(2:0) Addr. 0x11; bit 7:5 | |
|--|-----------------------|
| Code | Description |
| 0x0 | no additional '0' Bit |
| 0x1 | 1 additional '0' Bit |
| ... | ... |
| 0x7 | 7 additional '0'-Bits |

Table 40: Selection of additional ZEROS

The direction of rotation can be inverted with parameter ROT_ALL. The parameter affects the output of the data word through the serial interface in MODE_ST=0x0 and 0x1, the ABZ-interface and the UVW-interface.

| ROT_ALL Addr. 0x15; bit 7 | |
|----------------------------------|--|
| Code | Description |
| 0 | no inversion of direction of rotation |
| 1 | inversion of rotation |
| Note: | no effect in MODE_ST = 2 (raw-data) for the data output through the serial interface |

Table 41: Inversion of the direction of rotation (for MT and ST data)

SSI interface

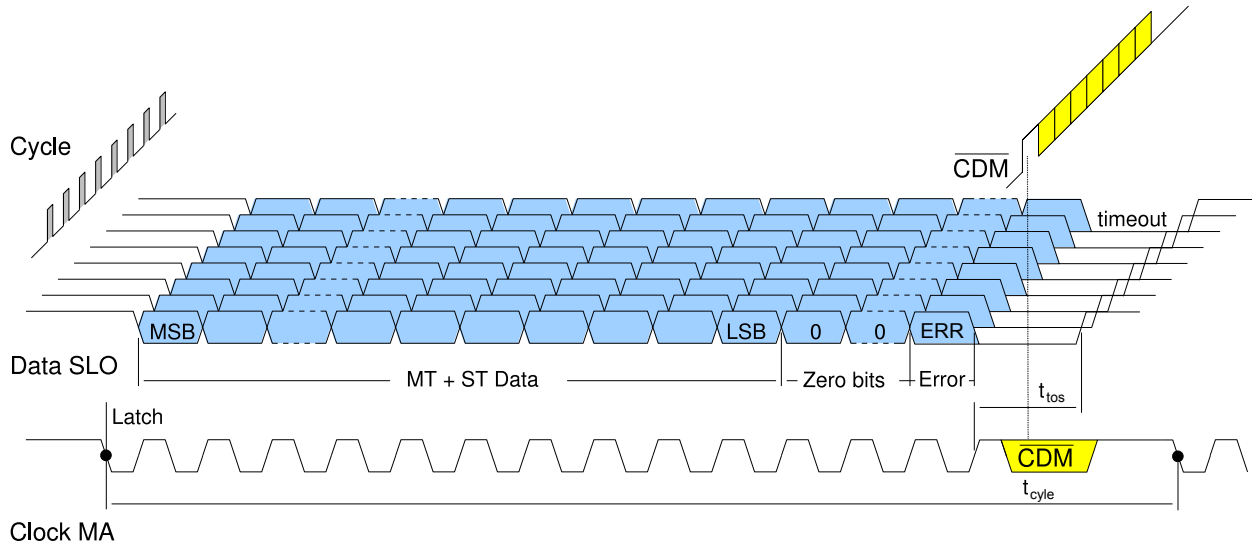


Figure 17: Example of SSI line signals (MODEA=0x5/0x6) with optional unidirectional register communication

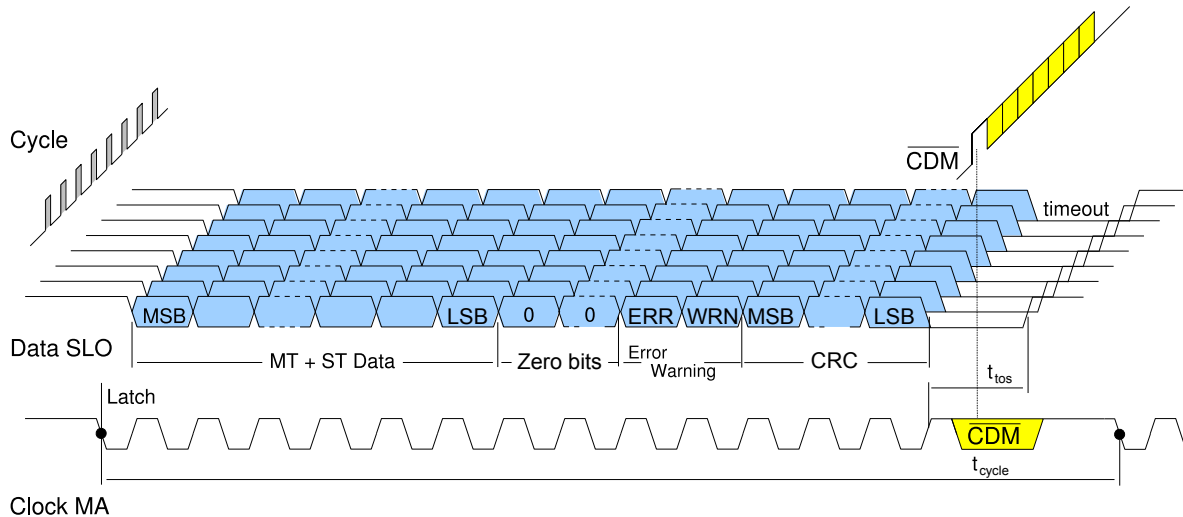


Figure 18: Example of extended SSI line signals (MODEA=0x7, ExtSSI)

| MODEA | |
|-------|--|
| Code | Description |
| 0x4 | Standard SSI, no error-bit |
| 0x5 | Standard SSI, error-bit low active |
| 0x6 | Standard SSI, error-bit high active |
| 0x7 | extended SSI, data-package like BiSS-C |

Table 44: MODEA: SSI

adaptive and the timeout period t_{out} is calculated based on the first MA edges as shown in Figure 6.

In standard SSI mode singleturn data and, optionally, multiturn data, an error, and a stop zero can be transmitted. In extended SSI mode (ExtSSI) the multiturn data (optional), singleturn data, error, warning, and CRC can be read out. All data is sent with the MSB first and is equivalent to the data package that is output through BiSS.

The SSI interface of iC-MU can handle sensor data communication and unidirectional register communication (Advanced SSI protocol see Figure 17). The timeout is

In SSI mode the sensor data can be output in binary or Gray code.

| GSSI ¹ | | Addr. 0x12; bit 7 |
|--------------------------|--------------|-------------------|
| Code | Data format | |
| 0 | binary coded | |
| 1 | Gray coded | |

Table 45: Data format (for MT and ST data)

SSI interface ring operation can be activated for the repeated output of position data in SSI protocol. In this mode position data output is repeated cycle by cycle separated by a zero-bit until the internal timeout t_{tos} (p. 13) is reached. After t_{tos} has elapsed a new request can

be made for position data. By checking the repeated position data for equality, SSI ring operation mode enables any possible transmission errors to be detected. If RSSI is deactivated zeros are subsequently output after the position data output.

| RSSI | | Addr. 0x12; bit 6 |
|-------------|----------------|-------------------|
| Code | Ring operation | |
| 0 | normal output | |
| 1 | Ring operation | |

Table 46: Ring operation

¹ Please refer to the design review on p. 66.

SPI Interface: general description

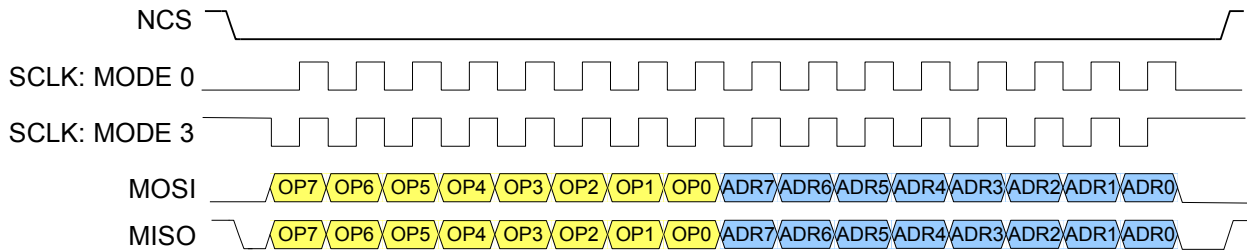


Figure 19: SPI transmission SPI-Mode 0 and 3, using opcode Read REGISTER(single) as an example

| MODEA | |
|-------|--------------------|
| Code | Description |
| 0x0 | SPI _{TRI} |
| 0x1 | SPI |

Table 47: MODEA: SPI

In mode SPI_{TRI} MISO (Pin PA3) is set to tristate if the slave is not selected by the master, i.e. NCS=1. This function is used for a parallel SPI bus configuration (Figure 20). In mode SPI the idle state of MISO (Pin PA3) is high if the slave is not selected by the master.

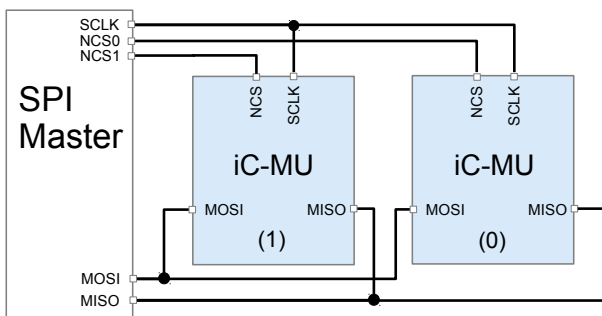


Figure 20: Example configuration SPI bus with 2 parallel Slaves

SPI modes 0 and 3 are supported, i.e. idle level of SCLK 0 or 1, acceptance of data on a rising edge. Data is sent in packages of 8 bits and with the MSB first (see Figure 19). Each data transmission starts with the master sending an opcode (Table 48) to the slave.

The following describes the typical sequence of an SPI data transmission, taking the command **Read REGISTER (single)** as an example (see Figure 19):

1. The master initializes a transmission with a falling edge at NCS.
2. iC-MU passes the level on from MOSI to MISO.

3. The master transmits the opcode OP and address ADR via MOSI; iC-MU immediately outputs OP and ADR via MISO.
4. The master terminates the command with a rising edge at NCS.
5. iC-MU switches its MISO output to 1 (MODEA=0x1) or tristate (MODEA=0x0).

| OPCODE | |
|--------|--------------------------------------|
| Code | Description |
| 0xB0 | ACTIVATE |
| 0xA6 | SDAD-transmission (sensor data) |
| 0xF5 | SDAD Status (no latch) |
| 0x97 | Read REGISTER(single) ² |
| 0xD2 | Write REGISTER (single) ² |
| 0xAD | REGISTER status/data |

Table 48: SPI OPCODEs

For the setup to be compatible with SPI protocol, when setting the sensor data length for the command "SDAD transmission" with parameters OUT_MSB, OUT_LSB, and OUT_ZERO, it must be ensured that the output data length is a multiple of 8 bits.

SPI Interface: Command ACTIVATE

Each iC-MU has one RACTIVE and one PACTIVE register. These registers are used pairwise to configure the register data channel and the sensor/actuator data channel of a slave.

Using the **ACTIVATE** command, the register and sensor data channels of the connected slaves can be switched on and off. The command causes all slaves to switch their RACTIVE and PACTIVE registers between MOSI and MISO and set them to 0 (slaves in daisy chain connection, Figure 23). The register and

² Please refer to the design review on p. 66.

sensor/actuator data channels can be switched on and off with data bytes following the OPCODE.

After startup of iC-MU RACTIVE and PACTIVE is set to 1.

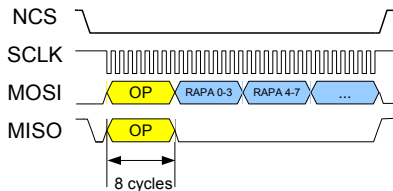


Figure 21: Set ACTIVATE: RACTIVE/PACTIVE (several slaves)

The **ACTIVATE** command resets the bits FAIL, VALID, BUSY, and DISMISS in the SPI-STATUS byte (see Table 52).

| RACTIVE | |
|---------|------------------------------------|
| Code | Description |
| 0 | Register communication deactivated |
| 1 | Register communication activated*) |
| Note | *) default after startup |

Table 49: RACTIVE

If RACTIVE is not set, on commands **Read REGISTER (single)**, **Write REGISTER (single)**, **REGISTER status/data** the ERROR bit is set in the SPI-STATUS byte (see Table 52) to indicate that the command has not been executed. At MISO the slave immediately outputs the data transmitted by the master via MOSI.

| PACTIVE | |
|---------|---------------------------------|
| Code | Description |
| 0 | Sensor data channel deactivated |
| 1 | Sensor data channel activated*) |
| Note | *) default after startup |

Table 50: PACTIVE

If PACTIVE is not set, on commands **SDAD status** and **SDAD transmission** the ERROR bit is set in the SPI-STATUS byte (see Table 52) to indicate that the command has not been executed. At MISO the slave immediately outputs the data transmitted by the master via MOSI.

If only one slave is connected up with one register and one sensor data channel, it must be ensured that the RACTIVE and PACTIVE bits come last in the data byte.

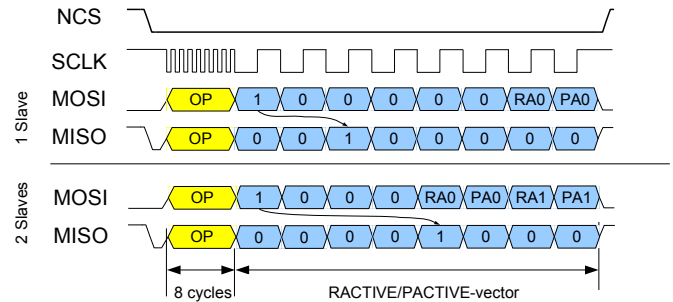


Figure 22: Set ACTIVATE: RACTIVE/PACTIVE (Example with one and two slaves (daisy chain))

An example for a daisy chain wiring of 2 SPI slaves is given in Figure 23. In order to do register communication (**Read REGISTER (single)**, **Write REGISTER (single)**, **REGISTER status/data**) with e.g. slave (1) the register communication has to be enabled explicitly for this slave and disabled for slave (0) with command **ACTIVATE** and parameter **RACTIVE**.

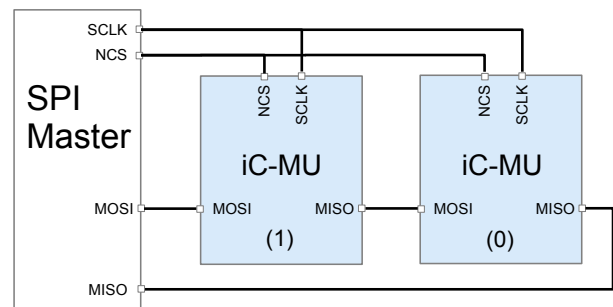


Figure 23: Example configuration with 2 Slaves (daisy chain)

SPI interface: Command SDAD transmission

iC-MU latches the absolute position on the first rising edge at SCLK, when NCS is at zero (e.g. Figure 24 LATCH). Because iC-MU can output the sensor data (SD) immediately, the master can transmit the **SDAD transmission** command directly. The sensor data shift register (the size of which is 8 to 40 bits in multiples of 8 using iC-MU) is switched and clocked out between MOSI and MISO.

If invalid data is sampled in the shift register, the ERROR bit is set in the SPI-STATUS byte (see Table 52) and the output data bytes are set to zero.

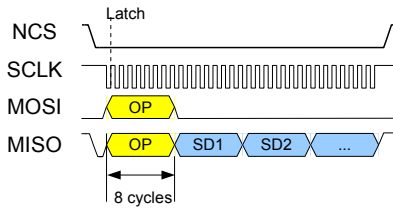


Figure 24: SDAD transmission: read SD

Note: iC-MU latches the absolute position on the first rising edge at SCLK, when NCS is at zero (e.g. Figure 24 - LATCH).

SPI interface: Command SDAD status

If the master does not know the processing time of the connected slaves, it can request sensor data using the command **SDAD status**. The command causes:

1. All slaves activated via PACTIVE to switch their SVALID register between MOSI and MISO.
2. The next request for sensor data started with the first rising edge at SCLK of the next SPI communication is ignored by the slave.

The end of conversion is signaled by SVALID (SV). Using this command, the master can poll to the end of conversion. The sensor data is read out via the command **SDAD transmission**.

| SVALID | |
|--------|---------------------|
| Code | Description |
| 0 | Sensor data invalid |
| 1 | Sensor data valid |

Table 51: SVALID

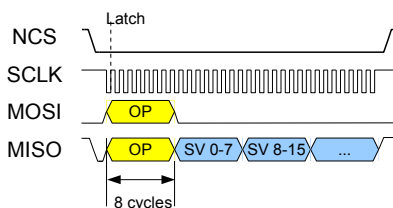


Figure 25: SDAD status

If only one slave is connected, the corresponding SVALID bit (SV0) is placed at bit position 7 in the SVALID byte.

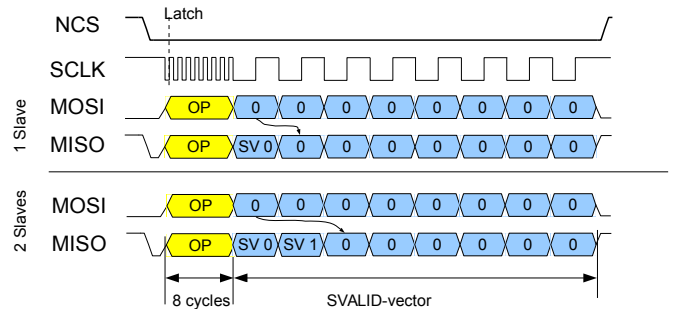


Figure 26: SDAD status (Example with one and two slaves)

Figure 27 shows the interaction of the two commands **SDAD Status** and **SDAD transmission**. It is not necessary to start each sensor data communication with the command **SDAD Status** (1). iC-MU has no processing time and can therefore directly output valid sensor data. Because of that the command sequence can start with **SDAD-transmission** (2). Following this, the command **REGISTER status/data** should be executed to detect an unsuccessful SPI communication.

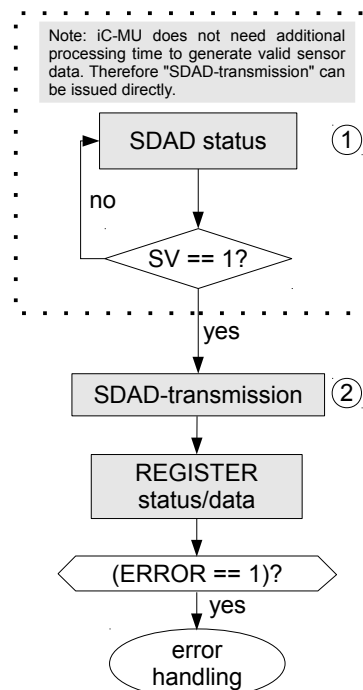


Figure 27: Example sequence of the commands SDAD Status/SDAD-transmission

SPI interface: Command Read REGISTER (single)

This command enables register data to be read out from the slave byte by byte.

The master first transmits the **Read REGISTER (single)** command and then address ADR. The slave immediately outputs the command and address at MISO.

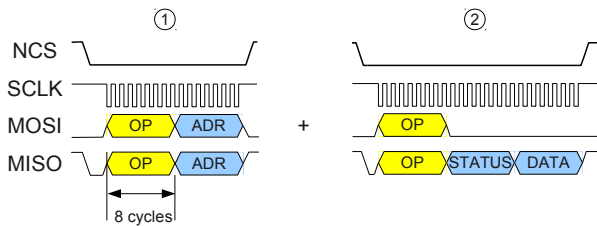


Figure 28: Read REGISTER (single): set the read address (1) + command REGISTER status/data to read-out data (2)

Following this, using the **REGISTER status/data** command (see page 38) the master can poll until the validity of the DATA following the SPI-STATUS byte is signaled via SPI-STATUS.

SPI interface: Command Write REGISTER (single)
This command enables data to be written to the slave byte by byte.

The master first transmits the **Write REGISTER (single)** command and then address ADR and the data (DATA). The slave immediately outputs the command, address, and data at MISO.

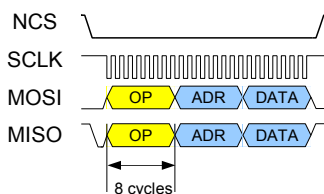


Figure 29: Write REGISTER (single); set write address and data

Using the **REGISTER status/data** command, the master can poll to the end of the register communication (signaled via the SPI-STATUS byte).

SPI interface: Command REGISTER status/data

The **REGISTER status/data** command can be used to request the status of the last register communication and/or the last data transmission. The SPI-STATUS byte contains the information summarized in Table 52.

| SPI-STATUS | | |
|---|------------------------------------|--|
| Bit | Name | Description of the status report |
| Status bits of the SDAD and register communication | | |
| 7 | ERROR | Opcode not implemented, Sensor data was invalid on readout |
| 6..4 | - | Reserved |
| Status bits of the register communication only | | |
| 3 | DISMISS | Address rejected |
| 2 | FAIL | Data request has failed |
| 1 | BUSY | Slave is busy with a request |
| 0 | VALID | DATA is valid |
| Note | Display logic: 1 = true, 0 = false | |

Table 52: Communication status byte

All SPI status bits are updated with each register access. The exception to the rule is the ERROR bit; this bit indicates whether an error occurred during the last SPI-communication with the slave.

The master transmits the **REGISTER status/data** opcode. The slave immediately passes the opcode on to MISO. The slave then transmits the SPI-STATUS byte and a DATA byte.

Following the commands **Read REGISTER (single)** and **Write REGISTER (single)**, the validity of the DATA byte is signaled with the VALID status bit.

The requested data byte is returned via DATA following the **Read REGISTER (single)** command. Following the **Write REGISTER (single)** command, the data to be written is repeated in the DATA byte. With all other opcodes, the DATA byte is not defined.

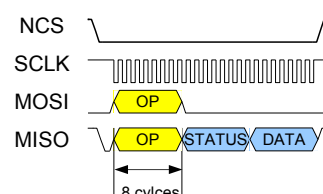


Figure 30: REGISTER status/data

Figure 31 shows the interaction of the commands **REGISTER read/write** and **REGISTER status/data**.

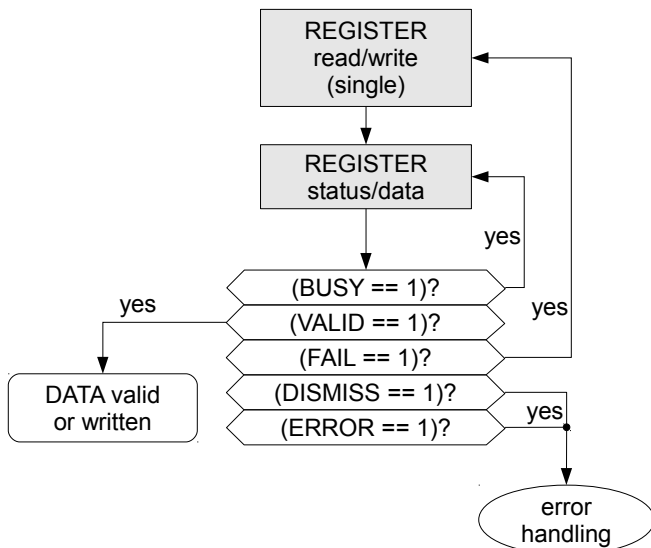


Figure 31: Example sequence of commands REGISTER read/write and REGISTER status/data

CONVERTER AND NONIUS CALCULATION

Converter principle

The system consist of two real-time tracking converters, each with a resolution of 12 bits for the master track and nonius track. Above the maximal permissible input frequency the status bits FRQ_CNV is set. The tracking converter can't follow the input signal any more. With a filter setting of type FILT1 and bigger an increased resolution of 14 bits is available.

A digital filter can be configured with FILT to reduce the noise of the digital output signals. Using this the digital angle values of the tracking converter can be filtered.

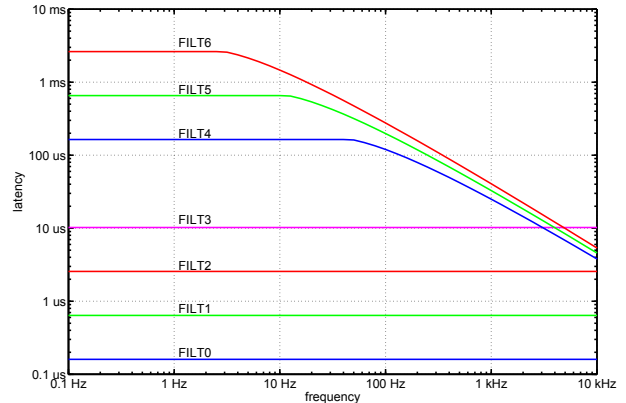


Figure 33: Filter latency

Synchronization mode

Table 54 lists the configurable master period counts and the resulting bit lengths for nonius synchronization, and the synchronization bit length used. The parameter MPC defines thus the nonius system and has to be chosen according to the magnetic code carrier. If MPC is switched during operation, command ABS_RESET must be executed and the track offset values must be calibrated again.

| FILT Addr. 0x0E; bit 2:0 | | | | |
|--------------------------|---|-------------------|---|-------------------|
| Code | Type | Noise suppression | Latency (see Figure 33) | Interpol. MAS/NON |
| 0x0 | FILT0 | 0 dB | < 1 μs | 12 bit |
| 0x1 | FILT1 | 15 dB | < 1 μs | 14 bit |
| 0x2 | FILT2 | 21 dB | 2.5 μs | 14 bit |
| 0x3 | FILT3 | 27 dB | 10 μs | 14 bit |
| 0x4 | FILT4 | 39 dB | $f_{sin} < 50 \text{ Hz}$: 164 μs $f_{sin} = 1 \text{ kHz}$: 25 μs | 14 bit |
| 0x5 | FILT5 | 45 dB | $f_{sin} < 12 \text{ Hz}$: 650 μs $f_{sin} = 1 \text{ kHz}$: 33 μs | 14 bit |
| 0x6 *) | FILT6 | 51 dB | $f_{sin} < 3 \text{ Hz}$: 2.6 ms $f_{sin} = 1 \text{ kHz}$: 41 μs | 14 bit |
| Note | Influences on the max. rotation speed with incremental output signals are shown in table 80 *) Please refer to "DESIGN REVIEW", item no. 8 | | | |

Table 53: Digital filter features

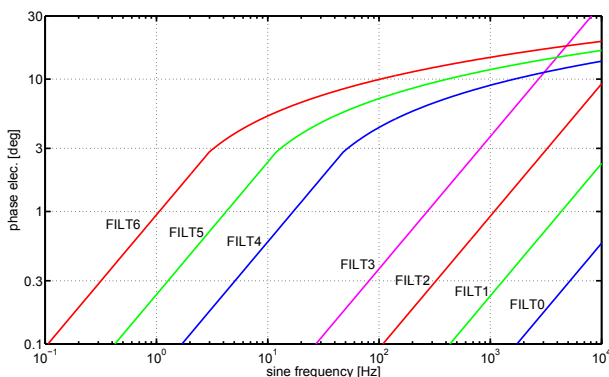


Figure 32: Phase relationship of the filters

| MPC(3:0) Addr. 0x0F; bit 3:0 | | | | | |
|-------------------------------|---------------------|---------------------|------------|------------------------------|-----------------------------------|
| Code | Master period count | Nonius period count | Bit length | Syn-chroni-sation bit length | Maximum absolute resolution [bit] |
| 0x4 | 16 | 15 | 4 | 8 | 18 |
| 0x5 | 32 | 31 | 5 | 7 | 19 |
| 0x6 | 64 | 63 | 6 | 6 | 20 |
| for MU as Nonius-Multiturn *) | | | | | |
| 0x7 | 128 | 127 | 7 | 5 | 21 |
| 0x8 | 256 | 255 | 8 | 4 | 22 |
| 0x9 | 512 | 511 | 9 | 3 | 23 |
| 0xA | 1024 | 1023 | 10 | 2 | 24 |
| 0xB | 2048 | 2047 | 11 | 1 | 25 |
| 0xC | 4096 | 4095 | 12 | 0 | 26 |
| Note | *) see page 46 | | | | |

Table 54: Master period count and the resulting bit lengths

LIN selects the hall sensor arrangement to linear or rotative for axial or radial/linear scanning (see table 55).

| LIN Addr. 0x0E; bit 4 | | |
|-----------------------|-------------------------|---|
| Code | Hall sensor arrangement | Type of target magnetization |
| 0 | Rotative | Axial (e.g. MU2S 30-32N) |
| 1 | Linear | Radial (e.g. MU7S 25-32N) or Linear (e.g. MUxL) |

Table 55: Selection of linear/rotative hall sensors

An offset between the nonius track and the master track within one revolution can be adjusted with SPO_BASE and SPO_x (x=0-14) .

The following formula describes how the error curve based on the raw data from the master and nonius track can be calculated. 2^{MPC} is the number of sine periods of the measuring distance.

$$TOL_{SPON} = RAW_{MASTER} - RAW_{NONIUS} * \frac{2^{MPC}}{2^{MPC} - 1}$$

The maximum tolerable phase deviation for a 2-track nonius system is shown in Table 56. For the tolerable phase deviation of a 3-track nonius system please refer to Table 70 page 46.

| Periods/revolution | | Permissible Max. Phase Deviation [given in degree per signal period of 360°] Master ↔ Nonius |
|--------------------|--------|--|
| Master | Nonius | |
| 16 | 15 | +/- 9.84° |
| 32 | 31 | +/- 4.92° |
| 64 | 63 | +/- 2.46° |

Table 56: Tolerable phase deviation for the master versus the nonius track of a 2 track nonius system (with reference to 360°, electrical)

Note: The lower the maximum permissible phase deviation, the higher the demands on the mechanical system design and the quality of the magnetic target.

An offset correction curve can be specified with SPO_BASE and SPO_x (x= 0-14). SPO_BASE is the start-value. SPO_0 to SPO_14 can be interpreted as slope-values. A change in the slope of the offset function can be made each 22.5°. The slope value SPO_15 is computed automatically by iC-MU. To do this the following condition must be met:

$$\sum_{x=0}^{14} SPO_x = \{-7 \dots 7\}$$

The offset value between two slopes (e.g. SPO_0 and SPO_1) is interpolated. The computed offset is added

to the converted result of the nonius track prior to synchronization and is used to calibrate the nonius to the master track. An offset value is chosen by the absolute position given by the nonius difference (master-nonius).

| SPO_BASE(3:0) Addr. 0x19; bit 3:0 | |
|---------------------------------------|---|
| SPO_BASE(3:0) Addr. SER:0x52; bit 3:0 | |
| Code | Starting point referred to 1 revolution |
| 0x0 | 0 * (22.5°/2 ^{MPC}) |
| ... | ... |
| 0x7 | 7 * (22.5°/2 ^{MPC}) |
| 0x8 | -8 * (22.5°/2 ^{MPC}) |
| 0x9 | -7 * (22.5°/2 ^{MPC}) |
| ... | ... |
| 0xF | -1 * (22.5°/2 ^{MPC}) |

Table 57: Nonius track offset start value

| SPO_0(3:0) | Addr. 0x19; bit 7:4 | Addr. SER: 0x52 |
|-------------|---|-----------------|
| SPO_1(3:0) | Addr. 0x1A; bit 3:0 | Addr. SER: 0x53 |
| SPO_2(3:0) | Addr. 0x1A; bit 7:4 | Addr. SER: 0x53 |
| SPO_3(3:0) | Addr. 0x1B; bit 3:0 | Addr. SER: 0x54 |
| SPO_4(3:0) | Addr. 0x1B; bit 7:4 | Addr. SER: 0x54 |
| SPO_5(3:0) | Addr. 0x1C; bit 3:0 | Addr. SER: 0x55 |
| SPO_6(3:0) | Addr. 0x1C; bit 7:4 | Addr. SER: 0x55 |
| SPO_7(3:0) | Addr. 0x1D; bit 3:0 | Addr. SER: 0x56 |
| SPO_8(3:0) | Addr. 0x1D; bit 7:4 | Addr. SER: 0x56 |
| SPO_9(3:0) | Addr. 0x1E; bit 3:0 | Addr. SER: 0x57 |
| SPO_10(3:0) | Addr. 0x1E; bit 7:4 | Addr. SER: 0x57 |
| SPO_11(3:0) | Addr. 0x1F; bit 3:0 | Addr. SER: 0x58 |
| SPO_12(3:0) | Addr. 0x1F; bit 7:4 | Addr. SER: 0x58 |
| SPO_13(3:0) | Addr. 0x20; bit 3:0 | Addr. SER: 0x59 |
| SPO_14(3:0) | Addr. 0x20; bit 7:4 | Addr. SER: 0x59 |
| Code | Slope referred to 1 revolution | |
| 0x0 | 0 * (22.5°/2 ^{MPC}) | |
| ... | ... | |
| 0x7 | 7 * (22.5°/2 ^{MPC}) | |
| 0x8 | -8 * (22.5°/2 ^{MPC}) | |
| 0x9 | -7 * (22.5°/2 ^{MPC}) | |
| ... | ... | |
| 0xF | -1 * (22.5°/2 ^{MPC}) | |
| Note | $\sum_{x=0}^{14} SPO_x = \{-7 \dots 7\} * (22.5°/2^{MPC})$ | |

Table 58: Nonius track offset slopes

| SPO_15(3:0) Addr. SER:0x5A; bit 3:0 | |
|-------------------------------------|--|
| Code | Slope |
| 0x0 | - |
| ... | is automatically computed: $-\sum_{x=0}^{14} SPO_x$ |
| 0xF | - |
| Note | internal register, not readable via serial interface |

Table 59: Nonius track offset slope (is automatically computed)

The principle is shown in Figure 34. The red curve corresponds to the error curve of the nonius difference absolute within 360°. By taking the blue marked SPO_x curve it is shown, that the nonius difference can be changed in a way that the resulting green curve is in the valid synchronisation range. It can be seen that an error within 22.5° (in the Figure between 67.5° and 90°) can not be corrected. For SPO_0 the range of a possible slope change is exemplary shown.

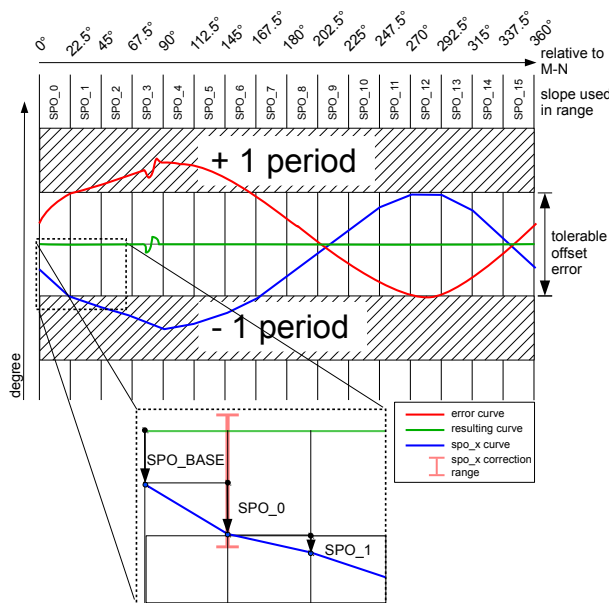


Figure 34: Nonius track offset calibration

Following the first nonius synchronization the number of exceeded periods is counted and output. Using NCHK_NON the system can be configured to check the internal period counter against the period given by the code disc at regular intervals. Command NON_VER explicitly requests nonius verification. If an error is found during verification of the nonius, bit NON_CTR is set in status register STATUS1.

Figure 35 describes the principle of nonius synchronization with verification, with φ representing the respective digitized angle of the relevant track.

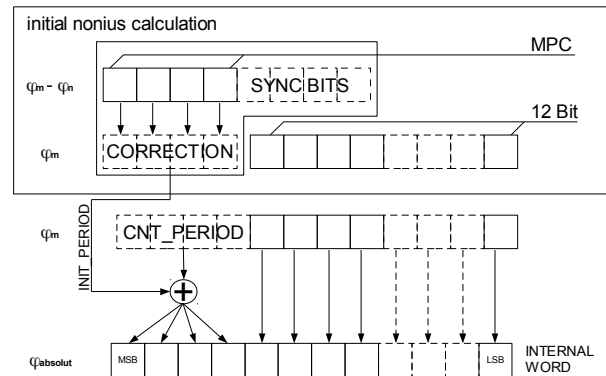


Figure 35: Principle of nonius synchronization

| NCHK_NON | | Addr. 0x0D; bit 5 |
|----------|---|-------------------|
| Code | Description | |
| 0 | automatic period verification | |
| 1 | no automatic period verification | |
| Notes: | For max. duration of the internal cyclic checks see elec. char. no. 408 | |

Table 60: Automatic nonius period verification

The nonius data and incremental interface can be automatically reset with ACRM_RES if the master amplitude is too low. The incremental section is reset as soon as the amplitude control unit indicates that the master amplitude is too low (AM_MIN occurs, see Table 98). The ABZ-interface shows position 0 as default. When the master amplitude is again in its set range, a new nonius calculation is carried out and the incremental section is restarted.

| ACRM_RES | | Addr. 0x0D; bit 4 |
|----------|------------------------|-------------------|
| Code | Description | |
| 0 | no automatic reset | |
| 1 | automatic reset active | |

Table 61: Automatic Reset triggered by AM_MIN

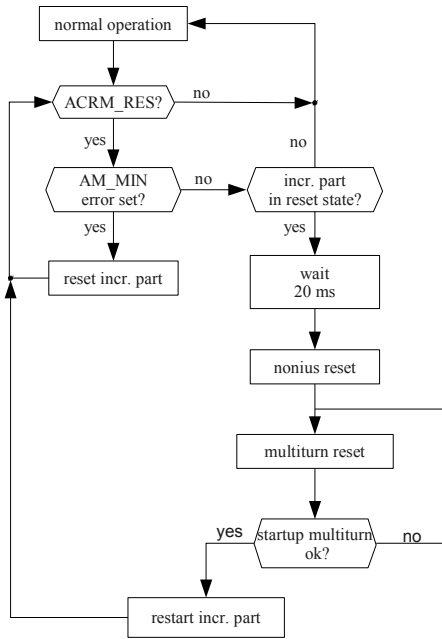


Figure 36: Automatic reset ACRM_RES

MT INTERFACE

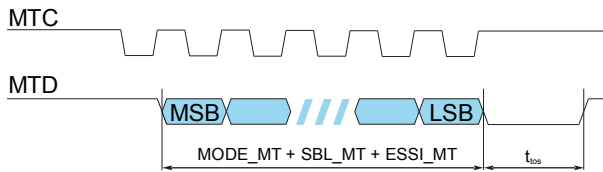


Figure 37: Example of multiturn SSI line signals

Configuration of the Multiturn interface

iC-MU can read and synchronize binary data from an external SSI sensor through the serial multiturn interface. On startup the first data value read in determines the start value of the internal MT counter. After startup the multiturn counter counts the ST cycles. If there is an error reading the external multiturn during startup, the read-in will be repeated.

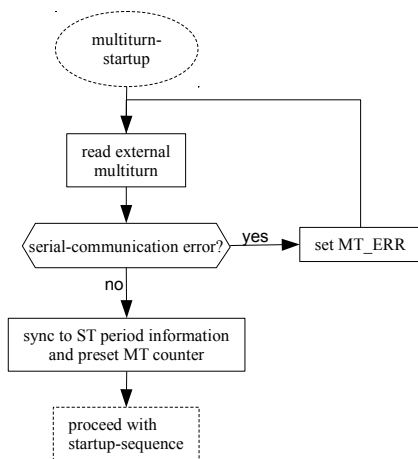


Figure 38: Error handling during startup

If the MT interface is not used (MODE_MT = 0x0), the internal 24-bit MT counter can extend the singleturn information to include the counted ST cycles. To access the internal MT counter increase parameter OUT_MSB accordingly.

For exclusive multiturn systems a 4, 8, 12, 16 or 18-bit multiturn data value can be read in (MODE_MT = 0xB-0xE).

There is also the possibility to interpret a part of the external multiturn data value as singleturn data (MODE_MT = 0x1-0xA). This influences the incremental output signals, UVW commutation signals and data output in MODE_ST = 0x01 (FlexCount®). For further information see **Construction of a Multiturn system with two iC-MU** p. 46.

| MODE_MT(3:0) | | Addr. 0x10; bit 3:0 | |
|--------------|---|---------------------|---------------|
| Code | Function | Code | Function |
| 0x0 | no external data | 0x8 | 4 *) + 12 bit |
| 0x1 | 1 *) bit | 0x9 | 5 *) + 12 bit |
| 0x2 | 2 *) bit | 0xA | 6 *) + 12 bit |
| 0x3 | 3 *) bit | 0xB | 4 bit |
| 0x4 | 4 *) bit | 0xC | 8 bit |
| 0x5 | 5 *) bit | 0xD | 12 bit |
| 0x6 | 6 *) bit | 0xE | 16 bit |
| 0x7 | 3 *) + 12 bit | 0xF | 18 bit |
| Notes: | *) data interpreted as ST If MPC ≥ 0x07 than MODE_MT has to be set to 0x0 or 0xD | | |

Table 62: MT interface operating mode

For synchronization a synchronization bit length must be set with SBL_MT. Synchronization takes place between the external multiturn data read in and the ST period information counted internally (see Fig. 40). Synchronization can take place automatically within the relevant phase tolerances.

| SBL_MT(1:0) | | Addr. 0x10; bit 5:4 | |
|-------------|-------------------------------|---|--|
| Code | MT synchronisation bit length | synchronisation tolerance (ST-resolution) | |
| 0x0 | 1 bit | ± 90° | |
| 0x1 | 2 bit | ± 90° | |
| 0x2 | 3 bit | ± 135° | |
| 0x3 | 4 bit | ± 157.5° | |

Table 63: MT synchronization bit length

Figure 39 shows the principle of a 2 bit MT synchronization for ideal signals (without indication of synchronization tolerance limits).

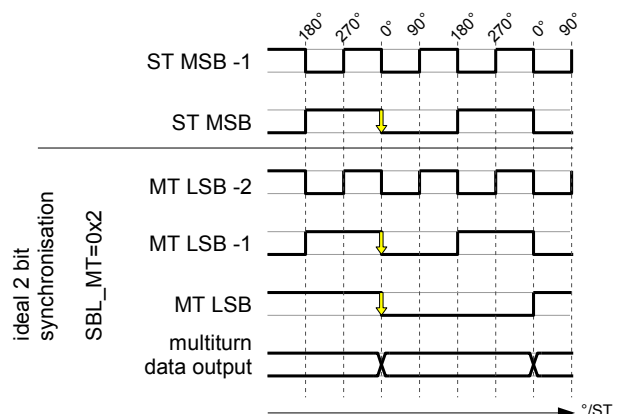


Figure 39: Principle of 2 bit MT synchronization

The direction of rotation of the read multiturn data can be inverted using parameter ROT_MT.

| ROT_MT | | Addr. 0x0E; bit 5 |
|--------|--------------------------------|-------------------|
| Code | Function | |
| 0 | no inversion of code direction | |
| 1 | inversion of code direction | |

Table 64: Inverted direction of rotation of external multiturn

The parameter ESSI_MT configures the evaluation of an optional error-bit send by the external multiturn device.

| ESSI_MT | | Addr. 0x0E; bit 7:6 |
|---------|-------------------------|---------------------|
| Code | Function | |
| 0x0 | no error bit | |
| 0x1 | 1 error-bit low active | |
| 0x2 | reserved | |
| 0x3 | 1 error-bit high active | |

Table 65: Evaluation of an error-bit of the external multiturn

The SSI parity and warning bit are not supported by iC-MU and need to be deactivated in the external multiturn sensor.

The total data length of the external read multiturn data word is determined by:

$$\text{data_length_ext_mt} = \text{Bits}(\text{MODE_MT}) + \text{Bits}(\text{SBL_MT}) + \text{Bits}(\text{ESSI_MT})$$

The parameter SPO_MT allows to balance an existing static offset between the singleturn and the multiturn. The offset is added before the synchronization of the read multiturn data (see Fig. 40).

| SPO_MT | | Addr. 0x0F; bit 7:4 |
|--------|------------------|---------------------|
| Code | Function | |
| 0x0 | multiturn offset | |
| ... | | |
| 0xF | | |

Table 66: Offset of external multiturn

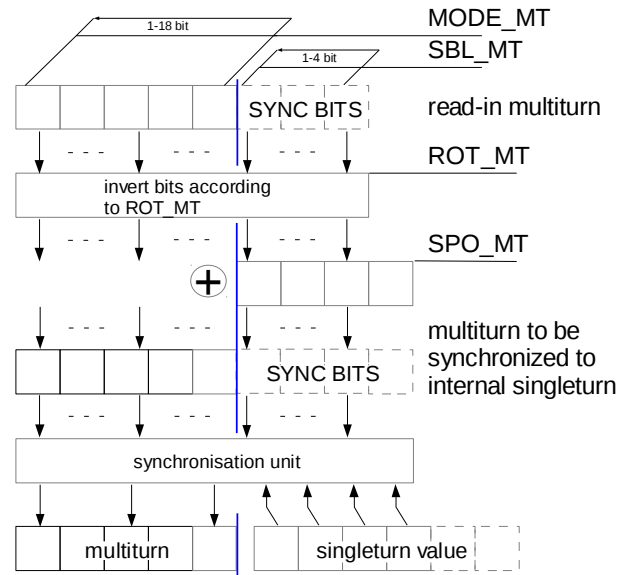


Figure 40: Parameters to configure external multiturn

CHK_MT can be used to verify the counted multiturn at regular intervals. Verification can also be requested using command MT_VER. A multiturn verification error (comparison of the internal MT counter with the external multiturn data) is reported on status bit MT_CTR.

| CHK_MT | | Addr. 0x10; bit 6 |
|--------|---|-------------------|
| Code | Function | |
| 0 | no verification | |
| 1 | periodical verification | |
| Notes: | For max. duration of the internal cyclic checks see Elec. Char. no. 408 | |

Table 67: Multiturn verification

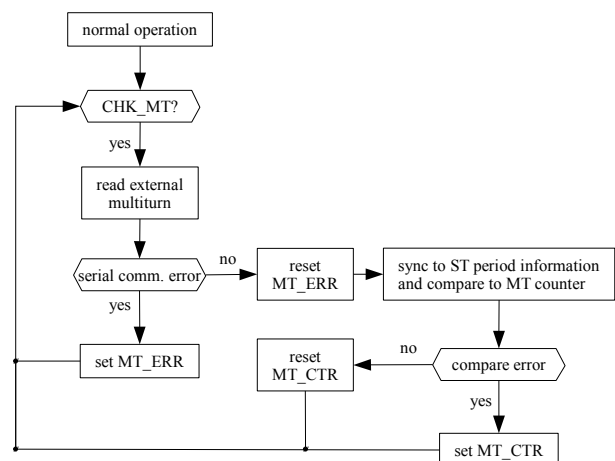


Figure 41: Error handling in normal operation with cyclic verification of the period counter

iC-MU MAGNETIC OFF-AXIS POSITION ENCODER - POLE WIDTH 1.28MM



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Construction of a Multiturn system with two iC-MU

A 3 track nonius system can be build using two iC-MU. The singleturn iC-MU (1) can be configured to interpret 3, 4, 5, or 6 bits of the read multiturn data as singleturn data (ST) (see Table 62). The output through the incremental interface, the UVW interface and the serial interface in MODE_ST = 0x1 (FlexCount) of iC-MU (1) is then absolute with this additional information.

The construction of such a system is shown as an example in Figure 42 and the configuration in Table 68.

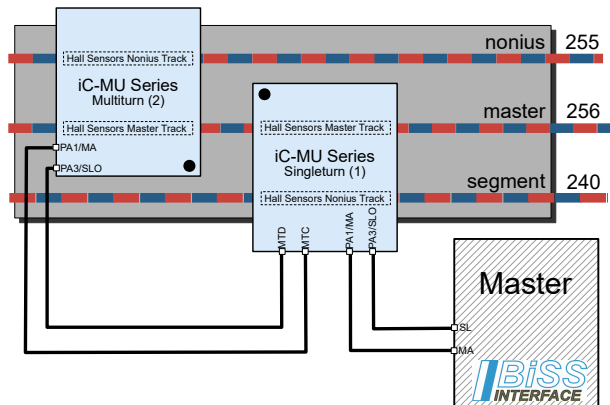


Figure 42: 3-track nonius with 2 iC-MU

Table 69 shows the possible settings for a 3-track nonius systems with 2 iC-MU and the resulting periods/revolution of the tracks. The maximum phase deviation of the tracks is summarized in Table 70.

| Master Periods | 128 | 256 | 512* | 1024* |
|---|-------|-------|-------|-------|
| iC-MU (1): singleturn | | | | |
| Parameter | Value | Value | Value | Value |
| MPC | 0x04 | 0x04 | 0x05 | 0x05 |
| MODE_MT | 0x03 | 0x04 | 0x04 | 0x05 |
| SBL_MT | 0x03 | 0x03 | 0x03 | 0x03 |
| ROT_MT | 0x01 | 0x01 | 0x01 | 0x01 |
| NCHK_NON | 0x00 | 0x00 | 0x00 | 0x00 |
| CHK_MT | 0x01 | 0x01 | 0x01 | 0x01 |
| ESSI_MT | 0x01 | 0x01 | 0x01 | 0x01 |
| LIN | 0x01 | 0x01 | 0x01 | 0x01 |
| OUT_LSB | 0x00 | 0x00 | 0x00 | 0x00 |
| OUT_MSB | 0x07 | 0x08 | 0x09 | 0x0A |
| iC-MU (2): multiturn | | | | |
| Parameter | Value | Value | Value | Value |
| MPC | 0x07 | 0x08 | 0x09 | 0x0A |
| MODE_MT | 0x00 | 0x00 | 0x00 | 0x00 |
| MODE_ST | 0x00 | 0x00 | 0x00 | 0x00 |
| ROT_ALL | 0x00 | 0x00 | 0x00 | 0x00 |
| NCHK_NON | 0x01 | 0x01 | 0x01 | 0x01 |
| GSSI | 0x00 | 0x00 | 0x00 | 0x00 |
| MODEA | 0x05 | 0x05 | 0x05 | 0x05 |
| LIN | 0x01 | 0x01 | 0x01 | 0x01 |
| OUT_LSB | 0x0F | 0x0F | 0x0F | 0x0F |
| OUT_MSB | 0x07 | 0x08 | 0x09 | 0x0A |
| OUT_ZERO | 0x01 | 0x01 | 0x00 | 0x00 |
| *) For 512 and 1024 master period systems an ABS_RESET command must be applied to finalize the encoder start-up sequence. | | | | |

Table 68: Configuration example for the 3-track nonius systems of 128, 256, 512 and 1024 master periods

| MPC (2) | (1) | Periods/revolution | | | ST Periods [Bit] | |
|---------|-----|--------------------|-------|--------|------------------|------------|
| | | Master | Segm. | Nonius | from MT(2) | from ST(1) |
| 0x7 | 0x4 | 128 | 120 | 127 | 3 | 4 |
| 0x8 | 0x4 | 256 | 240 | 255 | 4 | 4 |
| 0x9 | 0x5 | 512 | 496 | 511 | 4 | 5 |
| 0xA | 0x5 | 1024 | 992 | 1023 | 5 | 5 |
| 0xB | 0x6 | 2048 | 2016 | 2047 | 5 | 6 |
| 0xC | 0x6 | 4096 | 4032 | 4095 | 6 | 6 |

Table 69: Settings for a 3-track nonius system using 2 iC-MU

| Periods/revolution | | | Permissible Max. phase deviation [given in degree per signal period of 360°] | |
|--------------------|--------------------|--------|---|-----------------------|
| Master | Segm. | Nonius | Master ↔ Segm. (1) | Master ↔ Non.* (2) |
| 128 | 120 | 127 | +/-9.84° | +/-19.68° |
| 256 | 240 | 255 | +/-9.84° | +/-9.84° |
| 512 | 496 | 511 | +/-4.92° | +/-9.84° |
| 1024 | 992 | 1023 | +/-4.92° | +/-4.92° |
| 2048 | 2016 | 2047 | +/-2.46° | +/-4.92° |
| 4096 | 4032 | 4095 | +/-2.46° | +/-2.46° |
| Note | *) with SBL_MT=0x3 | | | |

Table 70: Tolerable phase deviation for the master versus the nonius or segment track of a 3-track nonius system (with reference to 360°, electrical)

Note: The lower the maximum permissible phase deviation, the higher the demands on the mechanical system design and the quality of the magnetic target.

Figure 43 shows the principle of the synchronisation of the data from iC-MU (2) to iC-MU (1).

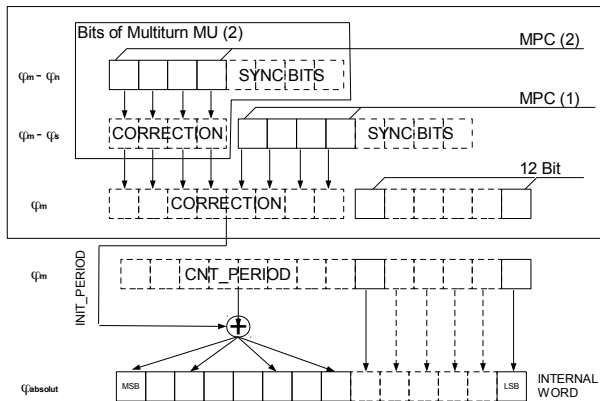


Figure 43: Principle of the synchronisation of a 3-track nonius system using 2 iC-MU without further multitrurn data

To facilitate the initial configuration of an iC-MU as a SSI multitrurn device the command SWITCH can be used (see page 60). The singleturn iC-MU (1) in Figure 42 has to enable the direct communication to the multitrurn sensor by setting GET_MT to 1. The configuration of iC-MU (2) can take place using the BiSS protocol. After the configuration of the external multitrurn MODEA_NEW and RPL_NEW are used to set the target configuration of MODEA and RPL. After that the command SWITCH is executed. By reading STATUS1 it is possible to control if there was an error while executing the command. After the next startup or after the execution of the command SOFT_RESET iC-MU starts with the interface configured with MODEA_NEW and RPL_NEW.

MT Interface Daisy Chain

The MT interface daisy chain mode gives direct access to an external multitrurn sensor for calibration purposes.

| MODEA | |
|-------|----------|
| Code | Function |
| 0x2 | BiSS |
| 0x5 | SSI+ERRL |
| 0x6 | SSI+ERRH |
| 0x7 | ExtSSI |

Table 71: MT Interface Daisy Chain: Possible MODEA configuration

Making use of the BiSS Interface bus capabilities, iC-MU can connect the external multitrurn sensor to the BiSS master controller in modes MODEA = 0x02 (BiSS) and MODEA = 0x05-0x07 (SSI with Error bit and ExtSSI; additional condition RSSI = 1) when GET_MT is enabled.

To this end input pin MA (PA1) receiving the BiSS master's clock signal is fed through to output pin MTC and the input pin MTD is activated in place of the input pin SLI (PA2). Upon enabling this mode the single cycle timeout (see Fig. 3) must have elapsed and an additional init command must be carried out by the BiSS master, before it can run the first register communication.

Note: Please see section "DESIGN REVIEW: Notes On Chip Functions" item no. 10.

For $FILT = 0$ a minimum bus idle time of $50 \mu s$ in between BiSS frames is recommended. For $FILT = 1...6$ a minimum bus idle time of $300 \mu s$ in between BiSS frames is recommended.

Note:

Additional condition $RSSI = 1$ when using GET_MT and MODEA = 0x05, 0x06 or 0x07.

Hint:

First set GET_MT then RSSI to activate direct communication to Multitrurn Sensor in SSI modes.

Example: external multitrurn sensor built with iC-MU is connected to the MT interface of a first iC-MU, preparing the singleturn data. With GET_MT enabled, the external multitrurn can then be addressed via BiSS ID 0 and the singleturn via BiSS ID 1. This temporal chain operation simplifies device parametrization during encoder manufacturing.

| GET_MT | | Addr. 0x10; bit 7 |
|--------|--------------------------|-------------------|
| Code | Function | |
| 0 | Disabled | |
| 1 | MT interface daisy chain | |

Table 72: Direct BiSS communication enable for MT sensor via I/O Interface

INCREMENTAL OUTPUT ABZ, STEP/DIRECTION AND CW/CCW

| MODEA | |
|--------|---|
| Code | Description |
| 0x3 | ABZ |
| MODEB | |
| Code | Description |
| 0x0 | ABZ |
| 0x2 | Step/Direction |
| 0x3 | CW/CCW Incremental |
| Notes: | It is not possible to select an incremental interface on MODEA and MODEB simultaneously |

Table 73: MODEA/MODEB: ABZ, step/direction and CW/CCW

The resolution of incremental signals ABZ can be programmed for each singleturn cycle within a range of 4 to 262,144 edges using the internal FlexCount®. The number of master periods which is equivalent to a singleturn cycle is defined by the settings in register MPC (Table 54).

| RESABZ(7:0) | | Addr. 0x13; bit 7:0 | |
|--------------|---|----------------------|--|
| RESABZ(15:0) | | Addr. 0x14; bit 7:0 | |
| Code | Resolution | Interpolation factor | |
| 0x0000 | 4 | 1 | |
| 0x0001 | 8 | 2 | |
| ... | ... | ... | |
| 0xFFFF | 262,144 | 65,536 | |
| Notes: | For non-binary resolutions above 32,768 (0x2000) the relative error increases | | |

Table 74: FlexCount®- Resolution

In linear application the min. increment of the incremental output (FlexCount) can be calculated as follows:

$$\frac{MPC * magnetic\ period}{max.\ resolution\ FlexCount} = min.\ increment\ linear$$

Example with MPC = 0x5 (master period count 32):

$$\frac{32 * 2.56mm}{262144} = 312.5nm$$

Note:

In linear applications the min. increment of 156nm can be read via the serial interfaces for MODE_ST = 0x0 (output absolute position) independent of the selected MPC.

Figure 44 shows the ABZ, step/direction, and CW/CCW signals. The length of a signal A or B cycle is defined

by φ_{360AB} as a range between two rising edges of an A or B signal.

φ_{hys} represents the hysteresis which must be exceeded before further edges are generated at the incremental interface.

Minimum edge distance t_{mtd} is the minimum time which must have elapsed before another event can be output at the incremental interface.

The length of the Z pulse with setting ZLEN = 0x00 is defined by φ_{z90} .

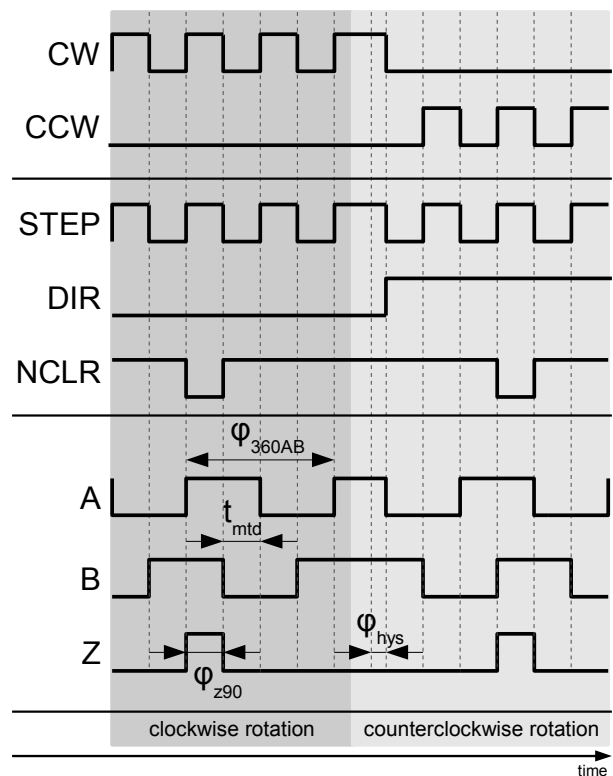


Figure 44: Definition of the ABZ, STEP/DIR, and CW/CCW signals

The phase position of the incremental output signals can be inverted using the relevant configuration bit INV_x (x = A,B,Z).

| INV_A | | Addr. 0x16; bit 2 |
|-------|------------------|-------------------|
| Code | A/STEP/CW-Signal | |
| 0 | normal | |
| 1 | inversion | |

Table 75: Inversion A-Signal

| INV_B | | Addr. 0x16; bit 1 |
|-------|------------------|-------------------|
| Code | B/DIR/CCW-Signal | |
| 0 | normal | |
| 1 | inversion | |

Table 76: Inversion B-Signal

| INV_Z | | Addr. 0x16; bit 0 |
|-------|---------------|-------------------|
| Code | Z/NCLR-Signal | |
| 0 | normal | |
| 1 | inversion | |

Table 77: Inversion Z-Signal

Index pulse Z can be programmed in four lengths. The position of the index pulse in relation to the A/B signals is shown in Figure 45.

| LENZ(1:0) | | Addr. 0x16; bit 7:6 |
|-----------|----------------|---------------------|
| Code | Z-pulse length | |
| 0x0 | 90° | |
| 0x1 | 180° | |
| 0x2 | 270° | |
| 0x3 | 360° | |

Table 78: Index pulse length

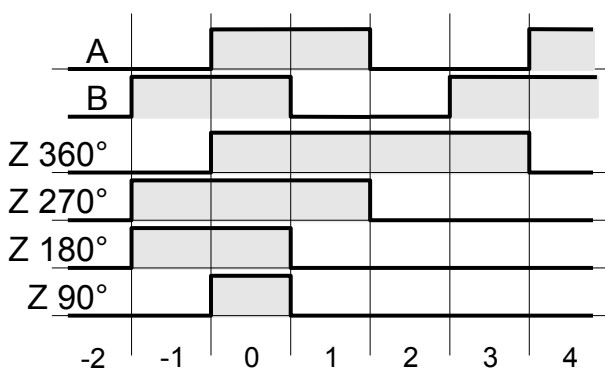


Figure 45: Index pulse length settings

The direction of rotation can be inverted with parameter ROT_ALL. The parameter affects the output of the data word through the serial interface in MODE_ST=0x0 and 0x1, the ABZ-interface and the UVW-interface.

| ROT_ALL | | Addr. 0x15; bit 7 |
|---------|--------------------------------|-------------------|
| Code | Description | |
| 0 | no inversion of code direction | |
| 1 | inversion of code direction | |

Table 79: Inverted direction of rotation

Parameter SS_AB must be configured depending on the maximum speed. With a filter setting of FILT = 0x00 (Table 53), correspondingly higher SS_AB step size values must be programmed. The maximum possible resolution of the incremental count signal is limited by the selected step size.

| SS_AB(1:0) | | Addr. 0x15; bit 5:4 | | | |
|------------|-----------------|---------------------|------------------------|------------------------|----------------------|
| Code | max res. | FILT | max. rotation speed *) | | |
| | | | MPC = 0x4 (16/15) | MPC = 0x5 (32/31) | MPC = 0x6 (64/63) |
| 0x0 | 2 ¹⁸ | 0x0 ≥ 0x1 | don't use 6000 rpm | don't use 6000 rpm | 1500 rpm 6000 rpm |
| 0x1 | 2 ¹⁷ | 0x0 ≥ 0x1 | don't use 12000 rpm | 3000 rpm 12000 rpm | 3000 rpm 6000 rpm |
| 0x2 | 2 ¹⁶ | 0x0 ≥ 0x1 | 6000 rpm 24000 rpm | 6000 rpm 12000 rpm | 6000 rpm 6000 rpm |
| 0x3 | 2 ¹⁵ | 0x0 ≥ 0x1 | 12000 rpm 24000 rpm | 12000 rpm 12000 rpm | 6000 rpm 6000 rpm |
| Note: | *) FRQAB = 0x0 | | | | |

Table 80: System AB step size and limitation of rotation frequency

The minimum edge distance t_{mtd} of the ABZ, STEP/DIR or CW/CCW interface can be limited by setting the maximum output frequency with FRQAB. It can be used to adjust the output frequency to a frequency limit given by an external ABZ, STEP/DIR or CW/CCW counter device. The FRQ_ABZ status bit is set in the case of an unacceptable high speed.

| FRQAB(2:0) | | Addr. 0x15; bit 2:0 | |
|------------|---------------------|--------------------------------|--|
| Code | Output frequency AB | Edge distance t_{mtd} | |
| 0x0 | 6.25 MHz | 40 ns | |
| 0x1 | 3.13 MHz | 80 ns | |
| 0x2 | 1.56 MHz | 160 ns | |
| 0x3 | 781.25 kHz | 320 ns | |
| 0x4 | 390.63 kHz | 640 ns | |
| 0x5 | 195.31 kHz | 1.28 μs | |
| 0x6 | 48.83 kHz | 5.12 μs | |
| 0x7 | 12.2 kHz | 20.48 μs | |

Table 81: AB output frequency

The incremental counter has an integrated hysteresis which prevents multiple switching of the incremental signals at the reversing point. Hysteresis φ_{hys} must first be exceeded before edges can again be generated at

A or B. This hysteresis can be set within a range of 0° to 0.35° according to Table 82 and is referenced to 360° of a singleturn cycle.

| CHYS_AB(1:0) Addr. 0x16; bit 5:4 | | |
|---|------------------|-----------------|
| Code | Hysteresis | parameter SS_AB |
| 0x0 | 0.0014° | 0x0 |
| 0x0 | 0.0041° | 0x1 |
| 0x0 | 0.0096° | 0x2 |
| 0x0 | 0.021° | 0x3 |
| 0x1 | 0.175° | d.c. |
| 0x2 | 0.35° | d.c. |
| 0x3 | 0.7° | d.c. |
| Notes: | d.c.: don't care | |

Table 82: Hysteresis with an inverted direction of rotation

The parameter ENIF_AUTO selects whether at startup the incremental interface is enabled after the converter has found its operating point or if the counting to the absolute angle can be seen at the incremental interface.

| ENIF_AUTO Addr. 0x15; bit 4 | |
|------------------------------------|---|
| Code | Description |
| 0 | counting to operating point visible |
| 1 | counting to operating point not visible |

Table 83: Incremental interface enable

See the chapter on the preset function (p. 64) to set the offset for ABZ output.

UVW COMMUTATION SIGNALS

| MODEB | |
|-------|-------------|
| Code | Description |
| 0x1 | UVW |

Table 84: MODEB: UVW

iC-MU can generate commutation signals for BLDC motors from 1 up to 16 pole pairs. The hysteresis is set fixed to 0.0879° referenced to a mechanical revolution.

Figure 46 shows the commutation sequence for a motor with 6 pole pairs. Here, a commutation sequence spanning an angle of φ_{360UVW} repeats itself 6 times within one mechanical revolution of the motor. The phase shift between the commutation signals is 120°.

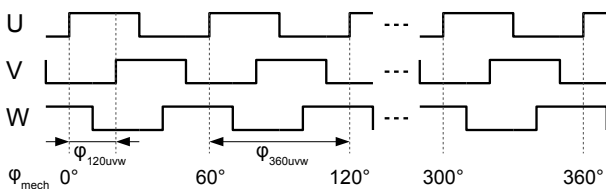


Figure 46: commutation signals UVW

Using parameter PPUVW the number of commutation sequences per mechanical revolution can be set.

| PPUVW(5:0) Addr. 0x17; bit 5:0 | | | |
|--------------------------------|----------------------|------|----------------------|
| Code | number of pole pairs | Code | number of pole pairs |
| 0x02 | 1 pole pair | 0x1A | 9 pole pairs |
| 0x05 | 2 pole pairs | 0x1D | 10 pole pairs |
| 0x08 | 3 pole pairs | 0x20 | 11 pole pairs |
| 0x0B | 4 pole pairs | 0x23 | 12 pole pairs |
| 0x0E | 5 pole pairs | 0x26 | 13 pole pairs |
| 0x11 | 6 pole pairs | 0x29 | 14 pole pairs |
| 0x14 | 7 pole pairs | 0x2C | 15 pole pairs |
| 0x17 | 8 pole pairs | 0x2F | 16 pole pairs |

Table 85: Number of commutation signal pole pairs

The sequence of the commutation signals can be selected by φ_{120UVW} as in Figure 46 or with a distance of 60° between two neighboring rising edges referenced to one UVW cycle using parameter PP60UVW.

| PP60UVW Addr. 0x16; bit 3 | |
|---------------------------|-------------------|
| Code | Phase UVW signals |
| 0 | 120° phase shift |
| 1 | 60° phase shift |

Table 86: Commutation signal phase length

Register OFF_UVW is used to set the start angle and compensate for the offset between the winding of the BLDC and the Hall sensor signals. This angle can be set with 12 bits.

Note:

After startup or the commands SOFT_RESET and ABS_RESET the OFF_UVW values are amended to include the nonius data, with a configured multi-turn updated with the multiturn data, and stored as OFF_COM in the internal RAM.

| OFF_UVW(3:0) | Addr. 0x28; bit 7:4 |
|----------------------|---|
| OFF_UVW(11:4) | Addr. 0x29; bit 7:0 |
| OFF_UVW(3:0) | Addr. SER:0x4B; bit 7:4 |
| OFF_UVW(11:4) | Addr. SER:0x4C; bit 7:0 |
| Code | Offset UVW signals |
| 0x000 | 0.00° mech |
| 0x001 | 0.09° mech |
| ... | $\frac{360.0^\circ \text{ mech}}{4096} \cdot \text{OFF_UVW}$ |
| 0xFFFF | 359.9° mech |

Table 87: Commutation signal start angle

| OFF_COM(3:0) | Addr. SER:0x23; bit 7:4 | R |
|----------------------|---|---|
| OFF_COM(11:4) | Addr. SER:0x24; bit 7:0 | R |
| Code | Description | |
| 0x000 | start angle commutation signal (automatically computed) | |
| ... | | |
| 0xFFFF | | |

Table 88: Commutation signal start angle amended by the nonius/MT

The direction of rotation can be inverted with parameter ROT_ALL. The parameter affects the output of the data word through the serial interface in MODE_ST=0x0 and 0x1, the ABZ-interface and the UVW-interface.

| ROT_ALL Addr. 0x15; bit 7 | |
|---------------------------|---------------------------------------|
| Code | Description |
| 0 | no inversion of direction of rotation |
| 1 | inversion of rotation |

Table 89: Inverted direction of rotation

REGISTER ACCESS THROUGH SERIAL INTERFACE (SPI AND BISS)

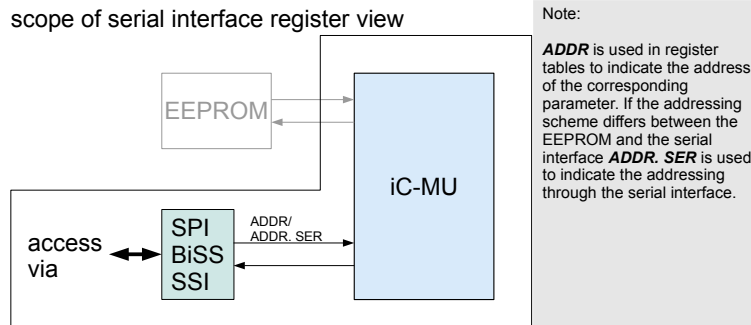


Figure 47: Scope of register mapping serial interface

The distribution of addresses in iC-MU corresponds to the document BiSS C Protocol Description which can be downloaded at www.biss-interface.com.

iC-MU supports an addressing scheme using banks. Therefore the internal address space is divided into banks of 64 bytes each. The address sections visible via the I/O interface recognizes a "dynamic" section (addresses 0x00 to 0x3F) and a "static" section which is permanently visible (addresses 0x40 to 0x7F). The static address section is always visible independent of the bank currently selected. Figure 48 illustrates how the banks selected by BANKSEL are addressed.

| BANKSEL(4:0) Addr. SER:0x40; bit 4:0 | |
|---|------------------------------|
| Code | Description |
| 0x0 | Selection of the memory bank |
| ... | |
| 0x1F | |

Table 90: Register to select a memory bank

The abbreviation *Addr. SER* used in the register tables of the specification of the iC-MU stands for the addressing of this register through the serial interface.

The address translation for the addressable memory areas via the bank register to the EEPROM addresses is shown in Table 91. Figure 49 shows a schematical overview of the register/memory mapping.

| Code | Bank | Memory location during operation | Mode |
|------|------|----------------------------------|--------------------------|
| CONF | 0 | internal register | iC-MU configuration data |
| EDS | 1 | E2P: 0x040-0x07F | Electronic Data Sheet |
| | ... | ... | |
| USER | 4 | E2P: 0x100-0x13F | OEM data, free user area |
| | ... | ... | |
| USER | 5 | E2P: 0x140-0x17F | OEM data, free user area |
| | ... | ... | |
| USER | 31 | E2P: 0x7C0-0x7FF | OEM data, free user area |
| | ... | ... | |

Table 91: Address translation Addr Ser: 0x00-0x3F

After startup the BANKSEL register is set to 0.

Note: Burst mode is not supported by iC-MU for write access to the registers. Data has to be written byte-by-byte.

| CONF: Bank 0, Addresses 0x00-0x3F | | | | | | | | |
|--|-------------|-------|-----------|-------|-----------|-------|-------|-------|
| Addr. SER | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x00 | GC_M(1:0) | | GF_M(5:0) | | | | | |
| 0x01 | GX_M(6:0) | | | | | | | |
| 0x02 | VOSS_M(6:0) | | | | | | | |
| 0x03 | VOSC_M(6:0) | | | | | | | |
| 0x04 | PH_M(6:0) | | | | | | | |
| 0x05 | ENAC | | | | CIBM(3:0) | | | |
| 0x06 | GC_N(1:0) | | GF_N(5:0) | | | | | |
| 0x07 | GX_N(6:0) | | | | | | | |
| 0x08 | VOSS_N(6:0) | | | | | | | |

| CONF: Bank 0, Addresses 0x00-0x3F | | | | | | | | | |
|-----------------------------------|---|------------|--------------|---------------|--------------|---------------|-------|-------|--|
| Addr. SER | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
| 0x09 | VOSC_N(6:0) | | | | | | | | |
| 0x0A | PH_N(6:0) | | | | | | | | |
| 0x0B | MODEB(2:0) | | | | MODEA(2:0) | | | | |
| 0x0C | CFGEW(7:0) | | | | | | | | |
| 0x0D | ACC_STAT | NCHK_CRC | NCHK_NON | ACRM_RES | EMTD(2:0) | | | | |
| 0x0E | ESSI_MT(1:0) | | ROT_MT | LIN | FILT(2:0) | | | | |
| 0x0F | SPO_MT(3:0) | | | | MPC(3:0) | | | | |
| 0x10 | GET_MT | CHK_MT | SBL_MT(1:0) | | MODE_MT(3:0) | | | | |
| 0x11 | OUT_ZERO(2:0) | | | OUT_MSB(4:0) | | | | | |
| 0x12 | GSSI | RSSI | MODE_ST(1:0) | | OUT_LSB(3:0) | | | | |
| 0x13 | RESABZ(7:0) | | | | | | | | |
| 0x14 | RESABZ(15:8) | | | | | | | | |
| 0x15 | ROT_ALL | SS_AB(1:0) | | ENIF_AUTO | FRQAB(2:0) | | | | |
| 0x16 | LENZ(1:0) | | CHYS_AB(1:0) | | PP60UVW | INV_A | INV_B | INV_Z | |
| 0x17 | RPL(1:0) | | PPUVW(5:0) | | | | | | |
| 0x18 | TEST(7:0) | | | | | | | | |
| 0x19 | RESERVED | | | | | | | | |
| ... | | | | | | | | | |
| 0x1D | RESERVED | | | | | | | | |
| 0x1E | OFF_ABZ(3:0) | | | | RESERVED | | | | |
| 0x1F | OFF_ABZ(11:4) | | | | | | | | |
| 0x20 | OFF_POS*(19:12) | | | | | | | | |
| 0x21 | OFF_POS*(27:20) | | | | | | | | |
| 0x22 | OFF_POS*(35:28) | | | | | | | | |
| 0x23 | OFF_COM**(3:0) | | | | RESERVED | | | | |
| 0x24 | OFF_COM**(11:4) | | | | | | | | |
| 0x25 | PA0_CONF(7:0) | | | | | | | | |
| 0x26 | RESERVED | | | | | | | | |
| ... | | | | | | | | | |
| 0x2A | RESERVED | | | | | | | | |
| 0x2B | RESERVED | | | ACGAIN_M(1:0) | | AFGAIN_M(2:0) | | | |
| 0x2C | RESERVED | | | | | | | | |
| ... | | | | | | | | | |
| 0x2E | RESERVED | | | | | | | | |
| 0x2F | RESERVED | | | ACGAIN_N(1:0) | | AFGAIN_N(2:0) | | | |
| 0x30 | RESERVED | | | | | | | | |
| ... | | | | | | | | | |
| 0x3F | RESERVED | | | | | | | | |
| Note: | * OFF_ABZ value amended to include nonius/multiturn information ** OFF_UVW value amended to include nonius information | | | | | | | | |

Table 92: Register mapping bank 0, addresses 0x00-0x3F (access via serial interface)

OFF_POS* are the offset values (OFF_ABZ) automatically changed by the period information of the initial nonius calculation and if configured by the external multiturn data. OFF_POS can thus be seen as a start value for the internally counted ST period and MT data.

iC-MU MAGNETIC OFF-AXIS POSITION ENCODER - POLE WIDTH 1.28MM



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| Static part: Addresses 0x40-0xBF | | | | | | | | | |
|----------------------------------|-------------------------|-------|-------|--------------|---------------|-------|-------|-------|--|
| Addr. SER | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
| 0x40 | | | | BANKSEL(4:0) | | | | | |
| 0x41 | EDSBANK(7:0) | | | | | | | | |
| 0x42 | PROFILE_ID(15:8) | | | | | | | | |
| 0x43 | PROFILE_ID(7:0) | | | | | | | | |
| 0x44 | SERIAL(31:24) | | | | | | | | |
| 0x45 | SERIAL(23:16) | | | | | | | | |
| 0x46 | SERIAL(15:8) | | | | | | | | |
| 0x47 | SERIAL(7:0) | | | | | | | | |
| 0x48 | OFF_ABZ(19:12) | | | | | | | | |
| 0x49 | OFF_ABZ(27:20) | | | | | | | | |
| 0x4A | OFF_ABZ(35:28) | | | | | | | | |
| 0x4B | OFF_UVW(3:0) | | | | RESERVED | | | | |
| 0x4C | OFF_UVW(11:4) | | | | | | | | |
| 0x4D | PRES_POS(3:0) | | | | RESERVED | | | | |
| 0x4E | PRES_POS(11:4) | | | | | | | | |
| 0x4F | PRES_POS(19:12) | | | | | | | | |
| 0x50 | PRES_POS(27:20) | | | | | | | | |
| 0x51 | PRES_POS(35:28) | | | | | | | | |
| 0x52 | SPO_0(3:0) | | | | SPO_BASE(3:0) | | | | |
| 0x53 | SPO_2(3:0) | | | | SPO_1(3:0) | | | | |
| 0x54 | SPO_4(3:0) | | | | SPO_3(3:0) | | | | |
| 0x55 | SPO_6(3:0) | | | | SPO_5(3:0) | | | | |
| 0x56 | SPO_8(3:0) | | | | SPO_7(3:0) | | | | |
| 0x57 | SPO_10(3:0) | | | | SPO_9(3:0) | | | | |
| 0x58 | SPO_12(3:0) | | | | SPO_11(3:0) | | | | |
| 0x59 | SPO_14(3:0) | | | | SPO_13(3:0) | | | | |
| 0x5A | RPL_RESET(7:0) | | | | | | | | |
| 0x5B | I2C_DEV_START(7:0) | | | | | | | | |
| 0x5C | I2C_RAM_START(7:0) | | | | | | | | |
| 0x5D | I2C_RAM_END(7:0) | | | | | | | | |
| 0x5E | I2C_DEVID(7:0) | | | | | | | | |
| 0x5F | I2C_RETRY(7:0) | | | | | | | | |
| 0x60 | USER_EXCHANGE_REGISTERS | | | | | | | | |
| ... | | | | | | | | | |
| 0x6F | RESERVED | | | | | | | | |
| 0x70 | | | | | | | | | |
| 0x71 | | | | | | | | | |
| 0x72 | EVENT_COUNT(7:0) | | | | | | | | |
| 0x73 | | | | | | | | | |
| 0x74 | | | | | | | | | |
| 0x75 | HARD_REV(7:0) | | | | | | | | |
| 0x76 | CMD_MU(7:0) | | | | | | | | |
| 0x77 | STATUS0(7:0) | | | | | | | | |
| 0x78 | STATUS1(7:0) | | | | | | | | |
| 0x79 | DEV_ID(47:40) | | | | | | | | |
| 0x7A | DEV_ID(39:32) | | | | | | | | |
| 0x7B | DEV_ID(31:24) | | | | | | | | |
| 0x7C | DEV_ID(23:16) | | | | | | | | |

| Static part: Addresses 0x40-0xBF | | | | | | | | |
|----------------------------------|--------------|-------|-------|-------|-------|-------|-------|-------|
| Addr. SER | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x7C | DEV_ID(15:8) | | | | | | | |
| 0x7D | DEV_ID(7:0) | | | | | | | |
| 0x7E | MFG_ID(15:8) | | | | | | | |
| 0x7F | MFG_ID(7:0) | | | | | | | |
| 0x80*) | CRC16(7:0) | | | | | | | |
| 0x81*) | CRC16(15:8) | | | | | | | |
| 0x82*) | CRC8(7:0) | | | | | | | |
| 0x83*) | RESERVED | | | | | | | |
| ... | | | | | | | | |
| 0xAF*) | | | | | | | | |

*) Access on address space SER > 0x7F only via SPI interface possible

Table 93: Register mapping bank 0-31, addresses 0x40-0xBF (access via serial interface)

The current iC-MU Series chip type and hardware revision can be read out through HARD_REV. The upper nibble indicates the chip type (iC-MU = 0b0000, iC-MU150 = 0b0001, iC-MU200 = 0b0010), and the lower nibble indicates the hardware revision.

| HARD_REV(7:0) Addr. SER: 0x74; bit 7:0 | |
|--|------------------------|
| Code | Chip Type and Revision |
| 0x02 | iC-MU 0 |
| 0x03 | iC-MU 1 |
| 0x04 | iC-MU Z |
| 0x05 | iC-MU Y |
| 0x06 | iC-MU Y1 |
| 0x07 | iC-MU Y2/Y2H |
| 0x10 | iC-MU150 0 |
| 0x11 | iC-MU150 1 |
| 0x20 | iC-MU200 0 |

Table 94: HARD_REV

Address sections/Register protection level

Register access can be restricted via RPL (see Table 95). RPL = 0x2/0x3 selects a shipping mode with limited access which can be set back to RPL = 0x0. To set back RPL the content of Bank: 0, Addr. SER: 0x17 has to be written to RPL_RESET.

| RPL(1:0) Addr. 0x17; bit 7:6 | | |
|------------------------------|---|--------------------|
| Code | Mode | Access restriction |
| 0x0 | Configuration mode, no restrictions | RP0 |
| 0x1 | Shipping mode, without command I2C_COM, reset is not possible | RP1 |
| 0x2 | Shipping mode, with command I2C_COM, reset to RP0 possible | RP1 |
| 0x3 | Shipping mode, without command I2C_COM, reset to RP0 possible | RP1 |

Table 95: Register access control

| RPL_RESET(7:0) Addr. SER:0x5A; bit 7:0 | |
|--|------------------------|
| Code | Description |
| 0x00 | Set back value for RPL |
| ... | |
| 0xFF | |

Table 96: Set back value for RPL

Sections CONF, EDS and USER are protected at different levels in shipping mode for read and write access (see Figure 48).

| RPL(1:0) Addr. 0x17; bit 7:6 | | | | |
|------------------------------|--|------|-----|------|
| RPL* | Section | CONF | EDS | USER |
| RP0 | | r/w | r/w | r/w |
| RP1 | | n/a | r | r/w |
| Note | *) RPL: Register Protection Level n/a: iC-MU denies access to those register addresses r: Registers are readable w: Registers are writeable | | | |

Table 97: Register Read/Write Protection Levels

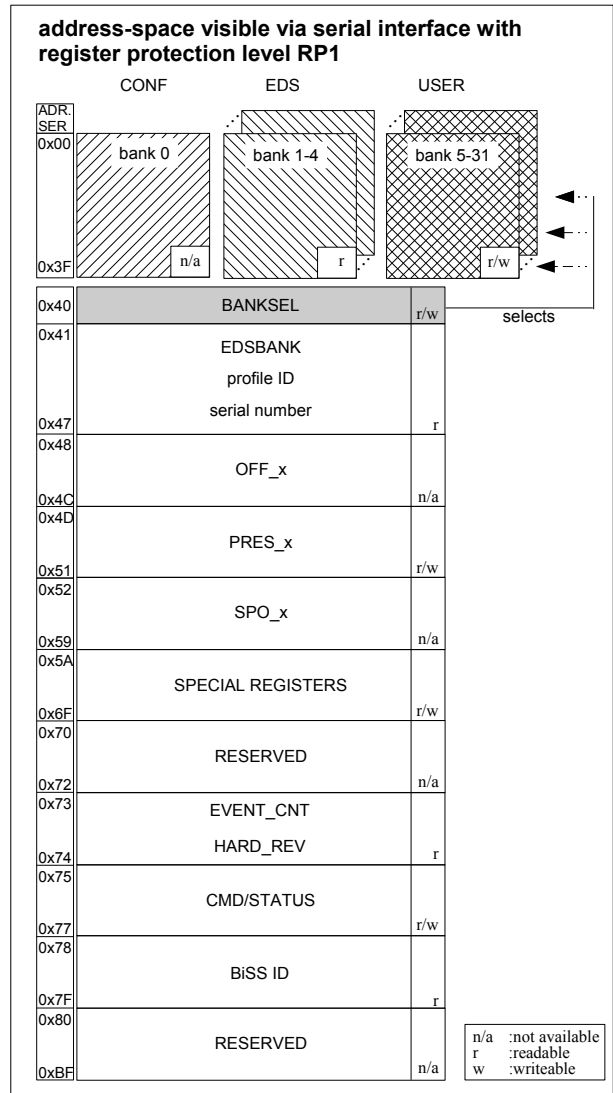


Figure 48: Principle of bank-wise memory addressing and access restrictions with register protection level RP1

Overview Register access: memory mapping, Register protection levels

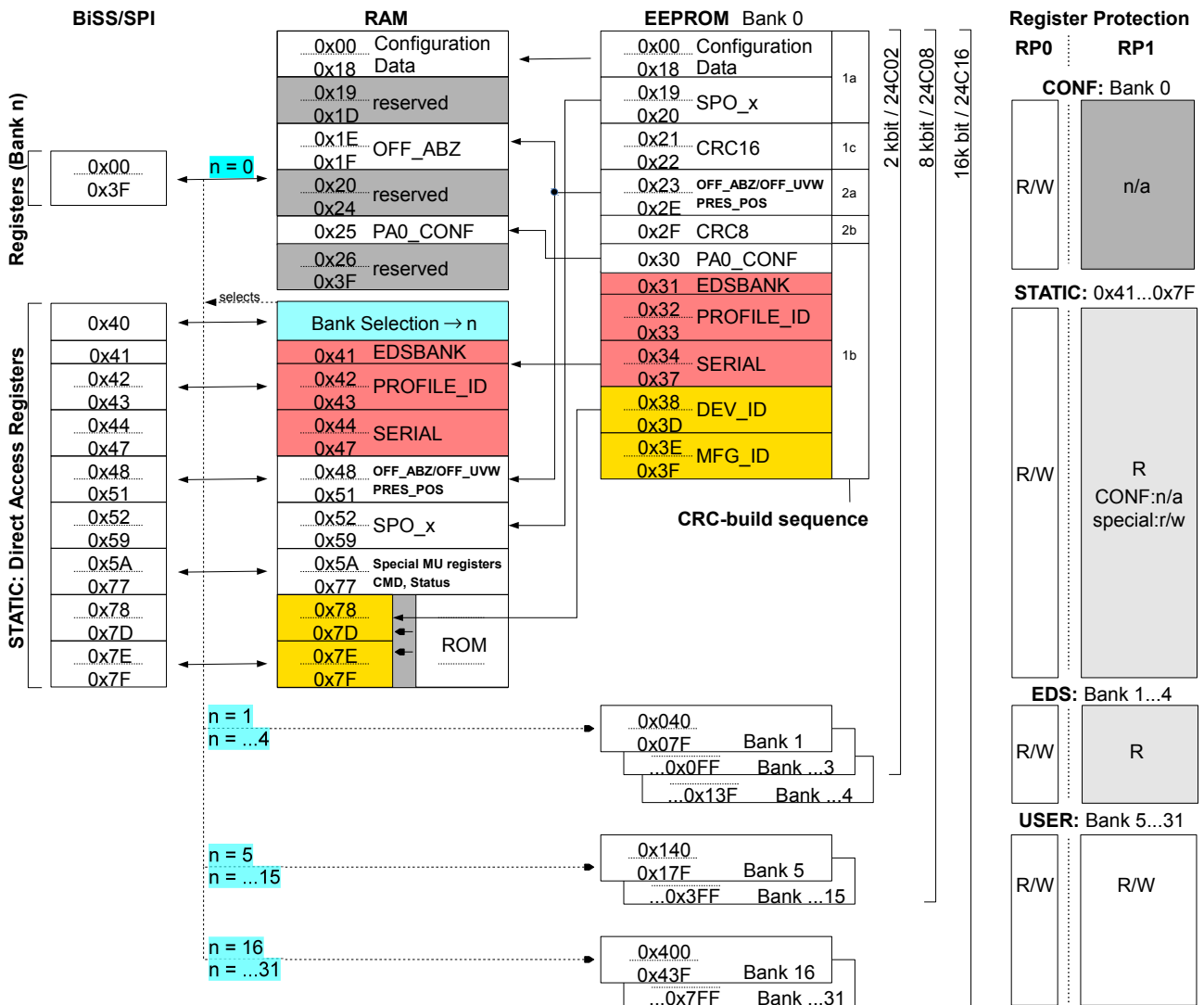


Figure 49: Register access with memory mapping

STATUS REGISTER AND ERROR MONITORING

Status register

Various Status-information can be read out via status bytes STATUS0 and STATUS1.

| STATUS0(7:0) | | Addr. SER: 0x76; bit 7:0 | R |
|--------------|--------|--|---|
| Bit | Name | Description of status message | |
| 4 | STUP | Startup iC-MU | |
| 3 | AN_MAX | Signal error*: clipping (nonius track) | |
| 2 | AN_MIN | Signal error*: poor level (nonius track) | |
| 1 | AM_MAX | Signal error*: clipping (master track) | |
| 0 | AM_MIN | Signal error*: poor level (master track) | |
| | Notes | Error indication logic: 1 = true, 0 = false, * for signal thresholds see elec. char. no. 508 and 509 | |

Table 98: Status register 0

Status bit **STUP** indicates that one or multiple of the following conditions apply during the startup routine:

- An I2C communication or CRC error occurred (ABZ/UVW engine is stopped, reset with ABS_RESET)
- The amplitude of the master track is too low and ACRM_RES = 1 (ABZ/UVW engine is stopped, reset when the master track amplitude is sufficient again)
This also applies during normal operation.
- The multiturn interface is active and communication fails or the SSI error bit is active

| STATUS1(7:0) | | Addr. SER: 0x77; bit 7:0 | R |
|--------------|---------|---|---|
| Bit | Name | Description of status message | |
| 7 | CRC_ERR | Invalid check sum internal RAM | |
| 6 | EPR_ERR | I2C communication error: - No EEPROM - I2C communication error | |
| 5 | MT_ERR | Multiturn communication error: - MTD line not 1 when trying to read MT data - MTD line is not 0 right after the last clock pulse - SSI error bit active on MT interface* | |
| 4 | MT_CTR | Multiturn data consistency error: counted multiturn ↔ external MT data | |
| 3 | NON_CTR | Period counter consistency error: counted period ↔ calculated Nonius position | |
| 2 | FRQ_ABZ | Excessive signal frequency for ABZ-converter | |
| 1 | FRQ_CNV | Excessive signal frequency for internal 12 Bit converter | |
| 0 | CMD_EXE | Command execution in progress | |
| | Notes | Error indication logic: 1 = true, 0 = false * ESSI_MT = 0x1 or 0x3 | |

Table 99: Status register 1

ACC_STAT configures, if the status registers show the actual or the accumulated status information.

If the accumulated status is configured, the status bits are maintained until the status register is read out or the command ABS_RESET or SOFT_RESET are executed. This is valid except for EPR_ERR, STUP and CMD_EXE. These bits are set in the status register independent of the ACC_STAT configuration while the status information is active. The status register can be accessed independently of the internal operating state.

| ACC_STAT | | Addr. 0x0D; bit 7 |
|----------|--|-------------------|
| Code | Description | |
| 0 | Output of actual status information | |
| 1 | Output of accumulated status information | |

Table 100: Output configuration of status register

Note:

A read access to the reserved addresses SER: 0x3D and 0x3E also clears the accumulated status information STATUS0 and STATUS1 if ACC_STAT is set to 1.

Error and warning bit configuration

The output and the polarity of the error and warning bit within the different serial protocols (MODEA Table 34) can be found in Table 101. Messages are allocated to the error and warning bit by parameter CFGEW according to Table 102.

| MODEA(2:0) | Addr. 0x0B; bit 2:0 | | | |
|------------|---------------------|-------------|------------|-------------|
| | Error | | Warning | |
| Function | low active | high active | low active | high active |
| SPI | - | - | - | - |
| BiSS | x | - | x | - |
| SSI | - | - | - | - |
| SSI+ERRL | x | - | - | - |
| SSI+ERRH | - | x | - | - |
| ExtSSI | x | - | x | - |

Table 101: MODEA: error/warning-bit within serial protocols

| CFGEW(7:0) Addr. 0x0C; bit 7:0 | |
|---------------------------------------|--|
| Bit | Visibility for error bit |
| 7 | MT_ERR/MT_CTR |
| 6 | NON_CTR |
| 5 | Ax_MAX and Ax_MIN |
| 4 | EPR_ERR |
| 3 | CRC_ERR |
| 2 | CMD_EXE |
| Bit | Visibility for warning bit |
| 1 | FRQ_CNV/FRQ_ABZ |
| 0 | Ax_MAX and Ax_MIN |
| Notes | x = M, N Encoding: 0 = message enabled, 1 = message disabled |

Table 102: Error and warning bit configuration

If an error pin is configured using MODEB (Table 35), an internal error (see status register, ACC_STAT configuration and error bit configuration with CFGEW) is signaled by pulling the NER pin (PB3) against VND. In that case pin PB3 is an open-collector output. With devices featuring open-drain alarm outputs a wired-or bus logic can be installed. The minimum message time for I/O pin NER can be set by EMTD.

| EMTD(2:0) Addr. 0x0D; bit 2:0 | | | |
|--------------------------------------|-----------------|------|-----------------|
| Code | min. disp. time | Code | min. disp. time |
| 0x0 | 0 ms | 0x4 | 50 ms |
| 0x1 | 12.5 ms | 0x5 | 62.5 ms |
| 0x2 | 25 ms | 0x6 | 75 ms |
| 0x3 | 37.5 ms | 0x7 | 87.5 ms |

Table 103: Minimum error display time

COMMAND REGISTER

Description of implemented commands

The CMD_MU register is used to execute defined commands received via the serial interface. As long as the command is queued the CMD_MU register keeps the respective command code. Once the command is accepted and execution started, CMD_MU is set to 0x00.

| CMD_MU(7:0) | | Addr. SER: 0x75; bit 7:0 | W |
|-------------|-----------------|--|---|
| Code | Command | Explanation | |
| 0x00 | reserved | no function | |
| 0x01 | WRITE_ALL | Write internal configuration and Offset values to EEPROM | |
| 0x02 | WRITE_OFF | Write internal Offset values to EEPROM | |
| 0x03 | ABS_RESET | Reset of Absolute value (including ABZ-part), takes typ. 10 ms | |
| 0x04 | NON_VER | Verification of actual position by doing a nonius calculation | |
| 0x05 | MT_RESET | New read in and synchronisation of multiturn value | |
| 0x06 | MT_VER | Read in of multiturn and verification of counted multiturn value | |
| 0x07 | SOFT_RESET | startup with read in of EEPROM | |
| 0x08 | SOFT_PRES | Set output to preset | |
| 0x09 | SOFT_E2P_PRES | Set output to preset and save offset values to EEPROM | |
| 0x0A | I2C_COM | start I2C communication | |
| 0x0B | EVENT_COUNT | increment event counter by 1 | |
| 0x0C | SWITCH | Writes all configurations parameters without offsets to EEPROM. MODEA/RPL will be exchanged with MODEA_NEW/RPL_NEW during write operation | |
| 0x0D | CRC_VER | Verification of CRC16 and CRC8 | |
| 0x0E | CRC_CALC | Recalculate internal CRC16 and CRC8 values | |
| 0x0F | SET_MTC | Set MTC-Pin *) | |
| 0x10 | RES_MTC | Reset MTC-Pin *) | |
| 0x11 | reserved | no function | |
| ...0xFF | | | |
| Note: | *) MODE_MT=0x00 | | |

Table 104: Implemented commands

WRITE_ALL stores the internal configuration and offset/preset values to the EEPROM. CRC16 and CRC8 are automatically updated.

WRITE_OFF only stores the offset/preset data area to the EEPROM. CRC8 is automatically updated.

Command **ABS_RESET** initiates a redefinition of the absolute value. A new nonius calculation is started. If a multiturn is configured, this is read in and synchronized. Offset values OFF_ABZ/OFF_UVW are amended to include the ST period and MT information and are stored as OFF_POS and OFF_COM. The ABZ/UVW converter is restarted.

Command **NON_VER** initiates a nonius calculation and the computed value is compared to the current counted period. If there is a discrepancy, error bit NON_CTR is set in status register STATUS1.

With command **MT_RESET** an external multiturn is read in anew and synchronized. Offset values

OFF_ABZ and OFF_UVW are changed to include the newly read-in multiturn data and stored as OFF_POS and OFF_COM.

Attention:

The ABZ/UVW converter is not restarted automatically with the command **MT_RESET**. If part of the multiturn data is used for the singleturn information, **ABS_RESET** has to be executed additionally.

With command **MT_VER** an external multiturn is read in and the counted multiturn value is verified. If there is a discrepancy, error bit MT_CTR is set in status register STATUS1.

With command **SOFT_RESET** internal finite state machines and counters are reset. The EEPROM is read in anew. A redefinition of the

absolute value is initiated (see **ABS_RESET**)

Attention:

After issuing the **SOFT_RESET** command no further communication attempt with iC-MU is permitted for at least 50ms.

Command **SOFT_PRES** initiates a preset sequence (cf. page 64) with preset values **PRES_POS**. The internal offset values **OFF_ABZ** are changed to set the output value to the value given by **PRES_POS**. The internal **CRC8** is automatically updated.

Command **SOFT_E2P_PRES** initiates a preset sequence (cf. page 64) with preset values **PRES_POS**. The altered offset values **OFF_ABZ** are stored in the EEPROM. **CRC8** is automatically updated.

Command **I2C_COM** initiates communication with a I2C device (**RPL=0x00** and **0x02**). Prior to this the following parameters must be configured:

- **I2C_DEVID**
- **I2C_RAM_START**
- **I2C_RAM_END**
- **I2C_DEV_START**

The device ID is written to **I2C_DEVID** (see Table 105). If an error occurs while communicating with an external I2C device up to 3 new communication attempts are started by iC-MU.

I2C_RAM_START defines the start address in the internal RAM which in case of a

- write access: marks the begin of the data area that holds the data to be written
- read access: marks the begin of the data area where the data read from the I2C device is written to

According to this **I2C_RAM_END** defines the end address of the data area in the internal RAM. The number of bytes **NUM_BYTES** to be read/written is determined as **I2C_RAM_END - I2C_RAM_START + 1** (if the **I2C_RAM_END** and **I2C_RAM_START** address are identical 1 byte is read/written).

I2C_DEV_START defines the start address of the I2C device from which **NUM_BYTES** bytes should be read/written.

The **USER_EXCHANGE_REGISTERS** (see Table 93) can be used for the data-exchange with the I2C device.

| I2C_DEVID(7:0) Addr. SER:0x5E; bit 7:0 | |
|---|--|
| Code | Meaning |
| 0xA0 | write EEPROM |
| 0xA1 | read EEPROM |
| 0xC0 | write iC-PVL (status/commands) |
| 0xC1 | read iC-PVL (status/commands) |
| Note: | I2C_DEVID needs to include the I2C read/write bit. |

Table 105: Examples of I2C Device IDs

| I2C_RAM_START Addr. SER: 0x5C; bit 7:0 | |
|---|-----------------------|
| Code | Description |
| 0x00 | I2C-RAM start address |
| ... | |
| 0xFF | |

Table 106: I2C-RAM start address

| I2C_RAM_END Addr. SER: 0x5D; bit 7:0 | |
|---|---------------------|
| Code | Description |
| 0x00 | I2C-RAM end address |
| ... | |
| 0xFF | |

Table 107: I2C-RAM end address

| I2C_DEV_START Addr. SER: 0x5B; bit 7:0 | |
|---|--------------------------|
| Code | Description |
| 0x00 | I2C device start address |
| ... | |
| 0xFF | |

Table 108: I2C device start address

With command **EVENT_COUNT** the value of register **EVENT_COUNT** is incremented by 1.

| EVENT_COUNT(7:0) Addr. SER:0x73; bit 7:0 | |
|---|---------------|
| Code | Description |
| 0x0 | Event counter |
| ... | |
| 0xFF | |

Table 109: Event counter

The command **SWITCH** makes it possible to write configurations of **MODEA** and **RPL** into the EEPROM which inhibit further register communications (e.g. **MODEA=ABZ**).

Note: **RPL** must be set to **0x0** before starting the command.

MODEA_NEW and RPL_NEW are used to set the target configuration of MODEA and RPL (e.g. ABZ, no RPL). On executing the command SWITCH MODEA and RPL are set to the target values and the configuration without the offsets is written to the EEPROM. Finally MODEA and RPL are set back to the original values. This makes it possible to control the success of the EEPROM write process by reading STATUS1 (EPR_ERR should not be set).

Note: CRC_ERR is set after command execution if there is the cyclic CRC check configured by NCHK_CRC=0 and the target values of MODEA and RPL differ from the originals values.

iC-MU starts with the interface and register protection level configured with MODEA_NEW and RPL_NEW after the next startup or after the execution of command SOFT_RESET.

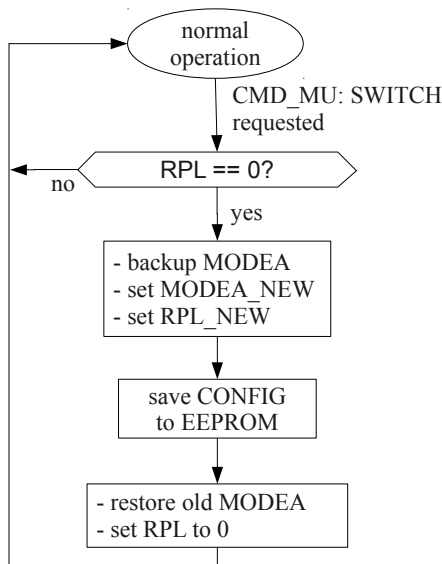


Figure 50: Event sequence of command SWITCH

Note: The SWITCH command should always be executed as the last command after all other configurations have been finished and stored to the EEPROM. Otherwise the values set by RPL_NEW and MODEA_NEW will be overwritten again by the actual RPL and MODEA values, defeating the purpose of the SWITCH command.

If the SWITCH command is used with an empty EEPROM, the WRITE_OFF command needs to be executed in addition to properly initialize the OFFSET/PRESET area CRC8.

| MODEA_NEW | | Addr. SER: 0x60; bit 2:0 | | | |
|-----------|-------|--------------------------|------|------|--------------------|
| Code | PA0 | PA1 | PA2 | PA3 | Function |
| 0x0 | NCS | SCLK | MOSI | MISO | SPI _{TR1} |
| 0x1 | NCS | SCLK | MOSI | MISO | SPI |
| 0x2 | NPRES | MA | SLI | SLO | BiSS |
| 0x3 | NPRES | A | B | Z | ABZ |
| 0x4 | NPRES | MA | SLI | SLO | SSI |
| 0x5 | NPRES | MA | SLI | SLO | SSI+ERRL |
| 0x6 | NPRES | MA | SLI | SLO | SSI+ERRH |
| 0x7 | NPRES | MA | SLI | SLO | ExtSSI |

Table 110: Target value of MODEA for the command SWITCH

| RPL_NEW | | Addr. SER: 0x60; bit 7:6 | |
|---------|--------------------|--------------------------|-----------------------|
| Code | Registerprotection | Command I2C_COM | Reset to RP0 possible |
| 0x0 | RP0 | x | x |
| 0x1 | RP1 | - | - |
| 0x2 | RP1 | x | x |
| 0x3 | RP1 | - | x |

Table 111: Target value for RPL for the command SWITCH

Command **CRC_VER** starts a verification of CRC16 and CRC8. In case of an crc error, the CRC_ERR status bit is set.

Command **CRC_CALC** starts a recalculation of CRC16 and CRC8. CRC16 and CRC8 are saved internally in iC-MU and are used for later CRC verifications.

The command **SET_MTC** sets pin MTC to logic level 1. **RES_MTC** resets pin MTC to logic level 0. iC-MU saves the actual logic level of pin MTD to MTD_STATUS before it sets or resets pin MTC. To use these commands MODE_MT has to be set to 0x0, i.e. no external multi-turn is configured.

| MTD_STATUS | | Addr. SER: 0x60; bit 0 |
|------------|---|------------------------|
| Code | Description | |
| 0 | MTD Pin was 0, before setting/resetting MTC | |
| 1 | MTD Pin was 1, before setting/resetting MTC | |

Table 112: Status of pin MTD before command execution SET_MTC and RES_MTC

Configurable NPRES Pin

A configurable NPRES pin can be used at pin PA0 if MODEA is set to 0x2-0x7. This pin can be used to execute a command configured by PA0_CONF on a falling edge of NPRES.

| PA0_CONF(7:0) Addr. 0x30; bit 7:0 | |
|---|---------------|
| PA0_CONF(7:0) Addr. SER: 0x25; bit 7:0 Bank 0 | |
| Code | Command |
| 0x00 | NO_FUNCTION |
| 0x01 | WRITE_ALL |
| 0x02 | WRITE_OFF |
| 0x03 | ABS_RESET |
| 0x04 | NON_VER |
| 0x05 | MT_RESET |
| 0x06 | MT_VER |
| 0x07 | SOFT_RESET |
| 0x08 | SOFT_PRES |
| 0x09 | SOFT_E2P_PRES |
| 0x0A | I2C_COM |
| 0x0B | EVENT_COUNT |
| 0x0C | SWITCH |
| 0x0D | CRC_VER |
| 0x0E | CRC_CALC |
| 0x0F | SET_MTC |
| 0x10 | RES_MTC |
| ...0xFF | no function |

Table 113: Command to be executed on falling edge of NPRES

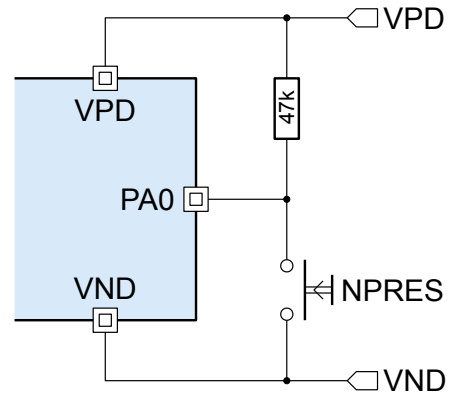


Figure 51: External circuitry for NPRES functionality

POSITION OFFSET VALUES AND PRESET FUNCTION

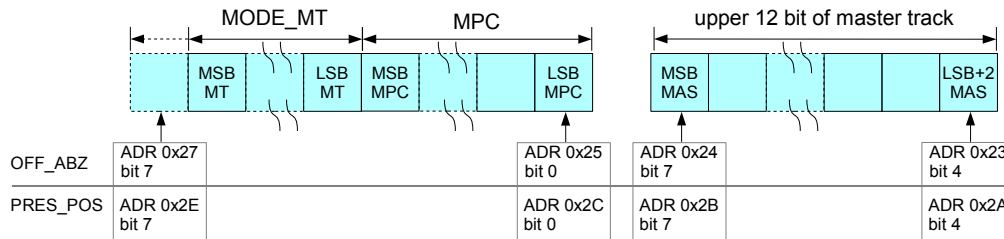


Figure 52: Position of the parameters OFF_ABZ and PRES_POS with respect to configured multiturn (MODE_MT), periods (MPC) and converter resolution

OFF_ABZ holds the position offset values stored in the EEPROM. After startup or the commands SOFT_RESET and ABS_RESET the OFF_ABZ values are amended to include the nonius data and the multiturn data (in case an external multiturn is configured) and stored as OFF_POS in the internal RAM. Value OFF_POS is subtracted with each conversion from the internally synchronized result. OFF_ABZ is not affected by the RESABZ parameter.

Preset function

The preset function corrects the output position value of the ABZ, SPI, or BiSS interface to the setpoint given by PRES_POS. Correction is initiated by writing command SOFT_PRESET or SOFT_E2P_PRESET to the command register (see page 60), or, if one of these commands is configured with PA0_CONF as NPRES command at PA0 pin, by a falling edge at NPRES. See Table 34 for configuration of NPRES and Table 113 for PA0_CONF.

| OFF_ABZ(3:0) | Addr. 0x23; bit 7:4 | |
|-----------------------|---|-------|
| OFF_ABZ(11:4) | Addr. 0x24; bit 7:0 | |
| OFF_ABZ(19:12) | Addr. 0x25; bit 7:0 | |
| OFF_ABZ(27:20) | Addr. 0x26; bit 7:0 | |
| OFF_ABZ(35:28) | Addr. 0x27; bit 7:0 | |
| OFF_ABZ(3:0) | Addr. SER:0x1E; bit 7:4 | Bank0 |
| OFF_ABZ(11:4) | Addr. SER:0x1F; bit 7:0 | Bank0 |
| OFF_ABZ(19:12) | Addr. SER:0x48; bit 7:0 | |
| OFF_ABZ(27:20) | Addr. SER:0x49; bit 7:0 | |
| OFF_ABZ(35:28) | Addr. SER:0x4A; bit 7:0 | |
| Code | Description | |
| 0x00000000 | Offset position relative to absolute position | |
| ... | | |
| 0xFFFFFFFF | | |

Table 114: Output offset position, relative to absolute position

| OFF_POS(19:12) | Addr. SER:0x20; bit 7:0 | Bank0, R |
|-----------------------|------------------------------------|----------|
| OFF_POS(27:20) | Addr. SER:0x21; bit 7:0 | Bank0, R |
| OFF_POS(35:28) | Addr. SER:0x22; bit 7:0 | Bank0, R |
| Code | Description | |
| 0x00000000 | Offset (is automatically computed) | |
| ... | | |
| 0xFFFFFFFF | | |

Table 115: Output position offset amended by the nonius/MT

When the preset function is started, the ABZ converter is stopped. The current position is then determined. The correction factor for output (OFF_POS) is calculated taking PRES_POS into account and stored in the internal RAM. Offset values OFF_ABZ are computed and if the command SOFT_E2P_PRESET is used written to the external EEPROM. The ABZ converter is then restarted.

| PRES_POS(3:0) | Addr. 0x2A; bit 7:4 |
|------------------------|-------------------------|
| PRES_POS(11:4) | Addr. 0x2B; bit 7:0 |
| PRES_POS(19:12) | Addr. 0x2C; bit 7:0 |
| PRES_POS(27:20) | Addr. 0x2D; bit 7:0 |
| PRES_POS(35:28) | Addr. 0x2E; bit 7:0 |
| PRES_POS(3:0) | Addr. SER:0x4D; bit 7:4 |
| PRES_POS(11:4) | Addr. SER:0x4E; bit 7:0 |
| PRES_POS(19:12) | Addr. SER:0x4F; bit 7:0 |
| PRES_POS(27:20) | Addr. SER:0x50; bit 7:0 |
| PRES_POS(35:28) | Addr. SER:0x51; bit 7:0 |
| Code | Description |
| 0x00000000 | Preset position |
| ... | |
| 0xFFFFFFFF | |

Table 116: Output position preset

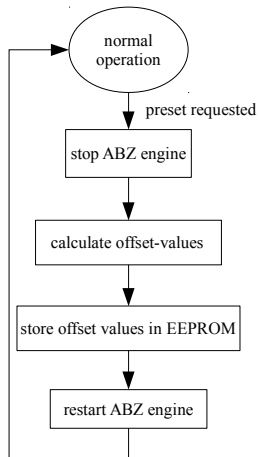


Figure 53: Preset sequence using command
SOFT_E2P_PRES

DESIGN REVIEW: Notes On Chip Functions

| iC-MU Y2/Y2H | | |
|--------------|--|--|
| No. | Function, Parameter/Code | Description and Application Notes |
| 1 | 3-track Nonius systems with two iC-MU MPC ≥ 0x7 | The period counter consistency error verification NON_CTR of the multiturn iC-MU (see Figure 42, iC-MU(2)) must be switched off → NCHK_NON = 0x1. |
| 2 | SPI interface (MODEA = 0x0, 0x1), Read/Write REGISTER(single) with access to EEPROM | SPI command sequence as in Figure 31. The end of a Read/Write REGISTER(single) command to an EEPROM address can be detected by checking the status bit BUSY. Register Status/Data and SPI-STATUS change from 0x02 (Busy) to 0x00. The status bits VALID/FAIL are without functionality. A successful I ² C communication between iC-MU and the EEPROM can be checked via STATUS1 flag EPR_ERR = 0. |
| 3 | SSI interface Gray coded MODEA = 0x4; GSSI = 0x1; OUT_ZERO = 0x0 | The level of the SSI output pin (signal SLO) can be "1" or "0" during timeout t_{fos} (see Figure 5). Therefore, a SSI timeout may not be detected by a SSI master in all cases. To obtain a reliable SSI timeout set parameter OUT_ZERO = 0x1 (includes a zero bit after position data) and send an additional clock pulse. |
| 4 | SSI interface Gray coded with error bit MODEA = 0x5 or 0x6; GSSI = 0x1; OUT_ZERO = 0x0 | Conversion of the SSI position data into Gray code requires following procedure: By setting parameter OUT_ZERO = 0x1 (includes a zero bit after position data) and sending an additional clock pulse and subsequently ignoring the additional ZERO bit, the singleturn data is converted correctly into Gray code. |
| 5 | Multiturn system - Using iC-MU and iC-PVL with a shared EEPROM | When iC-MU and iC-PVL share an EEPROM for configuration in a multiturn set-up, special care is required to configure iC-MU on the initial startup of the system when iC-PVL also tries to read its configuration from the EEPROM. Once iC-PVL is configured and connected to a backup power source via pin VBAT, it no longer tries to read the EEPROM on consecutive VDD power cycles. This allows the iC-MU to successfully configure itself on every VDD power cycle. For a reliable configuration of iC-MU via the EEPROM on the initial startup of such an iC-MU and iC-PVL based system (install backup power source → power on), it is recommended to either send a SOFT_RES command to iC-MU, or to power cycle the system after the initial startup procedure. This causes the iC-MU to read in the configuration data from the EEPROM again. |
| 6 | Port A = BiSS, SSI, SSI+ERRL, SSI+ERRH or ExtSSI (MODEA = 0x2, 0x4 to 0x7) | After power-up, the first position readout is shifted by one bit and should be discarded. To avoid this, either a clock pulse must be sent to initialize the serial interface or the potential at pin PA1 must be below 0.4V until the digital power supply VPD has exceeded 2.0V. In 3-track systems a configuration according to Table 68 must be used. For 512 and 1024 master period systems an ABS_RESET command must be applied to finalize the encoder start-up sequence. |
| 7 | Restrictions on Nonius phase margin / analog offset | Especially for the low Rth and thus larger QFN48-7x7 package the specific mechanical properties and package stress on board can cause increased analogue offset within the Nonius track (in particular with lower quality targets with 64/63 pole pairs; parameter MPC = 0x6). A significantly reduced Nonius phase margin would be indicated by the iC-MU as a NON_CTR error. A NON_CTR error can cause an incorrect absolute position when the system is restarted. iC-MU fits into the smaller DFN16-5x5 package with its advantages regarding required board space and lower mechanical package stress on board. Especially for the alternative lower Rth QFN48-7x7 packages sufficient Nonius phase margin requires - besides good quality magnetic targets and mechanical adjustment - thorough initial calibration at room temperature or a reduced operating temperature range. Safe operation can be determined e.g. by measuring the Nonius curve over the whole operating temperature range. For further information please request Application Note MU AN16 at support@ichaus.de. |
| 8 | Restrictions on FILT setting 0x6 (51dB) | For encoder systems with total GAIN values (ACGAIN_x * AFGAIN_x) less than 30-fold at room temperature, FILT setting 0x6 (51dB) is not recommended. Otherwise the Nonius calculation at start-up may fail, indicated by a NON_CTR error. |

Table 117: Notes on chip functions regarding iC-MU chip release Y2 and Y2H

iC-MU MAGNETIC OFF-AXIS POSITION ENCODER - POLE WIDTH 1.28MM



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| iC-MU Y2/Y2H | | |
|--------------|---|--|
| No. | Function, Parameter/Code | Description and Application Notes |
| 9 | Port A = SSI, SSI+ERRL, SSI+ERRH or ExtSSI (MODEA = 0x4 to 0x7) | If a switching edge is detected (Elec. Char. 901 & 902) at input MA during the Power-up Time (Elec. Char. 107) of iC-MU, the very first position word is output as zero. In operating modes SSI+ERRL, SSI+ERRH and ExtSSI the error bit is active in that case. All consecutive position words contain the valid position value and the error bit is cleared. |
| 10 | Restrictions on Multiturn interface daisy chain (GET_MT=1) | The MT interface daisy chain mode is designed for calibration and configuration purposes only. Precautions have to be taken into account if the BiSS frequency is higher as the usual clock period (see Elec. Char. 1001). Depending on the FILT settings it is necessary to have an appropriate idle time between BiSS requests to ensure that the signal conditioning for master and nonius channel are not affected by the pulses on pin MTC and MTD. For FILT=0 a minimum idle time of 50 μ s is recommended. For FILT=1..6 a minimum idle time of 300 μ s is recommended. |

Table 118: Notes on chip functions regarding iC-MU chip release Y2 and Y2H

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REVISION HISTORY

| Rel. | Rel. Date ³ | Chapter | Modification | Page |
|------|------------------------|---------|-----------------|------|
| B1 | 2013-04-30 | | Initial Release | |

| Rel. | Rel. Date ³ | Chapter | Modification | Page |
|------|------------------------|---------|---|------|
| C2 | 2015-11-02 | | Please refer to former datasheet release D1 | |

| Rel. | Rel. Date ³ | Chapter | Modification | Page |
|------|------------------------|---------|---|------|
| C3 | 2016-12-21 | | Please refer to former datasheet release D1 | |

| Rel. | Rel. Date ³ | Chapter | Modification | Page |
|------|------------------------|--|--|------|
| D1 | 2017-09-18 | ELECTRICAL CHARACTERISTICS | Item 407: max. value changed from 30MHz to 32MHz | 9 |
| | | REGISTER ASSIGNMENTS (EEPROM) | Table 11 revised | 19 |
| | | ANALOG SIGNAL CONDITIONING FLOW: x = M,N | Added note box with hyperlink to app note AN3 | 23 |
| | | CONFIGURABLE I/O INTERFACE | Formula to calculate data length corrected | 30 |
| | | STATUS REGISTER AND ERROR MONITORING | Table 98: enhanced notes | 58 |
| | | DESIGN REVIEW: Notes On Chip Functions | Table 117: added chip revision Y2H | 66 |

| Rel. | Rel. Date ³ | Chapter | Modification | Page |
|------|------------------------|---|---|-------------|
| E1 | 2018-10-16 | | Added package QFN48-7x7 | 5, 7, 8, 71 |
| | | PACKAGING INFORMATION | Updated package dimension DFN16-5x5 drawing | 6 |
| | | OPERATING CONDITIONS: I/O Interface | Item I115 and I119: max. value corrected Item I116: min. value changed from 100 ns to 200 ns, max. value removed Item I117 and I118: min. value changed from 50 ns to 100 ns Item I120: max. value removed | 12 |
| | | ANALOG SIGNAL CONDITIONING FLOW: x = M,N | Added note: in test mode TEST = 0x1F the I2C communication is disabled | 23 |
| | | EEPROM AND I2C INTERFACE | Chapter renamed: original name was 'I2C INTERFACE AND STARTUP BEHAVIOR' Description enhanced, added Table 26 and 27 Part 'STARTUP BEHAVIOR' was removed into a new chapter | 25 |
| | | STARTUP BEHAVIOR | New chapter, the content has been taken from the original chapter 'I2C INTERFACE AND STARTUP BEHAVIOR' without modification | 27 |
| | | INCREMENTAL OUTPUT ABZ, STEP/DIRECTION AND CW/CCW | Enhanced description re. linear application and min. increment | 48 |
| | | STATUS REGISTER AND ERROR MONITORING | Description of status flag STUP enhanced Table 99 description of status flag MT_ERR enhanced | 58 |
| | | COMMAND REGISTER | Description of command SWITCH enhanced | 61 |

| Rel. | Rel. Date ³ | Chapter | Modification | Page |
|------|------------------------|---|--|------|
| E2 | 2019-12-20 | OPERATING REQUIREMENTS | SPI Interface: Updated operating conditions SPI interface Updated Figure 2 | 12 |
| | | CONFIGURABLE I/O INTERFACE | Added information on analog mode output voltages to Table 35 | 29 |
| | | CONFIGURABLE I/O INTERFACE | Added information on MISO idle state = high in SPI mode | 35 |
| | | CONFIGURABLE I/O INTERFACE | Updated Table 52 | 38 |
| | | MT INTERFACE | Updated 3 track system description | 46 |
| | | INCREMENTAL OUTPUT ABZ, STEP/DIRECTION AND CW/CCW | Description of parameter SS_AB impact improved | 49 |
| | | COMMAND REGISTER | Improved I2C_COM command description | 61 |
| | | DESIGN REVIEW: Notes On Chip Functions | Added item 5 for iC-MU Y2/Y2H | 66 |
| | | DESIGN REVIEW: Notes On Chip Functions | Added item 6 for iC-MU Y2/Y2H | 66 |
| | | DESIGN REVIEW: Notes On Chip Functions | Removed design review for chip revision Y1 and Z. Please refer to former datasheet release E1. | 66 |

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| Rel. | Rel. Date ³ | Chapter | Modification | Page |
|------|------------------------|---|---|--------|
| E3 | 2020-04-08 | DESCRIPTION | Removed BiSS-Disclaimer | 2 |
| | | DESCRIPTION | Added Note on system responsibility | 2 |
| | | THERMAL DATA | Updated: Rthja according to JESD51 | 8 |
| | | I/O Interface | Corrected pin designation in SPI timing diagram | 12 |
| | | EEPROM AND I2C INTERFACE | Corrected Table 28 and Table 29 star symbol | 25, 26 |
| | | REGISTER ACCESS THROUGH SERIAL INTERFACE (SPI AND BISS) | Added note: Burst mode is not supported by iC-MU for write access to the registers. | 52 |
| | | REGISTER ACCESS THROUGH SERIAL INTERFACE (SPI AND BISS) | Amended HARD_REV table with all iC-MU Series versions | 55 |
| | | REGISTER ACCESS THROUGH SERIAL INTERFACE (SPI AND BISS) | Chip revision Y2H added to Table 94 | 55 |
| | | COMMAND REGISTER | Added Note on SWITCH command usage with an empty EEPROM | 62 |
| | | DESIGN REVIEW: Notes On Chip Functions | Added item 7: Restrictions on Nonius phase margin / analog offset | 66 |
| | | DESIGN REVIEW: Notes On Chip Functions | Minor corrections to the wording | 66 |

| Rel. | Rel. Date ³ | Chapter | Modification | Page |
|------|------------------------|---|--|------|
| F1 | 2021-01-12 | all | Minor spelling and wording corrections | all |
| | | all | Renamed parameter ROT to ROT_ALL to be consistent with iC-MU150 / iC-MU200 nomenclature | all |
| | | FEATURES | Updated system resolution statement | 1 |
| | | ELECTRICAL CHARACTERISTICS | Updated Elec. Char. Item No.509: min 5.0V → 4.9V and Item No. A03: max -1.5mA → -1.4mA | 10 |
| | | ELECTRICAL CHARACTERISTICS | Added Elec. Char. No. 510 | 10 |
| | | PRINCIPLE OF MEASUREMENT | Added maximum system resolution to Table 6 and Table 7. Added absolute measurement length to Table 7 | 14 |
| | | CONFIGURABLE I/O INTERFACE | Corrected typo in Table 35, VNA → VPA | 29 |
| | | CONVERTER AND NONIUS CALCULATION | Added maximum system resolution to Table 54 | 40 |
| | | CONVERTER AND NONIUS CALCULATION | Added remark regarding permissible Nonius phase deviation | 41 |
| | | MT INTERFACE | Added remark regarding permissible Nonius phase deviation | 46 |
| | | REGISTER ACCESS THROUGH SERIAL INTERFACE (SPI AND BISS) | Correction: RESERVED memory area 0x83 - 0xAF in Table 93. | 55 |
| | | DESIGN REVIEW: Notes On Chip Functions | Added item no. 8: Restrictions on FILT setting 0x6 (51dB) | 66 |

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| Rel. | Rel. Date ³ | Chapter | Modification | Page |
|------|------------------------|---|--|--------|
| F2 | 2021-07-22 | REGISTER ASSIGNMENTS (EEPROM) | Corrected BiSS EDS register byte order in Table 8, 9, 10, 12, 13 | 18, 19 |
| | | STARTUP BEHAVIOR, CONFIGURABLE I/O INTERFACE | Clarified that after failure to read EEPROM and with with PA0 = 1 iC-MU will switch to SPI _{TR1} | 27, 29 |
| | | CONFIGURABLE I/O INTERFACE | Added information that BiSS protocol commands are not supported by iC-MU. | 32 |
| | | MT INTERFACE | Updated 3-track Nonius system settings in Table 68 | 46 |
| | | MT INTERFACE | Added remark regarding Design Review item no. 10 | 47 |
| | | REGISTER ACCESS THROUGH SERIAL INTERFACE (SPI AND BISS) | Corrected BiSS EDS register byte order in Table 93 | 55 |
| | | COMMAND REGISTER | Added more information on command register behaviour. | 60 |
| | | COMMAND REGISTER | Added remark that after issuing the SOFT_RESET command no further communication attempt with iC-MU may be made for at least 50ms | 61 |
| | | DESIGN REVIEW: Notes On Chip Functions | Amended item no. 6 regarding 3-track system requirements | 66 |
| | | DESIGN REVIEW: Notes On Chip Functions | Amended item no. 6 with ExtSSI mode. | 66 |
| | | DESIGN REVIEW: Notes On Chip Functions | Added item no. 9: Switching edges on MA during startup in SSI, SSI+ERRL, SSI+ERRH or ExtSSI mode. | 67 |
| | | DESIGN REVIEW: Notes On Chip Functions | Added item no. 10: Restrictions on Multiturn interface daisy chain (GET_MT=1) | 67 |

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³ Release Date format: YYYY-MM-DD

iC-MU MAGNETIC OFF-AXIS
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ORDERING INFORMATION

| Type | Package | Options | Order Designation |
|-------|---------------------|--|-------------------|
| iC-MU | 16-pin DFN 5 x 5 mm | Pin compatible with iC-MU150 | iC-MU DFN16-5x5 |
| | 48-pin QFN 7 x 7 mm | Pin compatible with iC-MU150 and iC-MU200 | iC-MU QFN48-7x7 |

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