iC-MHL100 12-BIT LINEAR / ROTARY POSITION HALL ENCODER - POLE WIDTH 1.00 mm

preliminary

FEATURES

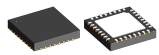
- Realtime system for linear speed up to 4 m/s at full resolution
- Absolute position within the magnetic period of 2 mm
- 12-bit interpolation w. 4096 increments, resolution better 0.5 µm
- Automatic signal offset compensation
- Automatic amplitude control for optimum operating point
- Programmable features: interpolation factor, hysteresis, minimum phase distance, zero position and code direction
- Electronic index generation with multi-purpose enable input
- RS422-compatible A/B/Z outputs for encoder quadrature signals with up to 8 MHz edge rate
- UVW commutation signals for EC motor applications
- BiSS/SSI interface for high-speed serial data output (BiSS/SSI) and configuration (BiSS)
- Zener-Zap ROM for non-volatile setup and OEM data
- Signal monitoring: loss of signal, excessive frequency
- Single 5 V supply
- Extended temperature range of -40 to +125 °C

APPLICATIONS

- Motion control
- Linear position encoders
- Incremental off-axis rotary encoders
- Brushless motors

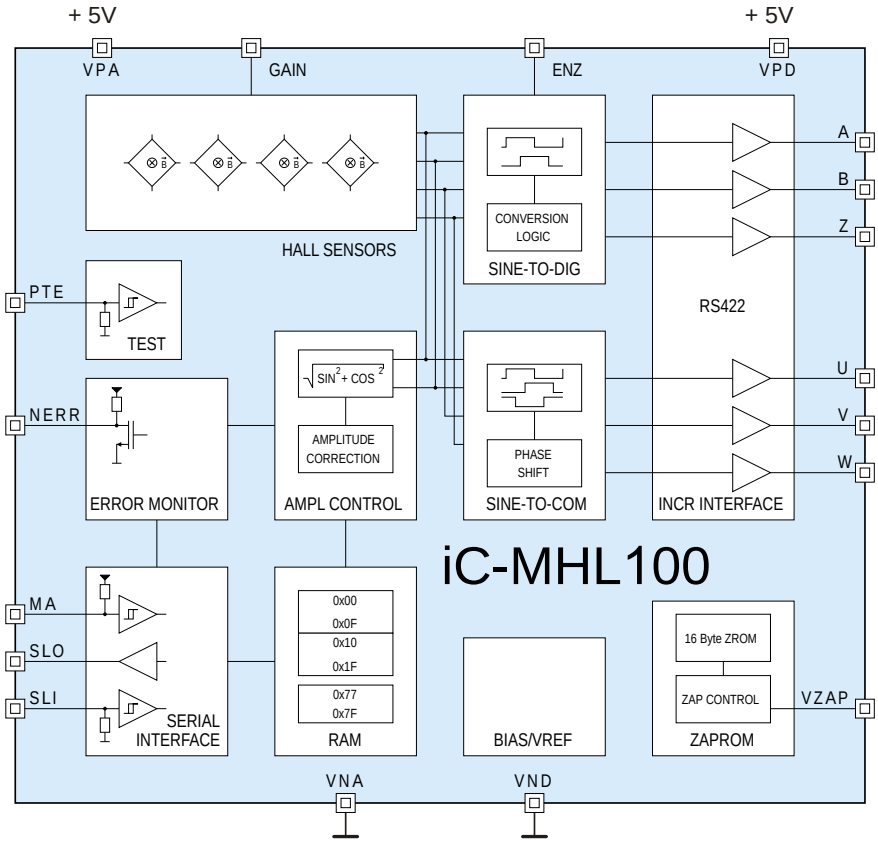
PACKAGES

TSSOP20
6.4 mm x 6.5 mm x 1 mm
RoHS compliant



QFN32
5 mm x 5 mm
RoHS compliant, available on request

BLOCK DIAGRAM



DESCRIPTION

The iC-MHL100 is a magnetic position sensor with integrated Hall sensors for the scanning of magnetic tapes and pole wheels featuring a pole pitch of 1 mm. Moving speeds of up to 4 m/s can be followed even at highest resolution representing 0.49 µm.

The signal conditioning unit generates constant-amplitude sine and cosine voltages that are used for real-time tracking sine-to-digital angle conversion. The resolution can be programmed up to a maximum of 4096 increments within one magnetic period of 2 mm.

The integrated BiSS interface enables daisy-chain operation of multiple devices with a synchronous position capture at all networked sensors. The device's memory can also be accessed via the bidirectional BiSS C protocol without interfering the readout cycles.

The incremental interface with the pins A, B and Z supplies encoder quadrature signals at an edge rate of up to 8 MHz. Complementary incremental signals are available at the U, V, W outputs. The index position at the Z output is adjustable and can be gated via enable input ENZ.

An additional converter operates for commutation signals UVW. The resolution of the interface depends on the pole pair count of the magnetic target. For instance, with a magnetic target of 10 pole pairs a EC-motor with 10 or 20 pole pairs can be commutated depending on chip setting. The zero point of the commutation signals can be set separately from the quadrature converter.

A/B/Z and U/V/W form RS422-compatible outputs and are programmable regarding the output's drive current and slew rate.

A gain-dependent analog signal is available at the GAIN output, which can be used to monitor mechanical alignment of the sensor with respect to the magnetic target.

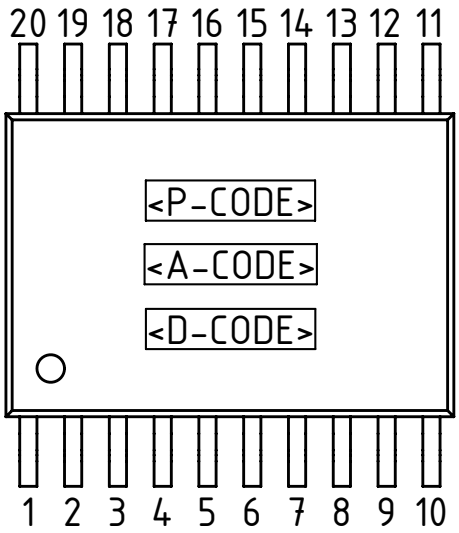
All device parameters can be stored in the internal non-volatile Zener-zapping ROM to allow self-configuration after power on. The required writing algorithm for programming is executed by the IC itself.

Together with the appropriate magnetic scale or pole wheel, the iC-MHL100 provides a single-chip solution for linear and rotary encoders.

The device described here is a multifunctional iC that contains integrated BiSS C interface components. The BiSS C process is protected by patent DE 10310622 B4 owned by iC-Haus GmbH and its application requires the conclusion of a license (free of charge).
Download the license at www.biss-interface.com/bua

PACKAGING INFORMATION TSSOP20 and QFN32-5x5

PIN CONFIGURATION TSSOP20



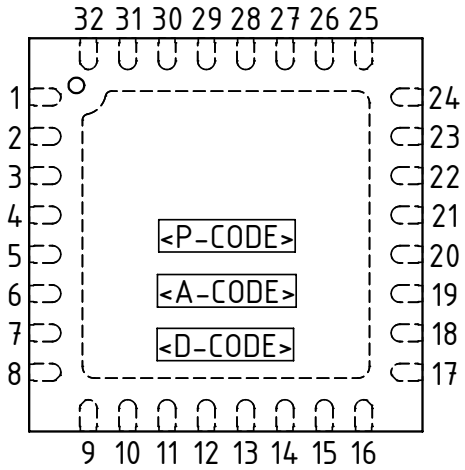
PIN FUNCTIONS

No.	Name	Function
1	SLI[1)]	BiSS Interface, Data Input
2	MA	BiSS Interface, Clock Input
3	VPA	+5 V Supply Voltage (analog)
4	VNA	Ground (analog)
5	nc	not connected
6	nc	not connected
7	VZAP	Zener Zapping Programming Voltage
8	A	Incremental Output A (+ NU)
9	B	Incremental Output B (+ NV)
10	Z	Index Output Z (+ NW)
11	VND	Ground (digital)
12	VPD	+5 V Supply Voltage (digital)
13	U	Commutation U (+NA)
14	V	Commutation V (+NB)
15	W	Commutation W (+NZ)
16	PTE[1)]	Test Enable Pin (iC-Haus use only)
17	NERR	Error Output (active low)
18	GAIN	Gain-Signal
19	ENZ	Enable Index Z
20	SLO	BiSS Interface, Data Output

[1)] If not used, the pin must be connect to VNA, VND.

IC top marking:
<P-CODE> = product code
<A-CODE> = assembly code (subject to changes)
<D-CODE> = date code (subject to changes)

PIN CONFIGURATION QFN32-5x5



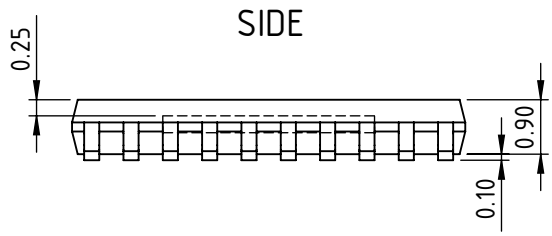
PIN FUNCTIONS

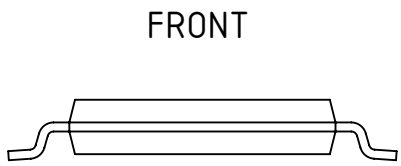
No.	Name	Function
1,2,3	nc	not connected
4	ENZ	Enable Index Z
5	SLO	BiSS Interface, Data Output
6	SLI[1]	BiSS Interface, Data Input
7	MA	BiSS Interface, Clock Input
8,9	nc	not connected
10	VPA	+5 V Supply Voltage (analog)
11	VNA	Ground (analog)
12,13	nc	not connected
14	VZAP	Zener Zapping Programming Voltage
15	A	Incremental Output A (+ NU)
16,17	nc	not connected
18	B	Incremental Output B (+ NV)
19	Z	Index Output Z (+ NW)
20	VND	Ground (digital)
21	VPD	+5 V Supply Voltage (digital)
22,23	nc	not connected
24,25	nc	not connected
26	U	Commutation U (+NA)
27	V	Commutation V (+NB)
28	W	Commutation W (+NZ)
29	PTE[1]	Test Enable Pin (iC-Haus use only)
30	NERR	Error Output (active low)
31	GAIN	Gain-Signal
32	nc	not connected
	TP[2]	Backside paddle

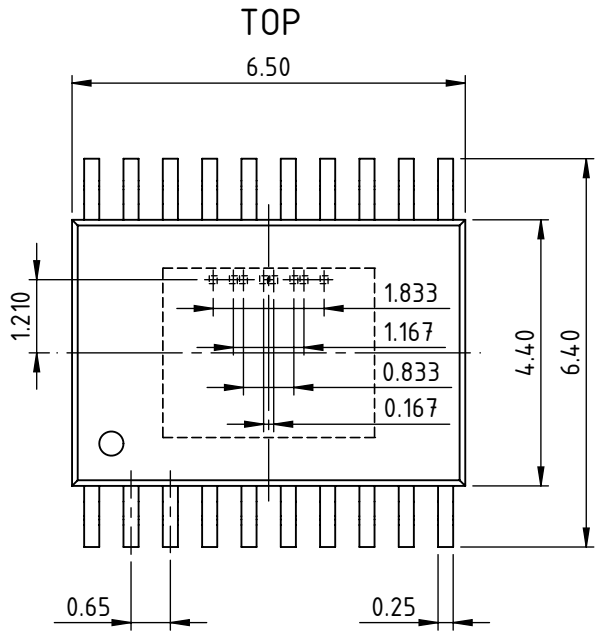
[1] If not used, the pin must be connect to VNA, VND.
[2] The *Backside Paddle* is to be connected to VNA on the PCB.

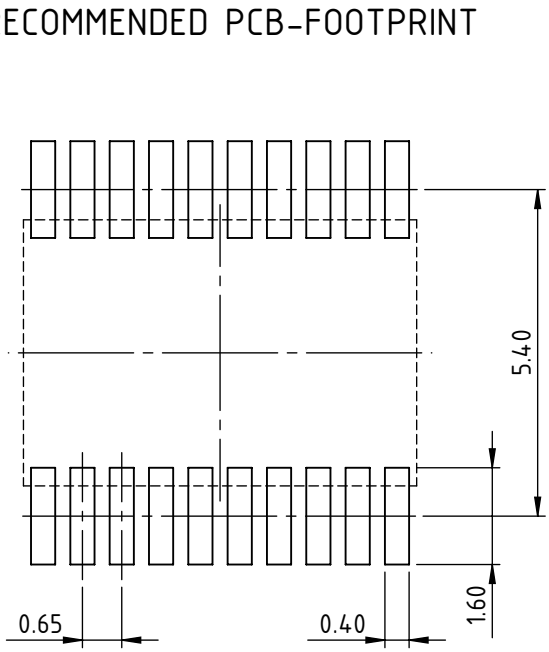
IC top marking:
<P-CODE> = product code
<A-CODE> = assembly code (subject to changes)
<D-CODE> = date code (subject to changes)
Orientation of the top marking is subject to alteration.

PACKAGE DIMENSIONS TSSOP20





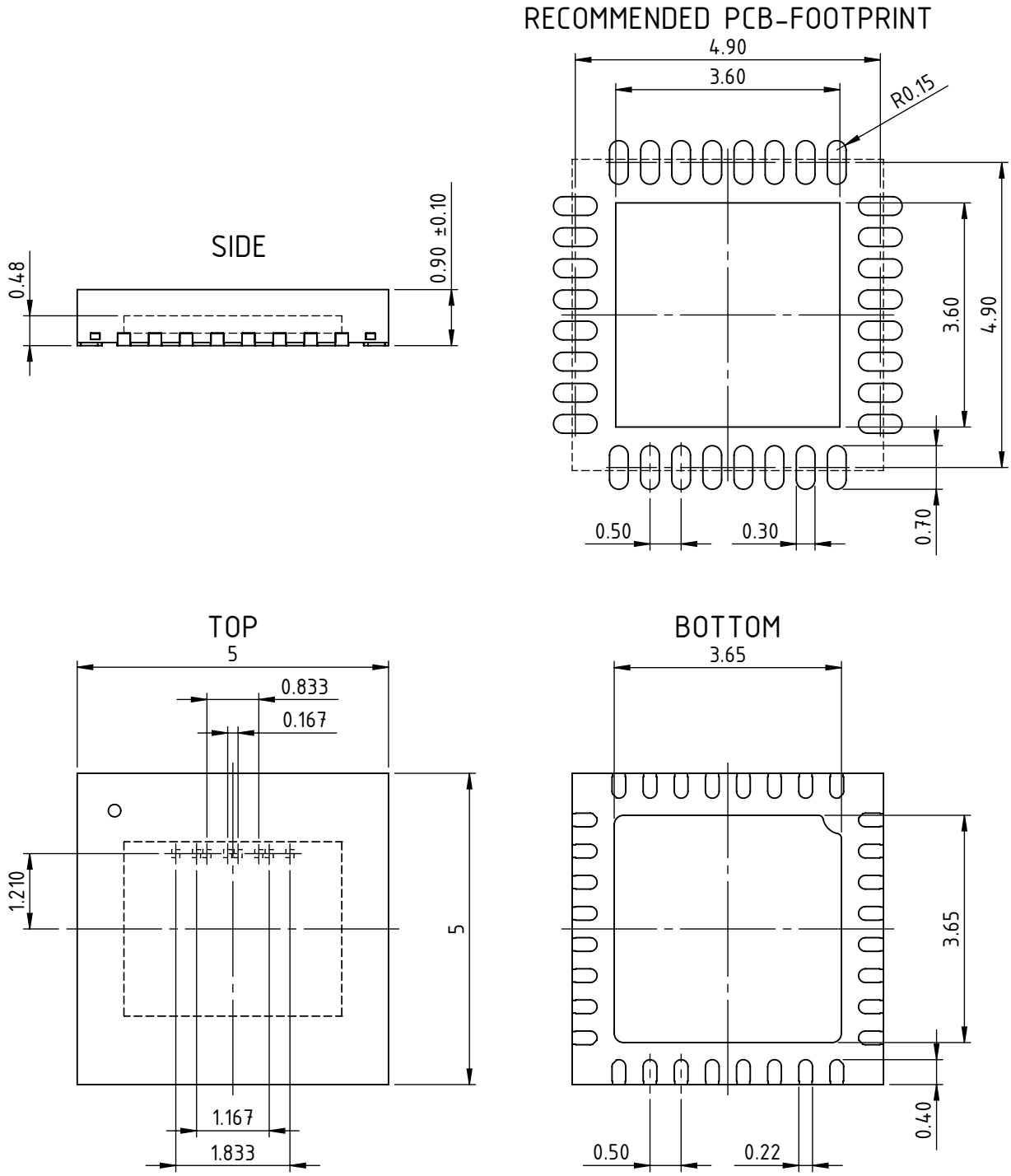




All dimensions given in mm. Tolerances of form and position according to JEDEC MO-153.
Tolerance of sensor pattern: ±0.15mm / ±1° (with respect to center of body).

dra_tssop20-1_mhl100_0_pack_1, 8:1

PACKAGE DIMENSIONS QFN32-5x5



All dimensions given in mm. Tolerances of form and position according to JEDEC MO-220.
Tolerance of sensor pattern: ±0.10mm / ±1° (with respect to center of backside pad).

dra_qfn32-5x5-6_mhl100_0_pack_1, 10:1

ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	V()	Voltage at VPA, VPD		-0.3	6	V
G002	V(VZAP)	Zapping Voltage		-0.3	8	V
G003	V()	Voltages at A, B, Z, U, V, W, MA, SLO, SLI, NERR, PTE		-0.3	6	V
G004	I()	Current in VPA		-10	20	mA
G005	I()	Current in VPD		-20	200	mA
G006	I()	Current in A, B, Z, U, V, W		-100	100	mA
G007	I()	Current in MA, SLO, SLI, NERR, PTE		-10	10	mA
G008	Vd()	ESD-voltage, all Pins	HBM 100 pF discharged over 1.5 kΩ		2	kV
G009	Ts	Storage Temperature		-40	150	°C
G010	Tj	Junction Temperature		-40	150	°C

THERMAL DATA

Operating conditions: VPA, VPD = 5 V ±10 %

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Ambient Temperature		-40		125	°C
T02	Rthja	Thermal Resistance Chip/Ambient	TSSOP20 package mounted on PCB		100		K/W

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating conditions:
VPA, VPD = 5 V ±10 %, Tj = -40...125 °C, IBM adjusted to 200 µA , unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
General							
001	V(VPA, VPD)	Permissible Supply Voltage		4.5		5.5	V
002	I(VPA)	Supply Current in VPA			5	8	mA
003	I(VPD)	Supply Current in VPD	PRM = 0, without load		10	18	mA
004	I(VPD)	Supply Current in VPD	PRM = 1, without load		4	8	mA
005	Vc(hi)	Clamp-Voltage hi at MA, SLI, SLO, PTE, NERR	Vc()hi = V() – VPD, I() = 1 mA	0.4		1.5	V
006	Vc(lo)	Clamp-Voltage lo	I() = -1 mA	-1.5		-0.3	V
Hall Sensors and Signal Conditioning							
101	Hext	Operating Magnetic Field Strength	at chip surface	20		100	kA/m
102	fmag	Operating Magnetic Field Frequency Linear Speed	with resolution set to 4 096, MTD set to 125 ns			2 4	kHz m/s
108	Vos	Trimming Range of Output Offset Voltage	VOSS or VOSC = 0x7F			-55	mV
109	Vos	Trimming Range of Output Offset Voltage	VOSS or VOSC = 0x3F	55			mV
110	Vopt	Optimal Differential Output Voltage	Vopt = Vpp(PSIN) – Vpp(NSIN), ENAC = 0, see Figure 7		4		Vpp
Amplitude Control							
201	Vampl	Differential Output Amplitude	Vampl = Vpp(PSIN) – Vpp(NSIN), ENAC = 1, see Figure 7	3.2		4.8	Vpp
202	Vratio	Amplitude Ratio	Vratio = Vpp(PSIN) / Vpp(PCOS)	1.09			
203	Vratio	Amplitude Ratio	Vratio = Vpp(PSIN) / Vpp(PCOS)			0.92	
204	tampl	Settling Time of Amplitude Control	±10%			300	µs
205	Vae()lo	Amplitude Error Threshold for MINERR	Vpp(PSIN) – Vpp(NSIN)	1.1		2.8	Vpp
206	Vae()hi	Amplitude Error Threshold for MAXERR	Vpp(PSIN) – Vpp(NSIN)	4.9		5.8	Vpp
Bandgap Reference							
401	Vbg	Bandgap Reference Voltage		1.18	1.25	1.32	V
402	Vref	Reference Voltage		45	50	55	%VPA
403	Iibm	Bias Current	CIBM = 0x0 CIBM = 0xF Bias Current adjusted	 -370 -220	 -200	-100 -180	µA µA µA
404	VPDon	Turn-on Threshold VPD, System on	V(VPD) – V(VND), increasing voltage	3.65	4.0	4.3	V
405	VPDoff	Turn-off Threshold VPD, System reset	V(VPD) – V(VND), decreasing voltage	3	3.5	3.8	V
406	VPDhys	Hysteresis System on/reset		0.3			V
407	Vosr	Reference Voltage Offset Compensation		475	500	525	mV

ELECTRICAL CHARACTERISTICS

Operating conditions:
VPA, VPD = 5 V ±10 %, Tj = -40...125 °C, IBM adjusted to 200 µA , unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Clock Generation							
501	f()sys	System Clock	bias current adjusted	0.85	1.0	1.2	MHz
502	f()sdc	Sine-to-Digital Converter Clock	bias current adjusted	14	16	18	MHz
Sine-to-Digital Converter							
602	AAabs	Absolute Angular Accuracy	Vpp() = 4 V, adjusted	-0.35		0.35	Deg
603	AArel	Relative Angular Accuracy	with reference to one output period at A, B, at Resolution 1 024, see Figure 18	-15	±10	15	%
604	f()ab	Output Frequency at A, B	CFGMTD = 0 CFGMTD = 1		0.5 2.0		MHz MHz
605	REScom	Resolution of Commutation Converter			1.875		Deg
606	AAabs	Absolute Angular Accuracy of Commutation Converter		-0.5		0.5	Deg
BiSS Interface, Digital Output SLO, Digital Inputs MA, SLI							
701	Vs(SLO)hi	Saturation Voltage hi	V(SLO) = V(VPD) – V(), I(SLO) = 4 mA			0.4	V
702	Vs(SLO)lo	Saturation Voltage lo	I(SLO) = 4 mA to VND			0.4	V
703	Isc(SLO)hi	Short-Circuit Current hi	V(SLO) = V(VND), 25 °C	-90	-50		mA
704	Isc(SLO)lo	Short-Circuit Current lo	V(SLO) = V(VPD), 25 °C		50	80	mA
705	tr(SLO)	Rise Time SLO	CL = 50 pF			60	ns
706	tf(SLO)	Fall Time SLO	CL = 50 pF			60	ns
707	Vt()hi	Threshold Voltage hi: MA, SLI				2	V
708	Vt()lo	Threshold Voltage lo: MA, SLI		0.8			V
709	Vt()hys	Threshold Hysteresis: MA, SLI		150	250		mV
710	Ipd(SLI)	Pull-up Current: MA, SLI	V() = 0...VPD – 1 V	6	30	60	µA
711	Ipu(MA)	Pull-Up Current 30 µA MA		-60	-30	-6	µA
712	f()MA	Permissible Frequency at MA				10	MHz
Zapping ROM and Test VZAP, PTE							
801	Vt()hi	Threshold Voltage hi VZAP, PTE	with reference to VND			2	V
802	Vt()lo	Threshold Voltage lo VZAP, PTE	with reference to VND	0.8			V
803	Vt()hys	Hysteresis	Vt()hys = Vt()hi – Vt()lo	100	250		mV
804	Vt()nozap	Threshold Voltage Nozap VZAP	V() = V(VZAP) – V(VPD), V(VPD) = 5 V ±5 %, at chip temperature 27 °C	0.8			V
805	Vt()zap	Threshold Voltage Zap VZAP	V() = V(VZAP) – V(VPD), V(VPD) = 5 V ±5 %, at chip temperature 27 °C			1.2	V
806	V()zap	Zapping Voltage	PROG = 1	6.9	7.0	7.1	V
807	V()zpd	Diode voltage, Zapped	for iC-Haus chip test only			2	V
808	V()uzpd	Diode Voltage, Unzapped	for iC-Haus chip test only	3			V
809	Rpd()VZAP	Pull-down Resistor at VZAP	V() = 0 V...V(VPD)	30		55	kΩ
Error Monitor NERR							
901	Vt()hi	Input Threshold Voltage hi	with reference to VND			2	V
902	Vs()lo	Saturation Voltage lo	I() = 4 mA , with reference to VND			0.4	V
903	Vt()lo	Input Threshold Voltage lo	with reference to VND	0.8			V
904	Vt()hys	Input Hysteresis	Vt()hys = Vt()hi – Vt()lo	150	250		mV
905	Ipu(NERR)	Pull-up Current	V(NERR) = 0...VPD – 1 V	-750	-300	-80	µA
906	Isc()lo	Short-Circuit Current NERR	V(NERR) = V(VPD), 25 °C		50	80	mA
907	tf(NERR)	Decay Time NERR	CL = 50 pF			60	ns

ELECTRICAL CHARACTERISTICS

Operating conditions:
VPA, VPD = 5 V ±10 %, Tj = -40...125 °C, IBM adjusted to 200 µA , unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Line Driver Outputs A, B, Z, U, V, W							
P01	Vs()hi	Saturation Voltage hi	Vs() = VPD − V(); CFGDR(1:0) = 00, I() = -4 mA CFGDR(1:0) = 01, I() = -50 mA CFGDR(1:0) = 10, I() = -50 mA CFGDR(1:0) = 11, I() = -20 mA			 200 700 700 400	 mV mV mV mV
P02	Vs()lo	Saturation Voltage lo	CFGDR(1:0) = 00, I() = -4 mA CFGDR(1:0) = 01, I() = -50 mA CFGDR(1:0) = 10, I() = -50 mA CFGDR(1:0) = 11, I() = -20 mA			200 700 700 400	mV mV mV mV
P03	Isc()hi	Short-Circuit Current hi	V() = 0 V; CFGDR(1:0) = 00 CFGDR(1:0) = 01 CFGDR(1:0) = 10 CFGDR(1:0) = 11	 -12 -125 -125 -60		 -4 -50 -50 -20	 mA mA mA mA
P04	Isc()lo	Short-Circuit Current lo	V() = VPD; CFGDR(1:0) = 00 CFGDR(1:0) = 01 CFGDR(1:0) = 10 CFGDR(1:0) = 11	 4 50 50 20		 12 125 125 60	 mA mA mA mA
P05	Ilk()tri	Leakage Current Tristate	TRIHL(1:0) = 11	-100		100	µA
P06	tr()	Rise-Time lo to hi at Q	RL = 100 Ω to VND; CFGDR(1:0) = 00 CFGDR(1:0) = 01 CFGDR(1:0) = 10 CFGDR(1:0) = 11	 5 5 50 5		 20 20 350 40	 ns ns ns ns
P07	tf()	Fall-Time hi to lo at Q	RL = 100 Ω to VND; CFGDR(1:0) = 00 CFGDR(1:0) = 01 CFGDR(1:0) = 10 CFGDR(1:0) = 11	 5 5 50 5		 20 20 350 40	 ns ns ns ns
Output Monitor GAIN							
Q01	RES()	Digital-to-Analog Converter Resolution			8		bit
Q02	Iload()	Permissible Output Current		-1		1	mA
Q03	dV0()hi	Output Voltage hi, Rail-to-Rail	dV0()hi = V(VPA) - V(GAIN); I() = -1 mA ENAC = 0; GAINF = 0x3E			250	mV
Q04	dV0()lo	Output Voltage lo, Rail-to-Rail	I() = 1 mA ENAC = 0; GAINF = 0x02			250	mV
Q05	Ilk()	Leakage Current	V(GAIN) = 0...VPA, CFGTRIG = 1	-5		5	µA
Q06	SR()hi	Slew Rate hi	V(GAIN): 20% → 80% of range	2			V/µs
Q07	SR()lo	Slew Rate lo	V(GAIN): 80% → 20% of range	2			V/µs
Index Gating Input ENZ							
R01	Vt()hi	Threshold Voltage hi ENZ				2	V
R02	Vt()lo	Threshold Voltage lo ENZ		0.8			V
R03	Vt()hys	Threshold Hysteresis ENZ		100	250		mV
R04	Ipd(ENZ)	Pull-down Current 30 µA ENZ	V() = 1 V...V(VPD)	6	30	60	µA

OPERATING REQUIREMENTS: Serial Interface

Operating conditions: VPA, VPD = 5 V ±10 %, Ta = -40...125 °C, IBM calibrated to 200 µA;
Logic levels referenced to VND: lo = 0...0.45 V, hi = 2.4 V...VPD

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
SSI Protocol (ENSSI = 1)						
I001	T_{MAS}	Permissible Clock Period	t_{out} determined by CFGTOS	250	2x t_{out}	ns
I002	t_{MASh}	Clock Signal Hi Level Duration		25	t_{out}	ns
I003	t_{MASl}	Clock Signal Lo Level Duration		25	t_{out}	ns

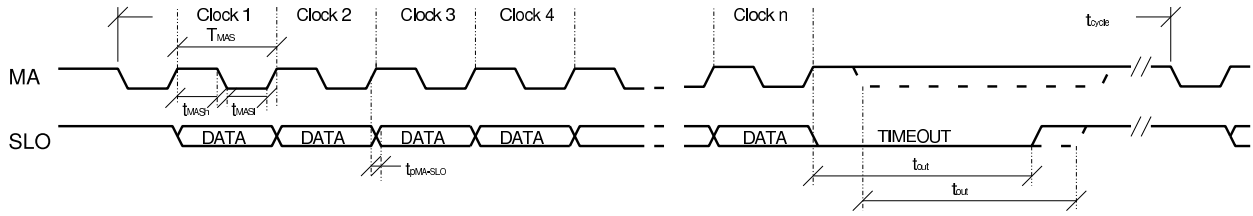


Figure 1: Serial Interface timing with SSI protocol

REGISTER MAP

OVERVIEW

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Hall Signal Conditioning								
0x00 *z*	GAING(1:0)		GAINF(5:0)					
0x01 *z*	ENAC	GCC(6:0)						
0x02 *z*	1*	VOSS(6:0)						
0x03 *z*	PRM	VOSC(6:0)						
0x04 *z*	HCLH	DPU	res.	CFGTOB	CIBM(3:0)*			
RS422 Driver								
0x05 *z*	ENSSI	CFGPROT	CFGO(1:0)		TRIHL(1:0)		CFGDR(1:0)	
Sine-to-Digital Converter								
0x06 *z*	CFGRES(7:0)							
0x07 *z*	CFGZPOS(7:0)							
0x08 *z*	CFGHYS(1:0)		CFGDIR	CFGMTD	CFGSU	CFGPOLE	CFGAB(1:0)	
0x09 *z*	CFGCOM(7:0)							
0x0A *z*	OEMA				CFGTRIG	CFGZ180	CFGENZ	CFGMTD2
0x0B *z*	OEMB							
0x0C *z*	OEMC							
0x0D	OEMRAM							
Test Settings								
0x0E *p*	TEST(7:0)							
0x0F *p*	ENHC	0	0	0	0	0	0	PROGZAP
ZAP Diodes (read only)								
0x10 .. 0x1F	ZAP diodes for addresses 0x00..0x0C and 0x7D..0x7F							
Not Used								
0x20 .. 0x41	'invalid addresses'							
Profile Identification (read only)								
0x42	Profile - 0x2C							
0x43	Profile - 0x0				DLEN(3:0)			
Not Used								
0x44 .. 0x75	'invalid addresses'							
Status Messages (read only; messages will be set back during reading)								
0x76	GAIN							
0x77	PROGERR	ERRSDATA	ERRAMIN	ERRAMAX	ERREXT	res.	res.	PROGOK

OVERVIEW								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BiSS Identification (0x78 bis 0x7B read-only)								
0x78	BiSS Device ID - 0x4D ('M')							
0x79	BiSS Device ID - 0x48 ('H')							
0x7A	BiSS Device ID Revision - 0x4C ('L')							
0x7B	BiSS Device ID Revision - 0x40 ('@')							
0x7C	-							CFGTOS
0x7D *z*	BiSS Device ID Manufacturer Revision - 0x00							
0x7E *z*	BiSS Device Manufacturer ID - 0x00							
0x7F *z*	BiSS Device Manufacturer ID - 0x00							

z: Register value programmable by zapping

*: Register value pre-programmed by iC-Haus

p: Register value write protected; can only be changed while V(VZAP)> Vt()hi

Table 5: Register layout

BASIC OPERATION

The iC-MHL100 uses an array of hall sensors to detect the local variation of the magnetic field emerging from a magnetic target. The target could be a magnetic tape with periodic varying polarity and a pitch (NS spacing) of 1 mm to match the iC-MHL100 sensor period P of 2 mm. An example for linear position sensing is shown in Figure 2.

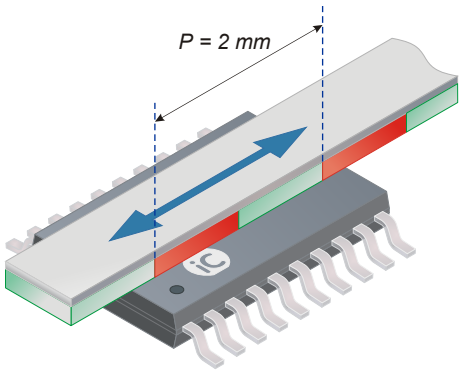


Figure 2: Typical arrangement of a magnetic tape to iC-MHL100

From the periodic magnetic field delivered by the target, the hall sensor array generates internal sensor signals which are then further processed and passed to the interpolator to generate incremental position data, as shown in Figure 3.

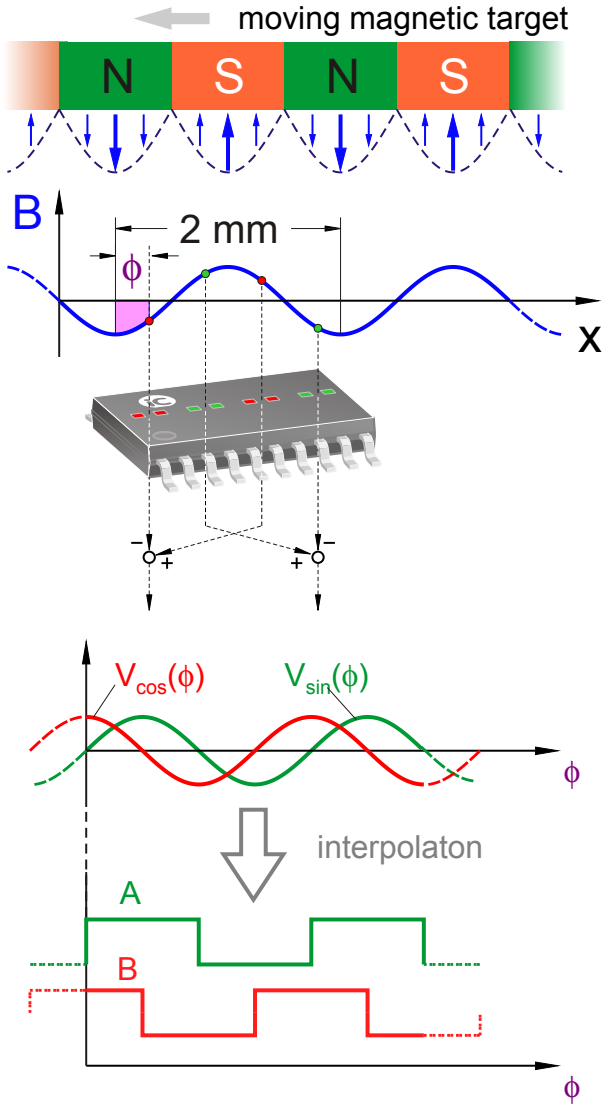


Figure 3: Signal generation and position data output

HALL SENSORS: Position and Analog Signals

The magnetic sensor array is placed in a line at the upper edge of the chip as shown in Figure 4. Each of the four sensor location (NCOS, PSIN, PCOS and NSIN) are equally spaced apart and are based on a pair of Hall sensors. Each Hall sensor pair provides a Hall output signal from the mean value of the two single sensors a pair consists of, thus representing the magnetic field strength at the center of each pair.

When a magnetic target is placed on top of the iC-MHL100 package, the resulting magnetic field generates corresponding Hall voltages. If a magnetic south pole is on top of a Hall sensor pair, the resulting Hall voltage is positive, whereas a magnetic north pole provides a negative one.

To provide accurate sensor signals, the magnetic target must consist of a periodic arrangement of north and south poles with a pitch (spacing NS) of 1 mm. The magnetic field distribution thus has a periodic variation of 2 mm, matching the Hall sensor array period exactly. Usually, a magnetic tape with magnetized north-south pattern is used together with the iC-MHL100.

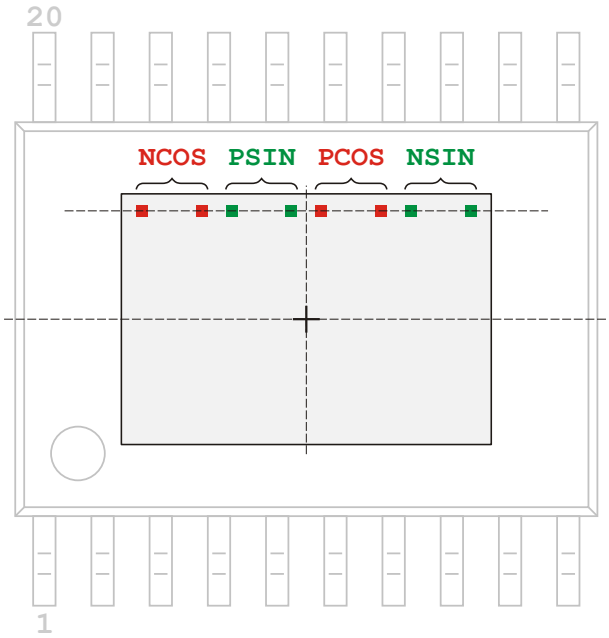


Figure 4: Position of the Hall sensors

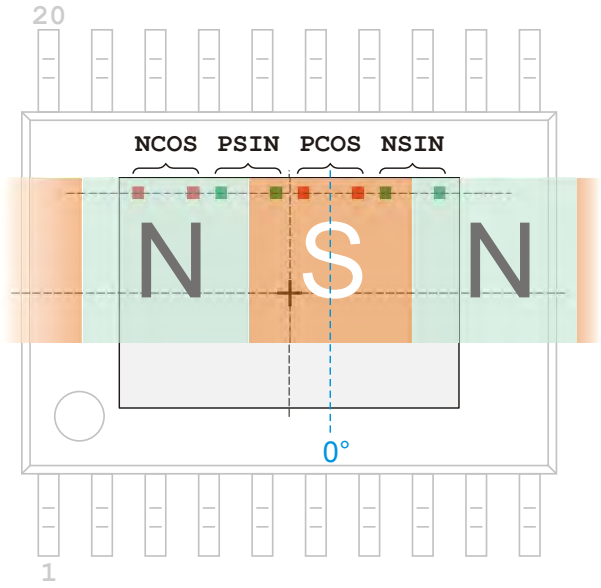


Figure 5: Zero angular position of the magnetic target. Center of south pole is aligned to the PCOS sensor pair

The field distribution can be approximately described as a sinusoidal variation of the magnetic field strength B along the target. As mentioned before, the iC-MHL100 provides analog sensor signals V_{SIN} and V_{COS} which represents the linear position of the tape with respect to the chip. The signals are internal but can be made externally available for test purposes (see the description of calibration procedure).

These signals are derived from the output signal difference of the complementary sensor pairs (PSIN/NSIN for the sine signal, PCOS/NCOS for the cosine signal) resulting in

$V_{SIN} = V_{PSIN} - V_{NSIN}$

and

$V_{COS} = V_{PCOS} - V_{NCOS}$.

Since the field distribution repeats periodically every 2 mm, an absolute position value can be defined only within a range of one magnetic period. Electrically, the sensor signals are repeating every 360 ° for every target movement of 2 mm.

By definition, the electrical zero position (within one period) is given by the corresponding angular zero value $\phi = 0$ where V_{sin} is zero and V_{cos} is at its maximum value. The mechanical zero-position location of the tape with respect to the iC-MHL100 is shown in Fig. 5.

The definition of a specific moving direction can be made by comparing the mechanical position with the corresponding electrical angular value. To obtain increasing angular position values, the magnetic tape has to be moved to the left (when looking on top of the chip/package) as shown in Fig. 6 where the tape has been shifted 0.5 mm to the left, as compared to Figure 5.

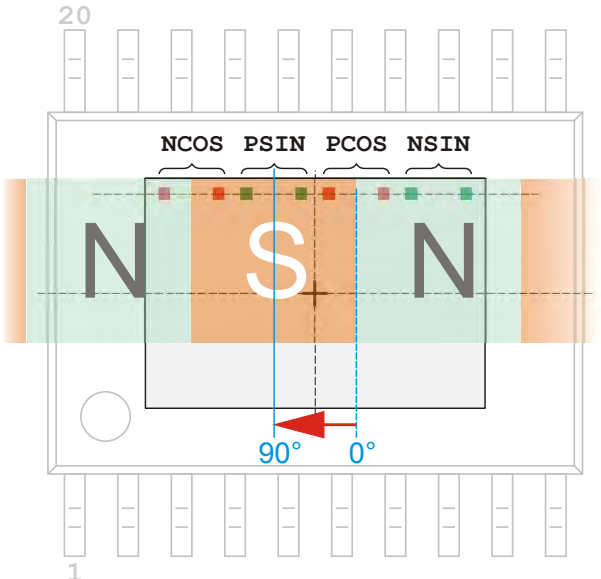


Figure 6: Position of the magnetic target at 90 ° electrical position. Center of south pole is aligned to the PSIN sensor pair

HALL SIGNAL CONDITIONING

The iC-MHL100 system has a signal calibration function that can compensate for the signal and adjustment errors. The Hall signals are amplified in two steps. First, the range of the field strength within which the Hall sensor is operated must be roughly selected. The first amplifier stage can be programmed in the following ranges:

GAING(1:0)	Addr. 0x00; bit 7:6
Value	Coarse Gain
0x00	5-fold
0x01	10-fold
0x02	15-fold
0x03	20-fold

Table 6: Range selection for Hall signal amplification

The operating range can be specified in advance in accordance with the temperature coefficient and the magnet distance. The integrated amplitude control can correct the signal amplitude between 1 and 20 via another amplification factor. Should the control reach the range limits, a different signal amplification must be selected via GAING.

GAINF(5:0)	Addr. 0x00; bit 5:0
Value	Fine Gain
0x00...0x02	1.098
0x03	1.150
...	$exp(\frac{ln(20)}{64} \cdot GAINF)$
0x3E...0x3F	18.213

Table 7: Hall signal amplification

The second amplifier stage can be varied in an additional range. With the amplitude control (ENAC = 0) deactivated, the amplification in the GAINF register is used. With the amplitude control (ENAC = 1) activated, the GAINF register bits have no effect.

GCC(6:0)	Addr. 0x01; bit 6:0
Value	Function
0x00	1.000
0x01	1.0015
...	$exp(\frac{ln(20)}{2048} \cdot GCC)$
0x3F	1.0965
0x40	0.9106
...	$exp(-\frac{ln(20)}{2048} \cdot (128 - GCC))$
0x7F	0.9985

Table 8: Amplification calibration cosine

The GCC register is used to correct the sensitivity of the sine channel in relation to the cosine channel. The cosine amplitude can be corrected within a range of approximately ±10 %.

ENAC	Addr. 0x01; bit 7
Value	Description
0x0	Amplitude control deactivated
0x1	Amplitude control active

Table 9: Activation of amplitude control

The integrated amplitude control can be activated with the ENAC bit. In this case the differential signal amplitude is adjusted to 4 Vss and the values of GAINF have no effect here.

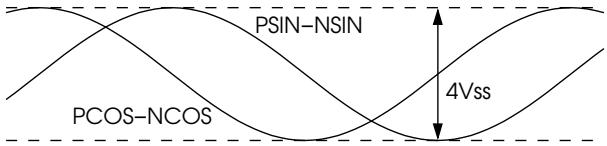


Figure 7: Definition of differential amplitude

After switch-on the amplification is increased until the setpoint amplitude is reached. The amplification is automatically corrected in case of a change in the input amplitude by increasing the distance between the magnet and the sensor, in case of a change in the supply voltage or a temperature change. The sine signals are therefore always converted into high-resolution quadrature signals at the optimum amplitude.

VOSS(6:0) Addr. 0x02; bit 6:0 **VOSC(6:0)** Addr. 0x03; bit 6:0	
Value	Offset correction
0x00	0 mV
0x01	1 mV
...	...
0x3F	63 mV
0x40	0 mV
0x41	-1 mV
...	...
0x7F	-63 mV

Table 10: Offset calibration for sine and cosine

Should there be an offset in the sine or cosine signal that, among other things, can also be caused by an inexactly adjusted magnet, then this offset can be corrected by the VOSS and VOSC registers. The output voltage can be shifted by ±63 mV in each case to compensate for the offset.

PRM	Addr. 0x03; bit 7
Value	Function
0x0	Energy-saving mode deactivated
0x1	Energy-saving mode activated

Table 11: Energy-saving mode

In the energy-saving mode the current consumption of the Hall sensors can be quartered. This also reduces the maximum rotating frequency by a factor of 4.

CIBM(3:0)	Addr. 0x04; bit 3:0
Value	Function
0x0	-40 %
...	...
0x8	0 %
0x9	+5 %
...	...
0xF	+35 %

Table 12: Calibration of bias current

In the test mode (TEST = 0x43) the internal bias current IBM can be measured on pin B vs pin VNA and changed via register CIBM to achieve a nominal value of 200 µA.

Note: CIBM is pre-programmed to the zapping ROM by iC-Haus and needs no further adjustment.

HCLH	Addr. 0x04; bit 7
Value	Frequency
0x0	250 kHz
0x1	500 kHz

Table 13: Activation of high Hall clock pulse

The switching-current hall sensors can be operated at two frequencies. At 500 kHz the sine has twice the number of support points. This setting is of interest at high magnetic input frequencies beyond 500 Hz (equivalent to 1 m/s comparable to Item 102).

TEST: Modes for Signal Calibration

For signal calibration iC-MHL100 has several test settings which make internal reference quantities and the amplified Hall voltages of the individual sensors accessible at external pins A, B, Z and U for measurement purposes. This enables the settings of the offset (VOSS, VOSC), gain (GAING, GAINF) and amplitude ratio of the cosine to the sine signal (GCC) to be directly observed on the oscilloscope.

Test mode can be triggered by connecting pin VZAP to VPD and programming the TEST register (address 0x0E). The individual test modes are listed in the following table:

Output signals in test mode					
Mode	TEST	Pin A	Pin B	Pin Z	Pin U
Normal	0x00	A	B	Z	U
Analog SIN	0x20	HPSP	HPSN	HNSP	HNSN
Analog COS	0x21	HPCP	HPCN	HNCP	HNCN
Analog OUT	0x22	PSIN	NSIN	PCOS	NCOS
Analog REF	0x43	VREF	IBM	VBG	VOSR
Digital CLK	0xC0	CLKD			

Table 14: Test modes and available output signals

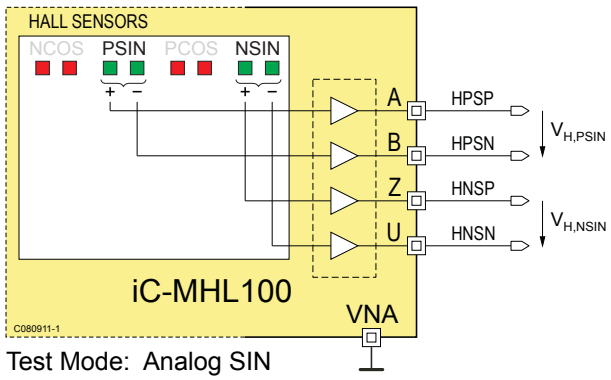
The output voltages are provided as differential signals with an average voltage of 2.5 V. The gain is determined by register values GAING and GAINF and should be set so that output amplitudes from the sine and cosine signals of about 1 V are visible.

Test Modes Analog SIN And Analog COS

In these test modes it is possible to measure the signals from the individual Hall sensors independent of one another. The name of the signal is derived from the sensor name and position. HPSP, for example, is the (amplified) Hall voltage of sensor PSIN at the positive signal path; similarly, HNCN is the Hall voltage of sensor NCOS at the negative signal path. The effective Hall voltage is accrued from the differential voltage between the positive and negative signal paths of the respective sensor.

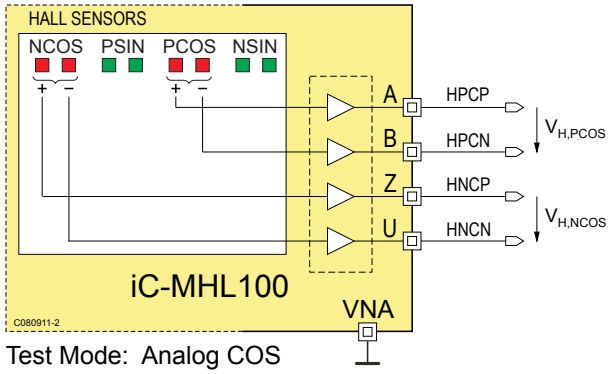
Test Mode Analog OUT

In this test mode the sensor signals are available at the outputs as they would be when present internally for further processing on the interpolator. The interpolation accuracy which can be obtained is determined by the quality of signals V_{sin} and V_{cos} and can be influenced in this particular test mode by the calibration of the offset, gain and amplitude ratio.



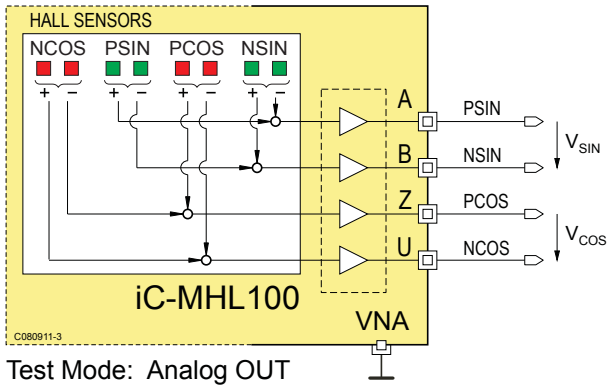
Test Mode: Analog SIN

Figure 8: Output signals of the sine Hall sensors in test mode Analog SIN



Test Mode: Analog COS

Figure 9: Output signals of the cosine Hall sensors in test mode Analog COS



Test Mode: Analog OUT

Figure 10: Differential sine and cosine signals in test mode Analog OUT

Test Mode Analog REF

In this mode various internal reference voltages are provided. VREF is equivalent to half the supply voltage (typically 2.5 V) and is used as a reference voltage for the Hall sensor signals. VBG is the internal bandgap reference (1.24 V), with VOSR (0.5 V) used to gener-

ate the range of the offset settings. Bias current IBM determines the internal current setting of the analog circuitry. In order to compensate for variations in this current and thus discrepancies in the characteristics of the individual iC-MHL100 devices (due to fluctuations in production, for example), this can be set within a range of -40% to +35% using register parameter CIBM. The nominal value of 200 µA is measured as a short-circuit current at pin B to ground.

Note: A CIBM preset value is programmed to the zapping ROM during chip test by iC-Haus and therefore no further customer programming is required.

Test Mode Digital CLK
If, due to external circuitry, it is not possible to measure IBM directly, by way of an alternative clock signal CLKD at pin A can be calibrated to a nominal 1 MHz in this test mode via register value CIBM.

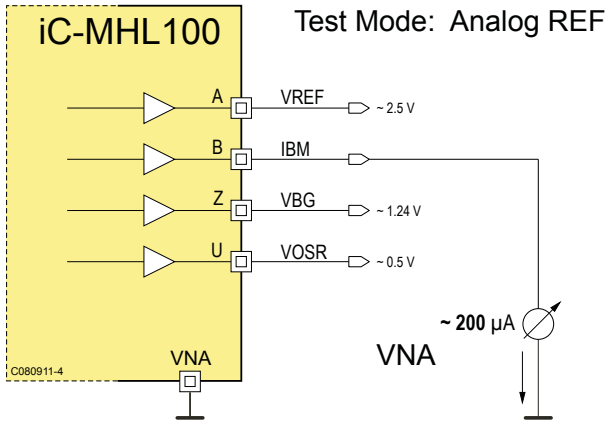


Figure 11: Setting bias current IBM in test mode Analog REF

CALIBRATION PROCEDURE

The calibration procedure described in the following applies to the optional setting of the internal analog sine and cosine signals and the mechanical adjustment of the magnet and iC-MHL100 in relation to one another.

BIAS Setting
The internal bias setting via register CIBM compensates for device process tolerances and an optimum setting value is **already pre-programmed** into the zapping ROM by iC-Haus during automatic chip test. Therefore, no further customer adjustments are needed for this setting. However, temporary changing the CIBM RAM content to extreme values can be used to imitate variations in device characteristic or to simulate changes in physical parameter like temperature or supply voltage (see chapter OTP Programming).

Mechanical Adjustment
iC-MHL100 can be adjusted in relation to the magnet in test modes Analog SIN and Analog COS, in which the Hall signals of the individual Hall sensors can be observed while the magnet rotates.

In test mode Analog SIN the output signals of the sine Hall sensors which are diagonally opposite one another are visible at pins A, B, Z and U. iC-MHL100 and the magnet are then adjusted in such a way that differential signals V_{PSIN} and V_{NSIN} have the same amplitude and a phase shift of 180 °. The same applies to test mode Analog COS, where differential signals V_{PCOS} and V_{NCOS} are calibrated in the same manner.

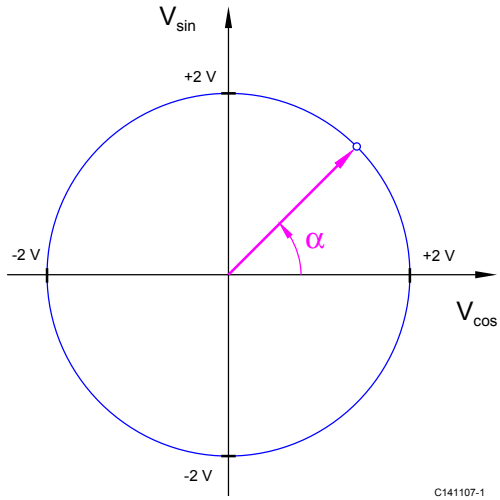


Figure 12: Ideal Lissajous curve

Calibration Using Analog Signals
In test mode Analog OUT as shown in Figure 10 the internal signals which are transmitted to the sine-to-digital converter can be tapped with high impedance. With a rotating magnet it is then possible to portray the differential signals V_{SIN} and V_{COS} as an x-y graph (Lissajous curve) with the help of an oscilloscope. In an ideal setup the sine and cosine analog values describe a perfect circle as a Lissajous curve, as illustrated by Figure 12.

At room temperature and with the amplitude control switched off (ENAC = 0) a rough GAING setting is selected so that at an average fine gain of GAINF = 0x20 (a gain factor of approx. 4.5) the Hall signal amplitudes

are as close to 2 V as possible. The amplitude can then be set more accurately by varying GAINF. Variations in the gain factor, as shown in Figure 13, have no effect on the Lissajous curve, enabling the angle information for the interpolator to be maintained.

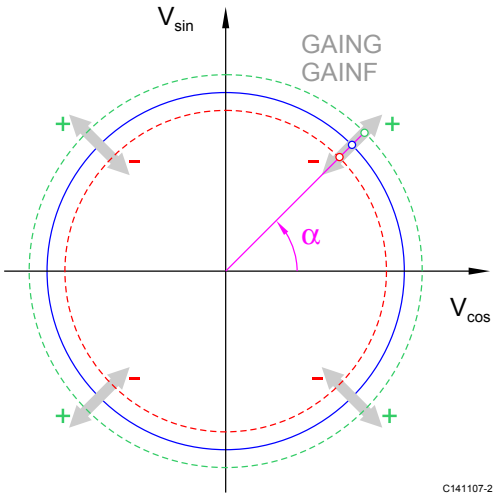


Figure 13: Effect of gain settings GAING and GAINF

Deviations of the observed Lissajous curve from the ideal circle can be corrected by varying the amplitude offset (register VOSS, VOSC) and amplitude ratio (register GCC). Changes in these parameters are described in the following Figures 14 to 16. Each of these settings has a different effect on the interpolated angle value. A change in the sine offset thus has a maximum effect on the angle value at 0 ° and 180 °, with no alterations whatsoever taking place at angles of 90 ° and 270 °. When varying the cosine offset exactly the opposite can be achieved as these angle pairs can be set independent of one another. Setting the cosine/sine amplitude ratio does not change these angles (0 °, 90 °, 180 ° and 270 °); however, in-between values of 45 °, 135 °, 225 ° and 315 ° can still be influenced by this parameter.

Once calibration has been carried out a signal such as the one illustrated in Figure 12 should be available.

In the final stage of the process the amplitude control can be switched back on (ENAC = 1) to enable deviations in the signal amplitude caused by variations in the magnetic field due to changes in distance and temperature to be automatically controlled.

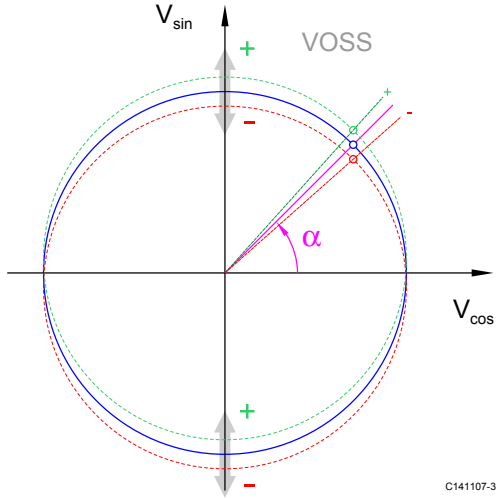


Figure 14: Effect of the sine offset setting

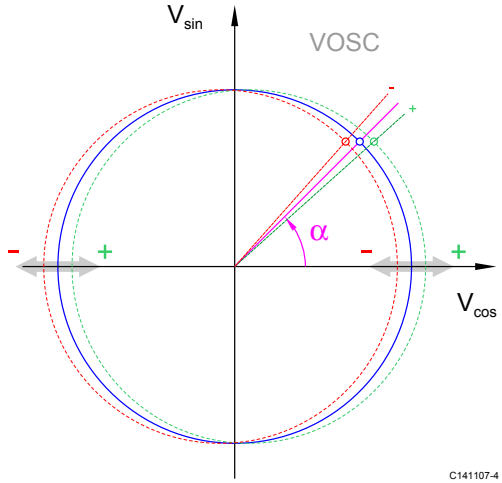


Figure 15: Effect of the cosine offset setting

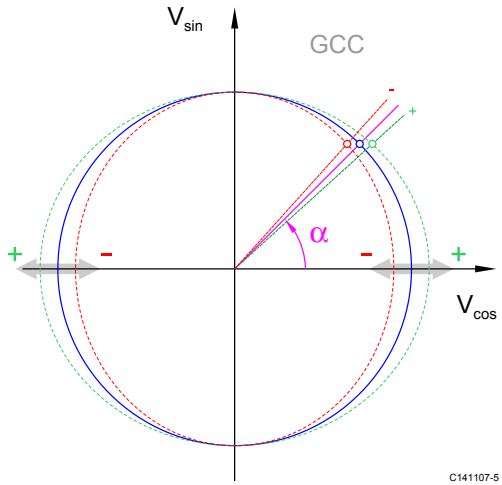


Figure 16: Effect of the amplitude ratio

Calibration Using Incremental Signals

If test mode cannot be used, signals can also be calibrated using the incremental signals or the values read out serially. In order to achieve a clear relationship between the calibration parameters which have an effect on the analog sensor signals and the digital sensor values derived from these, the position of the zero pulse should be set to ZPOS = 0 so that the digital signal starting point matches that of the analog signals.

At an incremental resolution of 8 edges per revolution (CFGRES = 0x1) those angle values can be displayed at which calibration parameters VOSS, VOSC and GCC demonstrate their greatest effect. When rotating the magnet at a constant angular speed the incremental signals shown in Figure 17 are achieved, with which the individual edges ideally succeed one another at a temporal distance of an eighth of a cycle (a 45 ° angle distance). Alternatively, the angle position of the magnet can also be determined using a reference encoder, rendering an even rotational action unnecessary and allowing calibration to be performed using the available set angle values .

The various possible effects of parameters VOSS, VOSC and GCC on the flank position of incremental signals A and B are shown in Figure 17. Ideally, the distance of the rising edge (equivalent to angle positions of 0 ° and 180 °) at signal A should be exactly half a period (PER). Should the edges deviate from this in distance, the offset of the sine channel can be adjusted using VOSS. The same applies to the falling edges of the A signal which should also have a distance of half a period; deviations can be calibrated using the offset of cosine parameter VOSC. With parameter GCC the distance between the neighboring flanks of signals A and B can then be adjusted to the exact value of an eighth of a cycle (a 45 ° angle distance).

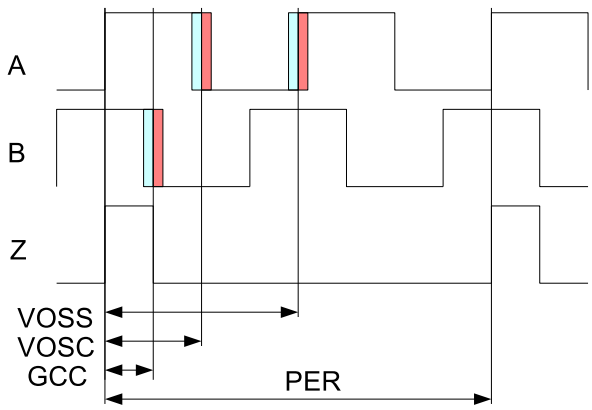


Figure 17: Calibration using incremental signals

SINE-TO-DIGITAL CONVERTER

The iC-MHL100 device integrates two separate sine-to-digital converters. A high-resolution 12-bit converter for the ABZ incremental signals can be programmed in broad ranges of the resolution and generate quadrature signals even at the highest speed and resolution.

The converter operates for the commutation signals UVW independently of this and can be set in the zero point separately from the quadrature converter. This enables the commutation at other angles based on the index track Z.

Incremental signals

CFGRES(7:0) Addr. 0x06; bit 7:0		
Value	Interpolation factor	Resolution
0x00	1	4
0x01	2	8
...	...	...
0x7e	127	508
0x7f	128	512
0x80	256	1024
0x81	512	2048
0x82	1 024	4096

Table 15: Programming interpolation factor

The resolution of the 12-bit converter can virtually be set as desired. Any resolution can be set up to an interpolation factor of 128, i.e. 512 edges per rotation. At higher resolutions, only the binary resolutions can be set, i.e. 256, 512 and 1 024. In the highest resolution with an interpolation factor of 1 024, 4 096 edges per rotation are generated and 4 096 angular steps can be differentiated. Even in the highest resolution, the absolute position can be calculated in real time at the maximum speed. After the resolution is changed, a module reset is triggered internally and the absolute position is recalculated.

CFGAB(1:0) Addr. 0x08; bit 1:0	
Value	Function
0x0	A and B not inverted
0x1	B inverted, A normal
0x2	A inverted, B normal
0x3	A and B inverted

Table 16: Inversion of AB signals

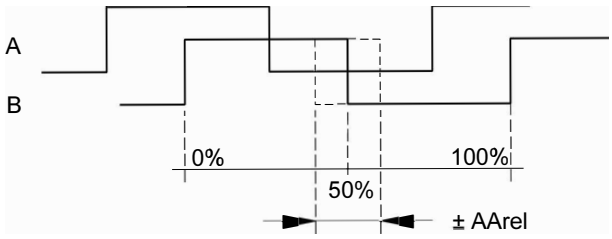


Figure 18: ABZ signals and relative accuracy

The incremental signals can be inverted again independently of the output drivers. As a result, other phase angles of A and B relative to the index pulse Z can be generated. The standard is A and B high level for the zero point, i.e. Z is equal to high.

Figure 18 shows the position of the incremental signals around the zero point. The relative accuracy of the edges to each other at a resolution setting of 10 bit is better than 10 %. This means that, based on a period at A or B, the edge occurs in a window between 40 % and 60 %.

CFGHYS(1:0) Addr. 0x08; bit 7:6	
Value	Hysteresis
0x0	0.17 °
0x1	0.35 °
0x2	0.7 °
0x3	1.4 °

Table 17: Programming angular hysteresis

With rotating direction reversal, an angular hysteresis prevents multiple switching of the incremental signals at the reversing point. The angular hysteresis corresponds to a slip which exists between the two rotating directions. However, if a switching point is approached from the same direction, then the edge is always generated at the same position on the output. The following Figure shows the generated quadrature signals for a resolution of 360 edges per rotation (interpolation factor 90) and a set angular hysteresis of 1.4 °.

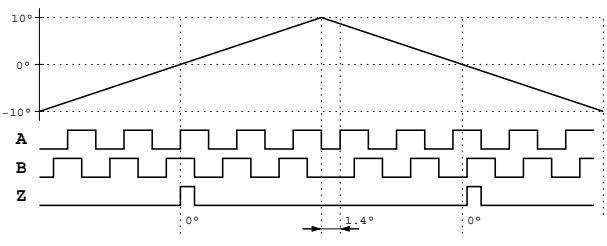


Figure 19: Quadrature signals for rotating direction reversal (hysteresis 1.4 °)

At the reversal point at +10 °, first the corresponding edge is generated at A. As soon as an angle of 1.4 ° has been exceeded in the other direction in accordance with the hysteresis, the return edge is generated at A again first. This means that all edges are shifted by the same value in the rotating direction.

CFGZPOS(7:0) Addr. 0x07; bit 7:0	
Value	Function
0x0	0 °
0x1	1.4 °
0x2	2.8 °
...	$\frac{360}{256}$·CFGZPOS
0xff	358.6 °

Table 18: Programming AB zero position

The position of the index pulse Z can be set in 1.4 ° steps. An 8-bit register is provided for this purpose, which can shift the Z-pulse once over 360 °.

CFGMTD Addr. 0x08; bit 4 **CFGMTD2** Addr. 0x0A; bit 0			
CFGMTD2	CFGMTD	Minimum edge spacing	
0	0	500 ns	max. 500 kHz at A
0	1	125 ns	max. 2 MHz at A
1	0	8 µs	max. 31.25 kHz at A
1	1	2 µs	max. 125 kHz at A

Table 19: Minimum edge spacing

The CFGMTD register defines the time in which two consecutive position events can be output. The default is a maximum output frequency of 500 kHz on A. This means that at the highest resolution, high magnetic input frequencies beyond 500 Hz (equivalent to 2 m/s comparable to Item 102) can be correctly shown. In the setting with an edge spacing of 125 ns, the edges can be generated even at the highest revolution and the maximum speed. However, the counter connected to the module must be able to correctly process all edges in this case. The settings with 2 µs, and 8 µs can be used for slower counters. It should be noted then, however, that at higher resolutions the maximum rotation speed is reduced.

CFGDIR Addr. 0x08; bit 5	
Value	Function
0x0	Rotating direction CCW
0x1	Rotating direction CW

Table 20: Rotating direction reversal

The rotating direction can easily be changed with the bit CFGDIR. When the setting is CCW (counter-clockwise, CFGDIR = 0) the resulting angular position values will increase when movement of the magnetic tape is performed as shown in Figure 3. To obtain increasing angular position values in the CW (clockwise) direction, CFGDIR then has to be set to 1.

The internal analog sine and cosine signal which are available in test mode are not affected by the setting of CFGDIR. They will always appear as shown in Figure 3.

CFGSU Addr. 0x08; bit 3	
Value	Function
0x0	ABZ output "111" during startup
0x1	AB instantly counting to actual position

Table 21: Configuration of output startup

Depending on the application, a counter cannot bear generated pulses while the module is being switched on. When the supply voltage is being connected, first the current position is determined. During this phase, the quadrature outputs are constantly set to "111" in the setting CFGSU = 0. In the setting CFGSU = 1, edges are generated at the output until the absolute position is reached. This enables a detection of the absolute position with the incremental interface.

Commutation signals

The converter for the generation of the commutation signals can be configured for two and four-pole motors. Three rectangular signals each with a phase shift of 120 ° are generated. With two-pole commutation, the sequence repeats once per rotation. With a four-pole setting, the commutation sequence is generated twice per rotation.

CFGPOLE Addr. 0x8; bit 2	
Value	Function
0x0	2 pole commutation (1 pole pair per mag. period)
0x1	4 pole commutation (2 pole pairs per mag. period)
Note	Magnetic period = 4 mm.

Table 22: Commutation

The zero position of the commutation, i.e. the rising edge of the track U, can be set as desired over a rotation. Here 192 possible positions are available. Values above 0xC0 are the mirrored positions from 0x70.

CFGCOM(7:0) Addr. 0x09; bit 7:0	
Value	Function
0x00	0 °
0x01	1.875 °
...	$\frac{360°}{192}$ · CFGCOM
0xBF	358.125 °

Table 23: Commutation Position

CFGENZ controls the pin ENZ. For CFGENZ = 0x00 the z-signal is enabled by ENZ = high. Otherwise, for CFGENZ = 0x01 the z-signal is enabled by ENZ = low.

CFGZ180 zero signal width can be changed between 90 ° (default, CFGZ180 = 0x00) and 180 ° (CFGZ180 = 0x01).

GAIN OUTPUT MONITOR

The pin GAIN serves as a monitor signal to indicate the current gain setting of the amplitude control loop. The output voltage at the GAIN pin increases linearly from VNA up to VPA level with increasing value of the internal GAIN register (refer to Item No. Q03 and Q04).

With CFGTRIG = 1 the GAIN output is disabled and set to tristate.

CFGTRIG Addr. 0x0A; bit 3	
Value	Function
0x0	GAIN output active
0x1	GAIN output deactivated (tristate)

Table 24: Setting GAIN output to tristate

OUTPUT DRIVERS

Six RS422-compatible output drivers are available, which can be configured for the incremental signals and commutation signals. The following table on the CFGO register bits provides an overview of the possible settings.

CFGO(1:0)	Addr. 0x05; bit 5:4
Value	Output
0x00	Differential incremental ABZ (U=NA, V=NB, W=NZ)
0x01	Incremental ABZ + commutation UVW
0x10	Differential commutation UVW (A=NU, B=NV, Z=NW)
0x11	Incremental ABZ + AB4 (U=A4, V=B4, W=0)

Table 25: Configuration of output drivers

In the differential incremental mode (CFGO = 00, Figure 20), quadrature signals are available on the pins A, B and Z. The respective inverted quadrature signals are available on the pins U, V and W. As a result, lines can be connected directly to the module. Another configuration of the incremental signals is specified in the section "Sine-to-Digital Converter".

With CFGO = 01 (Figure 21) the ABZ incremental signals and the UVW commutation signals are available on the six pins. As long as the current angular position is not yet available during the start-up phase, all commutation signals are at the low level.

With CFGO = 10, the third mode (Figure 22) is available for transferring the commutation signals via a differential line. The non-inverted signals are on the pins U, V and W, the inverted signals on A, B and Z.

The ABZ quadrature signals with an adjustable higher resolution and quadrature signals with one period per rotation are available in the fourth mode (Figure 23). Four segments can be differentiated with the pins U and V. This information can be used for an external period counter which counts the number of scanned complete rotations.

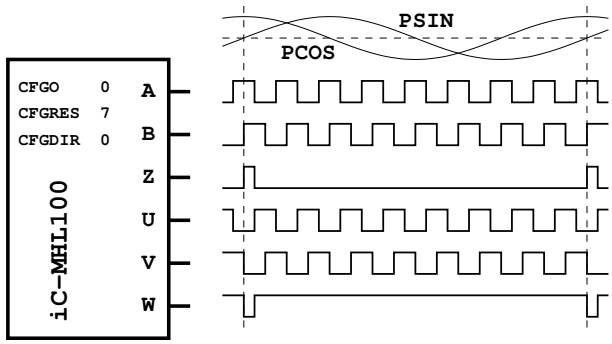


Figure 20: ABZ differential incremental signals

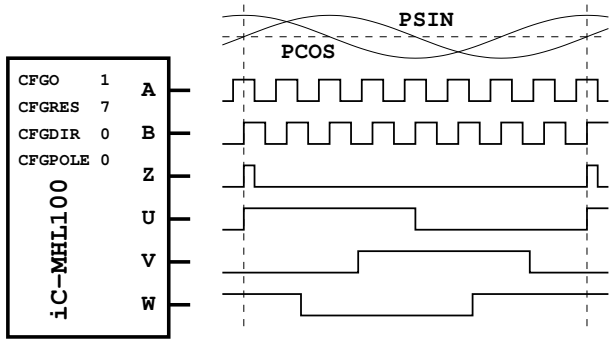


Figure 21: ABZ incremental / UVW commutation signals

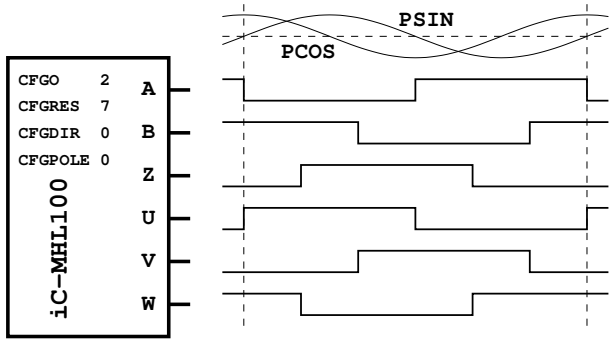


Figure 22: UVW differential commutation signals

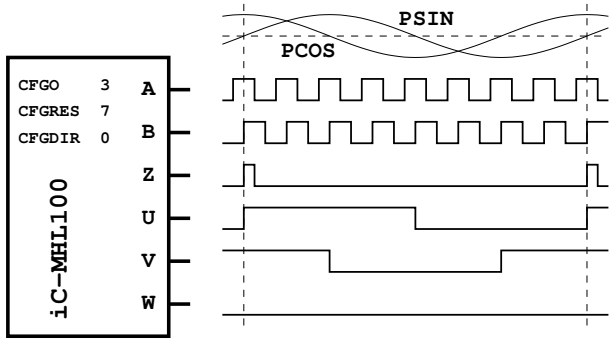


Figure 23: ABZ incremental signals / period counter

The property of the RS422 driver of the connected line can be adjusted in the CFGDR register.

CFGDR(1:0) Addr. 0x05; bit 1:0	
Value	Function
0x00	10 MHz, 4 mA (default)
0x01	10 MHz, 60 mA
0x10	300 kHz, 60 mA
0x11	3 MHz, 20 mA

Table 26: Driver property

Signals with the highest frequency can be transmitted in the setting CFGDR = 00. The driver capability is at least 4 mA, however it is not designed for a 100 Ω line. This mode is ideal for connection to a digital input on the same assembly. With the setting CFGDR = 01 the same transmission speed is available and the driver power is sufficient for the connection of a line over a short distance. Steep edges on the output enable a high transmission rate. A lower slew rate is offered by the setting CFGDR = 10, which is excellent for longer lines in an electromagnetically sensitive environment. Use of the setting CFGDR = 11 is advisable at medium transmission rates with a limited driver capability.

TRIHL Addr. 0x05; bit 3:2	
Value	Function
0x00	Push pull output stage
0x01	Low-side driver
0x10	High-side driver
0x11	Tristate

Table 27: Tristate Register

The drivers consist of a push-pull stage in each case with low-side and high-side drivers which can each be activated individually. As a result, open-drain outputs with an external pull-up resistor can also be realized.

BiSS INTERFACE

The BiSS interface with the BiSS C protocol is used to read out the absolute position and to parameterize the module. For a detailed description of the BiSS protocol, see separate BiSS C protocol specification.

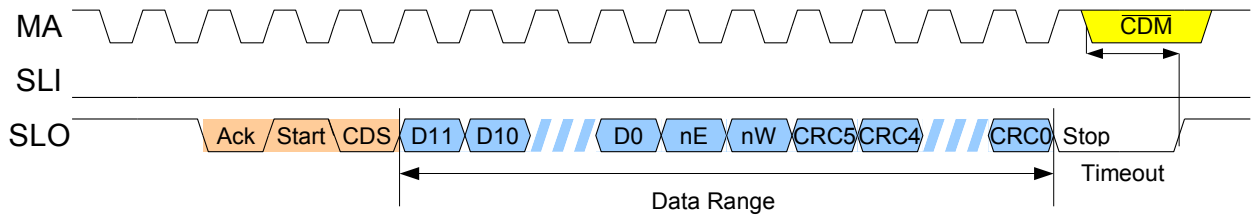


Figure 24: BiSS C Interface Protocol

The sensor sends a fixed cycle-start sequence containing the acknowledge-, start and control-bit followed by the binary 12 bit sensor data. At lower resolution settings the data word contains leading zeros. The low-active error bit nE a 0 indicates an error which can be further identified by reading the status register 0x77. The following bit nW is always at 1 state. Following the 6 CRC bits the data of the next sensors, if available, are presented. Otherwise, the BiSS master stops generating clock pulse on the MA line an the sensor runs into a timeout, indicating the end of communication.

Serial Protocol Content	**BiSS C**
Cycle start sequence	Ack/Start/CDS
Length of sensor data	12 bit + ERR + WARN
CRC polynomial	0b1000011
CRC mode	inverted
max. data rate	10 MHz

Table 28: BiSS C Protocol

ENSSI Addr. 0x05; bit 7	
Value	Interface
0x0	BiSS C protocol
0x1	SSI-Mode

Table 29: Activation of SSI mode

In the SSI mode the absolute position is output with 13 bits according to the SSI standard. However, in the SSI mode it is not possible to vary the parameter set. The data is transmitted as reduced Gray code, e.g. after converting into binary code, the data range is symmetrical to the center of the number string. For example, with a set resolution of 360 data values between 76 and 435 are transmitted.

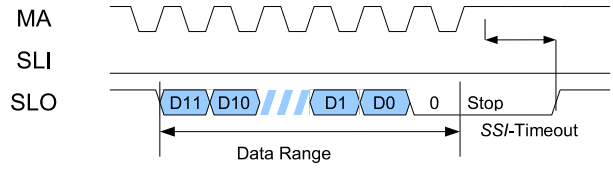


Figure 25: SSI protocol, data GRAY-coded

The register range 0x00 to 0x0F is equivalent to the settings with which the IC can be parameterized. The settings directly affect the corresponding switching parts. It is important to note that test register 0x0E can only be written to when pin VZAP is connected to VPD. When VPD > 6 V, write access to the test register is ignored. Register 0x0F can be configured at potentials V(VZAP) > Vt(VZAP)hi.

The range 0x10 to 0x1F is read-only and reflects the contents of the integrated zapping diodes. Following programming the data can be verified via these addresses. After the supply voltage is connected, the contents of the zapping diodes are copied to the RAM area 0x00 to 0x0F. Then the settings can be overwritten via the BiSS interface. Overwriting is not possible if the CFGPROT bit is set.

Errors in the module are signaled via the error message output NERR. This open-drain output signals an error if the output is pulled against VND. If the error condition no longer exists, then the pin is released again after a waiting time of approximately 1 ms. If the integrated pull-up resistor is deactivated with DPU = 1, then an external resistor must be provided. With DPU = 0 it brings the pin up to the high level again.

DPU	Addr. 0x04; bit 6
Value	Function
0x0	Pull-up activated
0x1	Pull-up deactivated

Table 30: Activation of NERR pull-up

With the BiSS profile ID, the data format of the sensor can be requested. Reading the BiSS profile ID results 0x2C in address 0x43, which identifies BiSS Profile BP1 and two most significant bits of the multiturn resolution, what is here always 00. Reading the register 0x43 contains the three least significant bits of the multiturn resolution, what is here always 000 and five bits of the singleturn resolution as is the data length DLEN of the transmitted sensor data in accordance with the set resolution. The sensor data is transmitted right-justified and filled with preceding zeros on smaller resolutions than 12 bit. The following table shows the data length according to the resolution.

DLEN	Addr. 0x43; bit 3:0
Value	Length
0	n/a
1	n/a
2	CFGRES = 00000000, 4
3	CFGRES = 00000001, 8
4	CFGRES = 0000001x, 12 to 16
5	CFGRES = 000001xx, 20 to 32
6	CFGRES = 00001xxx, 36 to 64
7	CFGRES = 0001xxxx, 68 to 128
8	CFGRES = 001xxxxx, 132 to 256
9	CFGRES = 01xxxxxx, 260 to 512
10	CFGRES = 10000000, 1 024
11	CFGRES = 10000001, 2 048
12	CFGRES = 10000010, 4 096

Table 31: Data length

Note: With CFGRES = 10000010, 4 096 and using BiSS protocol the device provides a BiSS Profile ID 0x2C 0x0C (0x2C in address 0x42 and 0x0C in address 0x43) that is "BiSS Profile BP1 Standard Rotary Encoder" conform.

The status register provides information on the status of the module. There are 5 different errors that can be signaled. Following unsuccessful programming of the zapping diodes, the bit PROGERR is set. If an attempt is made to read the current position via the BiSS interface during the start-up phase, an error is signaled with ERRSDATA, as the actual position is not yet known. The ERRAMAX bit is output to signal that the amplitude is too high, while the ERRAMIN bit signals an amplitude which is too low, caused, for example, by too great a distance to the magnet. If the NERR pin is pulled against VND outside the module, this error is also signaled via the BiSS interface. The ERREXT bit is then equal to 1. The error bits are reset again after the status register is read out at the address 0x77. The error bit in the data word is then also read in the next cycle as 0.

CFGTOB Addr. 0x04; bit 4 **CFGTOS** Addr. 0x7C; bit 0		
CFGTOS	**CFGTOB**	**Timeout**
0	0	16 µs
1	0	2 µs
x	1	2 µs

Table 32: BiSS timeout for sensor data

The BiSS timeout can be programmed to a shorter value with the CFGTOS bit. However, this setting is reset to the default value 16 µs again following a reset. The BiSS timeout can be permanently programmed for faster data transmission with the CFGTOB register via a zapping diode. Resetting to slower data transmission is then not possible.

The registers 0x78 to 0x7F are reserved for the BiSS Identifier. The BiSS Identifier identifies the device manufacturer and the type of BiSS module. The registers 0x7D to 0x7F are alterable and programmable to provide a manufacturer individual BiSS Device Manufacturer ID and revision.

OEM DATA

Parameters OEMA, OEMB and OEMC can be used and zapped as user specific data. OEMRAM can not be zapped.

Parameter	Address	Zapping possible
OEMA	0x0A; bit 7:4	yes
OEMB	0x0B; bit 7:0	yes
OEMC	0x0C; bit 7:0	yes
OEMRAM	0x0D; bit 7:0	no

Table 33: Overview of OEM Data

OTP PROGRAMMING

Once the RAM parameters have been configured these settings can be written to the underlying zapping ROM.

ENHC	Addr. 0x0F; bit 7
0	Default setting
1	ZAP diode testing: Use a higher current for reading the ZAP diodes memory (0x10. . . 0x1F)

Table 34: Enable High Current

As a requirement for programming, a zapping voltage (nominal 7 V, see item 806 in the electrical characteristics for tolerances) has to be provided via pins VZAP and VNA. Also, the device is not in the test mode, e.g. the test register has to be set to TEST = 0x00. CIBM has to be set to 0x00 temporarily.

The internal programming algorithm for the ZAP diodes is started by setting the bit PROGZAP. When the programming routine terminates, the PROGZAP bit resets automatically. Successful programming is then indicated by the status register (address 0x77) when bit PROGOK is set and PROGERR is unset - otherwise, an error situation has occurred (for example a missing zapping voltage).

PROGOK **PROGERR**	Addr. 0x77; bit 0 Addr. 0x77; bit 7	
PROGOK	**PROGERR**	**Corrective actions**
0	0	Set VZAP to 7 V
0	1	Set VZAP to 7 V and TEST = 0x00
1	0	Zapping was successful
1	1	Undefined state

Table 35: Zapping results

The ZAP memory can be tested by reading the register range 0x10. . . 0x1F. This test has to be done with a higher readout current (bit ENHC = 1) to simulate worst case operating conditions.

Note:
An alternative, more difficult procedure requires verification of the zapping ROM content while varying the supply voltages VPD and VPA to extreme limits of 4.0 and 5.5 V. As variation of supply voltages in a custom design might not be possible, (e.g. due to the use of fixed voltage regulators), this verification procedure will not be applicable then and is not discussed here any further. The reader may refer to earlier iC-MHL200 datasheets (B1 and earlier).

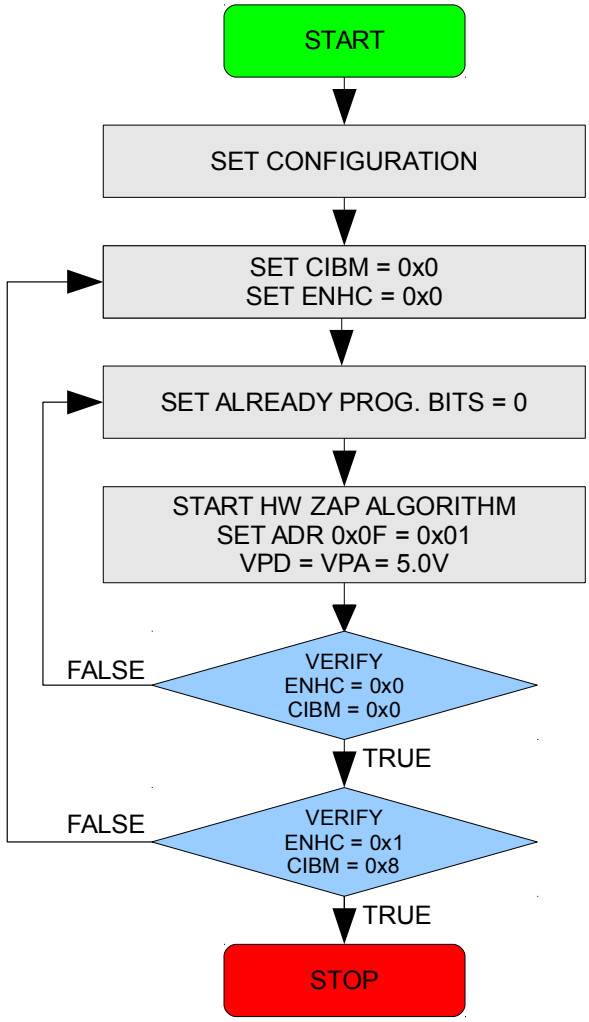


Figure 26: Programming algorithm

Figure 26 shows how the iC-MHL100 Evaluation Software performs the settings of the parameters for zapping ROM verification. First a device configuration is set to the RAM. With the parameters CIBM and ENHC both set to 0x00, the programming algorithm is started by setting 0x01 to address 0x0F. In case the verification of the ROM at two extreme conditions (ENHC = 0x00, CIBM = 0x00 and ENHC = 0x01, CIBM = 0x08) is successful, the verification is completed. Otherwise, in case some ROM bits are not identified as programmed, the zapping procedure has to be repeated. As already zapped ROM bits shall not be programmed again, the corresponding RAM bits have to be set to zero before repeating the next zapping procedure.

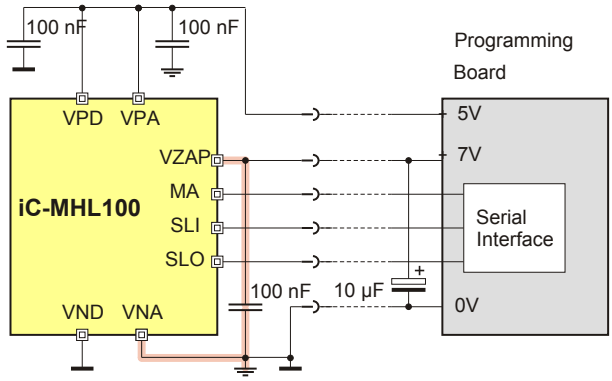


Figure 27: Recommended setup for external programming. A short low impedance path (shown in light red) must be provided directly from pin VZAP to pin VNA

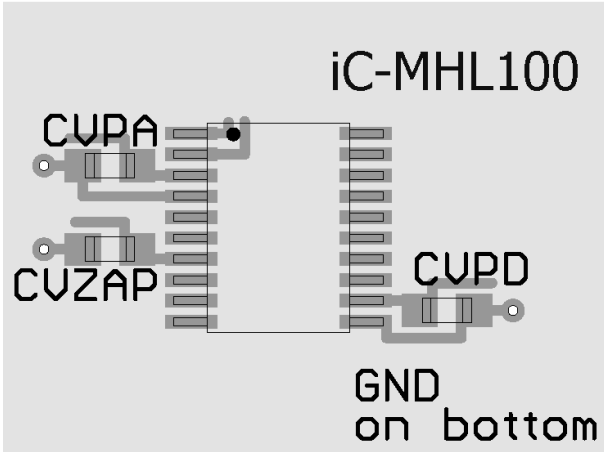


Figure 28: Example PCB layout showing low impedance connection of capacitors to supply voltages (VPA, VPD, VZAP) and common ground

For reliable ROM writing, a low impedance connection path as shown in Figure 27 must be established for the VZAP blocking capacitor (about 100 nF) between pin VZAP and pin VNA to ensure stable VZAP voltage during programming. A further capacitor of 10 µF which may be located externally (e.g. on the programming board) is recommended for additional blocking purpose.

A typical PCB layout may look like the one shown in Figure 28.

The ROM content may be protected against further changes by register CFGPROT.

CFGPROT	Addr. 0x05; bit 6
Value	Protection
0	no protection
1	write/read protection
Note	The VZAP voltage must not be applied.

Table 36: Write/read protection of configuration

With CFGPROT = 0, the registers at the addresses 0x00 to 0x0F and 0x78 to 0x7F are readable and writeable. The addresses 0x10 to 0x1F and 0x77 are read-only. With CFGPROT = 1, the address 0x7C is writeable. The addresses 0x42, 0x43 and 0x76 to 0x7F are readable, while all others are read-protected.

REVISION HISTORY

Rel.	Rel. Date[1]	Chapter	Modification	Page
A1	2019-01-28	All	First Release (Preliminary)	

[1] Release Date format: *YYYY-MM-DD*

ORDERING INFORMATION

Type	Package	Order Designation
iC-MHL100	TSSOP20	iC-MHL100 TSSOP20
iC-MHL100	QFN32-5x5	iC-MHL100 QFN32-5x5

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