

# iC-HTP

## DUAL CW P-TYPE LASER DIODE DRIVER



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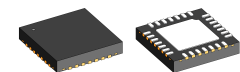
### FEATURES

- ◆ Dual channel CW and pulsed operation up to 300 kHz
- ◆ Up to 1500 mA with both channels (750 mA each) combined
- ◆ 2.8 to 11 V power supply
- ◆ Operation with or without  $\mu$ Controller
- ◆ Individual enable input per channel
- ◆ Individual laser power supply per channel
- ◆ Control loop accuracy better than 1%
- ◆ Internal programmable logarithmic monitor resistor
- ◆ Operating point setup with 10 bit logarithmic resolution
- ◆ ACC or APC mode individually configurable for each channel
- ◆ A/D converters for analog monitoring
- ◆ SPI or I<sup>2</sup>C programming interface
- ◆ Configuration content verification and validation
- ◆ Programmable laser overcurrent protection
- ◆ Optimized for P- and M-type laser diodes
- ◆ Low drop linear regulator for 3.3 V
- ◆ Low current standby mode
- ◆ Temperature monitor
- ◆ Temperature range -40 to 85 °C

### APPLICATIONS

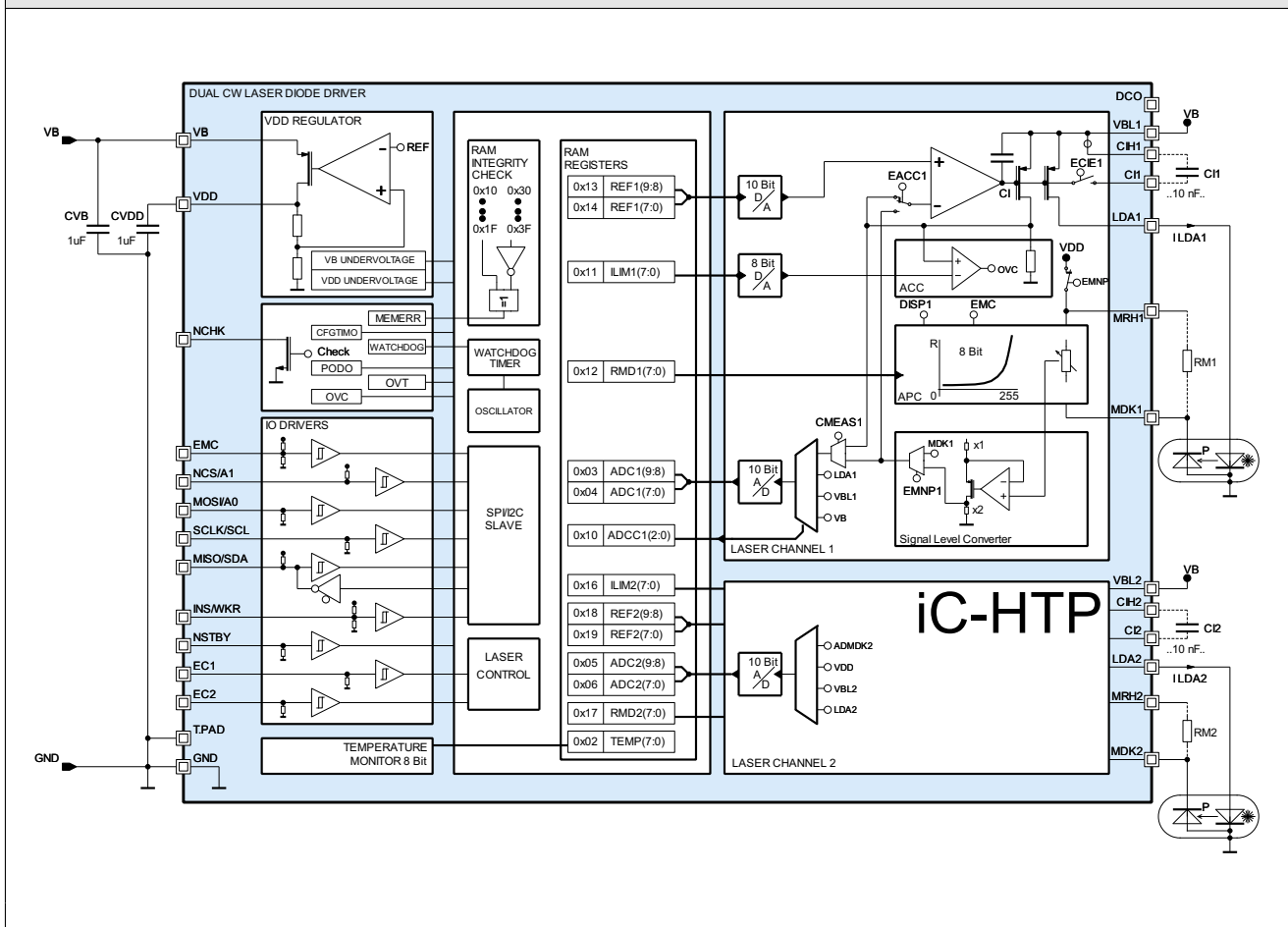
- ◆ Laser diode and LED modules
- ◆ CW P- and M-type laser diode drivers
- ◆ Embedded laser diode controllers
- ◆ Structured-light 3D illuminations
- ◆ Multiple laser diode control
- ◆ Optical amplification/pumping
- ◆ Safety related laser controllers

### PACKAGES



QFN28 5 mm x 5 mm

### BLOCK DIAGRAM



### DESCRIPTION

Dual CW laser diode driver iC-HTP can operate two individual laser diodes with up to 750 mA laser current, depending on the heat dissipation. Each channel can be enabled independently. The laser diode driver can be controlled by an external microcontroller (MCU mode) or operated stand-alone with pin/resistor configuration (iC-WK mode). In MCU mode, both channels can be combined for driving up to 1500 mA.

Each channel can be operated individually either in automatic current control (ACC) or automatic power control (APC). All parameters including the internal reference voltages are set via serial communication (I<sup>2</sup>C or SPI). A 10 bit resolution D/A converter with logarithmic characteristic is used for setting the operating point. This allows an operating point resolution better than 1%.

In APC control, the monitor diode photocurrent is used to track the optically emitted power of the laser diode. The feedback for the laser diode driver is the voltage drop of the photocurrent across a monitor resistor. An 8 bit internal programmable logarithmic monitor resistor (PLR) or an external monitor resistor can be selected for closing the control loop. The PLR ranges from 100  $\Omega$  to 407 k $\Omega$  with a step width less than 5%.

In ACC control, the laser diode current can be set directly. The current ranges are selectable.

iC-HTP disables the laser channels when an overcurrent threshold has been exceeded. The overcurrent threshold of each channel has 2 ranges and is programmable through an 8 bit linear D/A converter.

The temperature monitor measures the internal chip temperature. iC-HTP disables the laser channels when overtemperature is detected.

A variety of voltages can be measured with a 10 bit A/D converter. The following voltages can be measured:

- V(LDAx)
- V(VBLx)
- V(VDD)
- V(VB)
- V(PLRx)
- V(MDKx)
- V(RACCx)

The DCO current output pin can control an external DC/DC converter. Controlling the DC/DC output voltage can optimize the power dissipation of the whole system e.g. to extend battery life or reduce total power consumption.

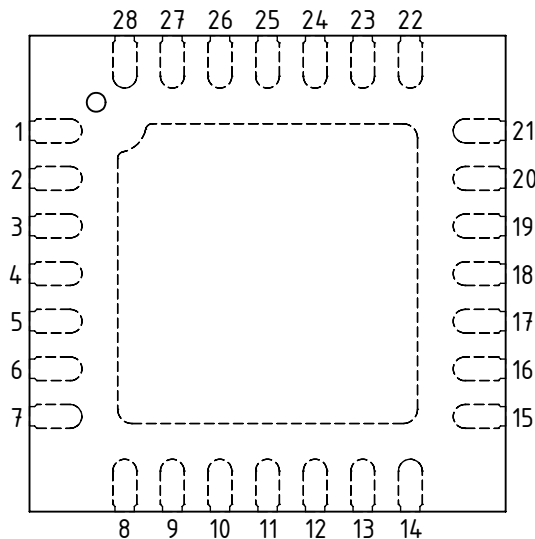
iC-HTP in standby mode has a very low current consumption and does retain its configuration.

Features for **safe operation**:

- Configuration verification
- Tri-state configuration pins
- Write protection in operating mode
- Safe default/startup state
- Software parameter controllable channel disabling
- Hardware pin controllable channel enabling
- Configuration timeout for access monitoring

### PACKAGING INFORMATION QFN28 5 mm x 5 mm

#### PIN CONFIGURATION QFN28 5 mm x 5 mm (topview)



#### PIN FUNCTIONS

| No. | Name     | Function  |
|-----|----------|---|
| 1   | LDA1     | Laser Diode Anode for channel 1   |
| 2   | LDA1     | Laser Diode Anode for channel 1   |
| 3   | VBL1     | Laser Power Supply for channel 1  |
| 4   | CI1      | Integration Capacitor for channel 1   |
| 5   | CIH1     | Integration Capacitor for channel 1, high side                                      |
| 6   | MDK1     | Monitor Diode Cathode for channel 1   |
| 7   | MRH1     | Monitor Resistor for channel 1, high side   |
| 8   | EMC      | Enable Microcontroller input  |
| 9   | SCLK/SCL | SPI Clock / I <sup>2</sup> C Clock  |
| 10  | MISO/SDA | SPI Master In Slave OUT / I <sup>2</sup> C Data                                     |
| 11  | MOSI/A0  | SPI Master Out Slave In / I <sup>2</sup> C Address bit 0                            |
| 12  | NCS/A1   | Chip Select, active low / I <sup>2</sup> C Address bit 1                            |
| 13  | EC1      | Enable Channel 1 input  |
| 14  | EC2      | Enable Channel 2 input  |
| 15  | MRH2     | Monitor Resistor for channel 2, high side   |
| 16  | MDK2     | Monitor Diode Cathode for channel 2   |
| 17  | CIH2     | Integration Capacitor for channel 2, high side                                      |
| 18  | CI2      | Integration Capacitor for channel 2   |
| 19  | VBL2     | Laser Power Supply for channel 2  |
| 20  | LDA2     | Laser Diode Anode for channel 2   |
| 21  | LDA2     | Laser Diode Anode for channel 2   |
| 22  | GND      | Ground  |
| 23  | DCO      | Digital Current Output  |
| 24  | INS/WKR  | I <sup>2</sup> C or SPI selection input / Reference voltage selection in iC-WK mode |
| 25  | VDD      | 3.3 V output supply   |
| 26  | VB       | Power supply  |
| 27  | NCHK     | Error output, active low  |
| 28  | NSTBY    | Standby input, active low   |
| TP  |          | Thermal Pad (GND)   |

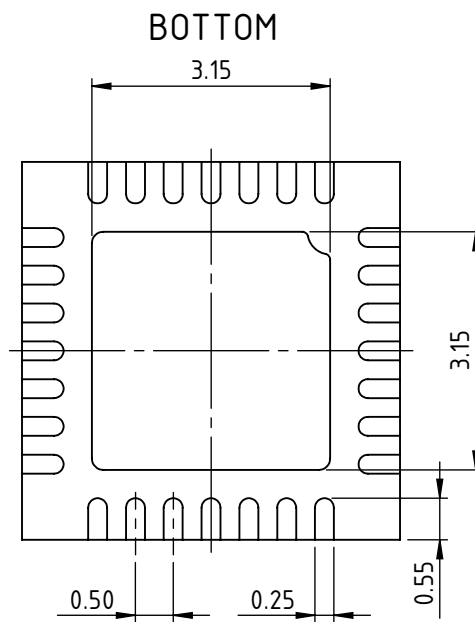
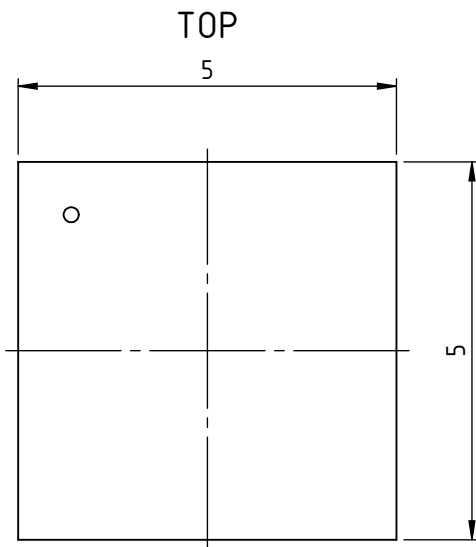
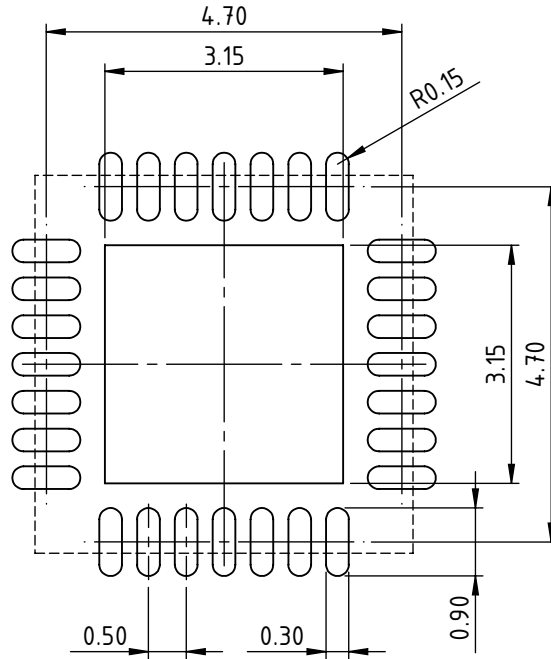
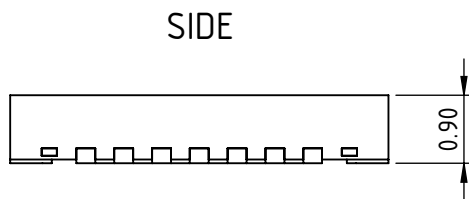
The *Thermal Pad* is to be connected to a *Ground Plane* (GND, AGND1...2) on the PCB.

**Only pin 1 marking on top or bottom defines the package orientation (⊗ HTP label and coding is subject to change).**

## PACKAGE DIMENSIONS QFN28-5x5

All dimensions given in mm.  
This package falls within JEDEC MO-220-VHHD-1.

## RECOMMENDED PCB-FOOTPRINT



# iC-HTP

## DUAL CW P-TYPE LASER DIODE DRIVER



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### ABSOLUTE MAXIMUM RATINGS

These ratings do not imply permissible operating conditions; functional operation is not guaranteed. Exceeding these ratings may damage the device.

| Item No. | Symbol  | Parameter  | Conditions                            | Limits |      | Unit |
|----------|---------|--|---------------------------------------|--------|------|------|
|          |         |  |                                       | Min.   | Max. |      |
| G001     | VB      | Voltage at VB  |                                       | -0.3   | 11   | V    |
| G002     | I(VB)   | Current in VB  |                                       | -20    | 50   | mA   |
| G003     | VDD     | Voltage at VDD   |                                       | -0.3   | 5.5  | V    |
| G004     | I(VDD)  | Current in VDD   |                                       | -20    | 1    | mA   |
| G005     | V()     | Voltage at EC1, EC2, MDK1, MDK2, EMC, SCLK/SCL, MISO/SDA, MOSI/A0, NCS/A1, DCO, INS/WKR, NCHK  |                                       | -0.3   | 5.5  | V    |
| G006     | I()     | Current in CI1, CI2, CIH1, CIH2, EC1, EC2, MDK1, MDK2, EMC, SCLK/SCL, MISO/SDA, MOSI/A0, NCS/A1, DCO, INS/WKR, NCHK, NSTBY, CIL1, CIL2, MRH1, MRH2 |                                       | -20    | 20   | mA   |
| G007     | V()     | Voltage at CI1, CI2, CIH1, CIH2, VBL1, VBL2, LDA1, LDA2, NSTBY   |                                       | -0.3   | 11   | V    |
| G008     | I(AGND) | Current in VBL1, VBL2  | DC current                            | -1     | 900  | mA   |
| G009     | I(LDK)  | Current in LDA1, LDA2  | DC current                            | -900   | 20   | mA   |
| G010     | Vd()    | ESD Susceptibility at all pins   | HBM, 100 pF discharged through 1.5 kΩ |        | 2    | kV   |
| G011     | Tj      | Operating Junction Temperature   |                                       | -40    | 125  | °C   |
| G012     | Ts      | Storage Temperature Range  |                                       | -40    | 150  | °C   |

### THERMAL DATA

Operating Conditions: VB = 2.8 ... 11 V (referenced to GND)

| Item No. | Symbol | Parameter                           | Conditions     | Limits |      |      | Unit |
|----------|--------|-------------------------------------|----------------|--------|------|------|------|
|          |        |                                     |                | Min.   | Typ. | Max. |      |
| T01      | Ta     | Operating Ambient Temperature Range |                | -40    |      | 85   | °C   |
| T02      | Rthja  | Thermal Resistance Chip/Ambient     | Mounted on PCB |        | 25   |      | K/W  |
| T03      | RthjTP | Thermal Resistance Chip/Thermal Pad |                |        | 4    |      | K/W  |

All voltages are referenced to ground unless otherwise stated.

All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

### ELECTRICAL CHARACTERISTICS

 Operating Conditions:  $V_B = 2.8 \dots 11 \text{ V}$  (referenced to GND),  $T_j = -40 \dots 125 \text{ }^\circ\text{C}$  unless otherwise stated

| Item No.   | Symbol                     | Parameter  | Conditions  |                              |                          |                           | Unit                           |
|--|----------------------------|--|---|------------------------------|--------------------------|---------------------------|--------------------------------|
|  |                            |  |   | Min.                         | Typ.                     | Max.                      |                                |
| <b>Total Device</b>  |                            |  |   |                              |                          |                           |                                |
| Functionality and parameters beyond the operating conditions (with reference to independent voltage supplies, for instance) are to be verified within the individual application using FMEA methods. |                            |  |   |                              |                          |                           |                                |
| 001  | $V_B, V_{BLx}$             | Permissible Supply Voltages at $V_B, V_{BLx}$  | Referenced to GND   | 2.8                          |                          | 11                        | V                              |
| 002  | $I(V_B)$                   | Standby Current in $V_B$   | $V(NSTBY) \leq 0.4 \text{ V}$ ,<br>$V_{BL1}$ and $V_{BL2}$ connected to $V_B$ ;<br>$V_B = 2.8 \dots 5 \text{ V}$<br>$V_B = 5 \dots 11 \text{ V}$  |                              |                          | 10<br>30                  | $\mu\text{A}$<br>$\mu\text{A}$ |
| 003  | $I(V_B)$                   | Supply Current in $V_B$  | No load, EC1, EC2, NSTBY = hi   |                              |                          | 5                         | mA                             |
| 004  | $V(V_B)\text{off}$         | Turn-off threshold   | Decreasing $V_B$  | 1                            |                          | 2.6                       | V                              |
| 005  | $V(V_{BLx})\text{off}$     | Turn-off threshold   | Decreasing $V_{BLx}$  | 1                            |                          | 2.6                       | V                              |
| 006  | $V_{BLx}\text{equal}$      | Detection for $V_{BL1}$ not equal to $V_{BL2}$   | Merge mode enabled, $ V_{BL1} - V_{BL2} $   | 0.5                          |                          | 1.3                       | V                              |
| 007  | $V(V_{DD})\text{on}$       | Turn-on threshold  | Increasing VDD  | 1.4                          |                          | 2.2                       | V                              |
| 008  | $V(V_{DD})\text{off}$      | Turn-off threshold   | Decreasing VDD  | 1.2                          |                          | 2.2                       | V                              |
| 009  | $V(V_{DD})\text{Hys}$      | Power-on hysteresis  |   | 20                           |                          | 250                       | mV                             |
| 010  | $V(V_B)\text{INITR}$       | RAM memory reset during Stand-By   | NSTBY = lo  |                              | 1.4*                     |                           | V                              |
| 011  | Ragnd()                    | Resistor to $V_{BLx}$ at CIHx  |   |                              |                          | 20                        | $\Omega$                       |
| 012  | $V_c()\text{lo}$           | Clamp Voltage lo at $V_B, V_{DD}, NCHK, EMC, NCS/A1, MISO/SDA, MOSI/A0, SCLK/SCL, INS/WKR, NSTBY, EC1, EC2, DCO, LDA1, LDA2, CI1, CIH1, CI2, CIH2, AGND1, AGND2, MDK1, MDK2$ | $I() = -10 \text{ mA}$  | -1.6                         |                          | -0.3                      | V                              |
| <b>Laser Driver LDAx, Clx, MDKx</b>  |                            |  |   |                              |                          |                           |                                |
| 101  | $V_s(\text{LDA})\text{lo}$ | Saturation Voltage lo at LDA   | CRNGx = 00, $I(\text{LDAx}) = -750 \text{ mA}$ ,<br>$V_B = 4 \dots 11 \text{ V}$ , $V() = V(V_{BLx}) - V(\text{LDAx})$  |                              |                          | 0.7                       | V                              |
| 102  | $V(\text{LDASAT})$         | LDAx saturation detection threshold  | RLDASx = 00<br>RLDASx = 01<br>RLDASx = 10<br>RLDASx = 11  | 0.4<br>0.6<br>0.9<br>1.1     | 0.6<br>0.8<br>1.1<br>1.3 | 0.9<br>1.1<br>1.2<br>1.5  | V<br>V<br>V<br>V               |
| 103  | $I_{dc}(\text{LDA})$       | Permissible DC Current at LDAx   | EACCx = 1, RACCx = 0, REFx(9:0) = 0x3FF,<br>$V(\text{LDAx}) = V(V_{BLx}) - 0.7 \text{ V}$ ;<br>CRNGx = 00<br>CRNGx = 01<br>CRNGx = 10<br>CRNGx = 11   |                              |                          | -750<br>-100<br>-25<br>-9 | mA<br>mA<br>mA<br>mA           |
| 104  | $I_{leak}(\text{LDA})$     | LDAx leakage current   | $V(\text{LDAx}) = 0 \text{ V}$  | -10                          |                          |                           | $\mu\text{A}$                  |
| 105  | C(CI)                      | Capacitor at CI1, CI2  | ECIE = 1, EMC = hi  | 10                           |                          |                           | nF                             |
| 106  | $I(\text{CI})$             | Charge Current at CI1, CI2   | $V(\text{CI}) = 0 \text{ V}$ , EC1, EC2 = hi, ECIEx = 1   | -150                         |                          | -5                        | $\mu\text{A}$                  |
| 107  | $I(\text{LDA})\text{max}$  | Laser overcurrent shutdown threshold   | CRNGx = 00, EACCx = 0, $V_B = 5 \dots 11 \text{ V}$ ,<br>$V(\text{LDA}) = V(V_{BLx}) - 0.7 \text{ V} \dots 1.5 \text{ V}$ ;<br>ILIMx(7:0) = 0x00, RACCx = 0<br>ILIMx(7:0) = 0xFF, RACCx = 0<br>ILIMx(7:0) = 0x00, RACCx = 1<br>ILIMx(7:0) = 0xFF, RACCx = 1 | -25<br>-2266<br>-3.2<br>-284 |                          | 0<br>-750<br>0<br>-130    | mA<br>mA<br>mA<br>mA           |
| 108  | $\Delta I(\text{LDA})$     | Shutdown threshold resolution  | CRNGx = 00, ILIMx(7:0) = 0x00 to 0xFF;<br>RACCx = 0<br>RACCx = 1  | -8<br>-0.8                   | -4<br>-0.5               | -3<br>-0.3                | mA<br>mA                       |
| 109  | tovc                       | Time to overcurrent shutdown   | Laser current decreased 10%   |                              | 5†                       |                           | $\mu\text{s}$                  |
| 110  | $V(\text{MDK})$            | Voltage at MDK1, MDK2  | Closed control loop, EC1, EC2 = hi;<br>EMC = lo, INS/WKR = lo<br>EMC = lo, INS/WKR = hi   | 110<br>220                   | 125<br>250               | 150<br>295                | mV<br>mV                       |

\* Projected values by sample characterization

† Not tested

### ELECTRICAL CHARACTERISTICS

Operating Conditions: VB = 2.8 ... 11 V (referenced to GND), Tj = -40 ... 125 °C unless otherwise stated

| Item No.                           | Symbol     | Parameter  | Conditions   |                              |                              |                          | Unit                 |
|------------------------------------|------------|--|--|------------------------------|------------------------------|--------------------------|----------------------|
|                                    |            |  |  | Min.                         | Typ.                         | Max.                     |                      |
| 111                                | Ten        | Time to system ready   | NSTBY lo → hi, no load at VDD, CVDD = 1 μF   |                              | 1.3*                         |                          | ms                   |
| 112                                | Tci        | Time to light  | NSTBY = hi, ECIE = 0, COMP = 010, light off to 80 % target value   |                              |                              | 300                      | μs                   |
| 113                                | Tcio       | Time to target light   | Light from 80 % to 99 % target value   |                              |                              | 4700                     | μs                   |
| 114                                | Idc(LDA)   | LDAx ACC mode current  | EC1, EC2, EMC = hi, EACCx = 1, LINLOG = 0, V(LDAx) = V(VBLx) – 0.7 V...1.5 V, VB = 5...11 V, CRNGx = 00; REFx(9:0) = 0x000, RACCx = 0<br>REFx(9:0) = 0x3FF, RACCx = 0<br>REFx(9:0) = 0x000, RACCx = 1<br>REFx(9:0) = 0x3FF, RACCx = 1                  | -200<br>-2200<br>-25<br>-230 | -130<br>-1570<br>-15<br>-160 | -70<br>-940<br>-9<br>-90 | mA<br>mA<br>mA<br>mA |
| 115                                | TK         | Temperature coefficient ACC mode   |  | -1500                        | -500                         |                          | ppm/K                |
| 116                                | IdcLSB     | REFx(9:0) step current at LDA in ACC mode  | EC1, EC2, EMC = hi, EACCx = 1, LINLOG = 0, V(LDAx) = V(VBLx) – 0.7 V...1.5 V, CRNGx = 00; RACCx = 0; REFx(9:0) = 0x000 → 0x001<br>RACCx = 0; REFx(9:0) = 0x30E → 0x30F<br>RACCx = 1; REFx(9:0) = 0x000 → 0x001<br>RACCx = 1; REFx(9:0) = 0x30E → 0x30F | 0.04<br>0.8<br>0.01<br>0.1   |                              | 1<br>2.7<br>0.08<br>0.8  | mA<br>mA<br>mA<br>mA |
| <b>Programmable Resistor</b>       |            |  |  |                              |                              |                          |                      |
| 201                                | Rmdk       | Resistor at MDKx pin   | DISPx = 0; RMDx(7:0) = 0xFF<br>RMDx(7:0) = 0x00  | 350<br>0.154                 | 500<br>0.220                 | 650<br>0.286             | kΩ<br>kΩ             |
| 202                                | Tk         | Temperature coefficient  |  | -1500                        | -500                         | 0                        | ppm/K                |
| 203                                | ΔR         | Percentual resistor increment  | $\Delta R = \frac{R(n+1) - R(n)}{R(n)}$  | 1                            | 3.3                          | 7                        | %                    |
| 204                                | Ileak(MDK) | MDKx leakage current   | DISPx = 1  | -1                           |                              | 1                        | μA                   |
| 205                                | Ron(MDH)   | VDD-MDH Ron resistor   | EMNPx = 0  |                              |                              | 100                      | Ω                    |
| <b>D/A Converter</b>               |            |  |  |                              |                              |                          |                      |
| 301                                | R(DAC)     | D/A converter resolution   |  |                              |                              | 10                       | bit                  |
| 302                                | ΔV         | Percentual voltage increments  | LINLOG = 0, $\Delta V = \frac{V(n+1) - V(n)}{V(n)}$  | 0.05                         | 0.235                        | 1                        | %                    |
| 303                                | ΔV         | Voltage increments   | LINLOG = 1   |                              | 1                            |                          | mV                   |
| 304                                | V(DAC)     | D/A converter  | REFx(9:0) = 0x000 lowest value<br>REFx(9:0) = 0x3FF highest value  | 0.09<br>1.00                 | 0.10<br>1.10                 | 0.12<br>1.25             | V<br>V               |
| 305                                | DATK†      | DAC Temperature Accuracy   | REFx(9:0) = 0x3FF highest value  | -2.5                         |                              | 2.5                      | %                    |
| <b>Check Output NCHK</b>           |            |  |  |                              |                              |                          |                      |
| 401                                | Vs()lo     | Saturation Voltage lo at NCHK  | I(NCHK) = 1.0 mA   |                              |                              | 0.4                      | V                    |
| 402                                | Isc()lo    | Short Circuit Current lo at NCHK   | V(NCHK) = 0.4 ... 3.3 V  | 9                            |                              | 33                       | mA                   |
| 403                                | Iik()      | Leakage Current at NCHK  | NCHK = 1, V(NCHK) = 0 ... 5.5 V  | -10                          |                              | 10                       | μA                   |
| <b>Series Regulator Output VDD</b> |            |  |  |                              |                              |                          |                      |
| 501                                | V(VDD)     | Regulated output voltage   | VB ≥ 3.7 V, I(VDD) = -10 ... 0 mA, NSTBY = hi  | 3                            |                              | 3.5                      | V                    |
| 502                                | V(VB,VDD)  | Voltage Drop between VB and VDD  | VDD unregulated, I(VDD) = -10 ... 0 mA, NSTBY = hi   |                              | 100                          | 400                      | mV                   |
| 503                                | C(VOUT)    | Capacitor at VDD   | Ri(C) < 1 Ω  | 1                            |                              | 3.3                      | μF                   |
| 504                                | Tvdd       | Settling time VDD  | NSTBY lo → hi, no load at VDD, V(VDD) 0 to 90 %, CVDD = 1 μF   |                              |                              | 1                        | ms                   |
| <b>Digital inputs</b>              |            |  |  |                              |                              |                          |                      |
| 601                                | Vt()hi     | Input Threshold Voltage hi at NCS/A1, MISO/SDA, MOSI/A0, SCLK/SCL, NSTBY, EC1, EC2 |  |                              |                              | 2                        | V                    |
| 602                                | Vt()lo     | Input Threshold Voltage lo at NCS/A1, MISO/SDA, MOSI/A0, SCLK/SCL, NSTBY, EC1, EC2 |  | 0.8                          |                              |                          | V                    |

\* Projected values by sample characterization

† Safe by design

### ELECTRICAL CHARACTERISTICS

 Operating Conditions:  $V_B = 2.8 \dots 11 \text{ V}$  (referenced to GND),  $T_j = -40 \dots 125 \text{ }^\circ\text{C}$  unless otherwise stated

| Item No.                   | Symbol   | Parameter  | Conditions  | Min.     | Typ.     | Max.      | Unit             |
|----------------------------|----------|--|---|----------|----------|-----------|------------------|
|                            |          |  |   |          |          |           |                  |
| 603                        | Vt(jhys) | Hysteresis at NCS/A1, MISO/SDA, MOSI/A0, SCLK/SCL, NSTBY, EC1, EC2                         | $V_t(jhys) = V_t(jhi) - V_t(jlo)$   | 100      |          |           | mV               |
| 604                        | Ipd()    | Pull-Down Current at MOSI/A0, EC1, EC2   | $V() = 0.4 \text{ V} \dots V_{DD}$  | 1        |          | 50        | $\mu\text{A}$    |
| 605                        | Ipd()    | Pull-Down Current at NSTBY   | $V() = 0.4 \text{ V} \dots V_B$   | 0.7      |          | 50        | $\mu\text{A}$    |
| 606                        | Rpu()    | Pull-Up Resistor at SCLK/SCL, NCS/A1   |   | 80       | 150      | 260       | k $\Omega$       |
| 607                        | Rpu()    | Pull-Up Resistor at MISO/SDA   | EMC = hi, INS/WKR = hi  | 53       | 100      | 174       | k $\Omega$       |
| 608                        | Er()     | Safe enable threshold voltage at EMC, INS/WKR  | Rising<br>Falling   | 52<br>30 | 54<br>32 | 56<br>34  | % VDD<br>% VDD   |
| 609                        | Voc()    | Open Circuit Voltage at EMC, INS/WKR   |   | 39       | 41       | 43        | % VDD            |
| 610                        | Ri()     | Internal Resistance at EMC, INS/WKR  |   | 170      | 250      | 330       | k $\Omega$       |
| 611                        | Isc(jlo) | Short Circuit current I <sub>o</sub> in MISO/SDA   | EMC = hi, INS/WKR = lo, V(MISO/SDA) = 5.5 V   | -40      |          | -4        | mA               |
| 612                        | Vs(jlo)  | Saturation Voltage I <sub>o</sub> at MISO/SDA  | EMC = hi, INS/WKR = lo, I(MISO/SDA) = 2 mA  |          |          | 0.4       | V                |
| 613                        | Vs(jhi)  | Saturation Voltage I <sub>o</sub> at MISO/SDA  | EMC = hi, INS/WKR = lo, V <sub>s(jhi)</sub> = VDD - V(), I <sub>load</sub> = 10 $\mu\text{A}$ |          |          | 0.4       | V                |
| <b>A/D Converter</b>       |          |  |   |          |          |           |                  |
| 701                        | Ton*     | ADC initialization time. Time to wait after ADC source changed before ADCC(2) is set to 1. | ADCCx(1:0) changed  |          |          | 500       | $\mu\text{s}$    |
| 702                        | Tconv    | Conversion time  | ADCC(2) 0 → 1 to DRDY 0 → 1   |          |          | 140       | $\mu\text{s}$    |
| 703                        | R(ADC)   | A/D Converter Resolution   |   |          |          | 10        | bit              |
| 704                        | RAC†     | Relative Accuracy  |   | -1       |          | +1        | LSB              |
| 705                        | VZS()    | Zero Scale Voltage   | ADCx(9:0) = 000h  |          | 0        |           | V                |
| 706                        | VFS()    | Full Scale Voltage   | ADCx(9:0) = 3FFh  | 1.0      | 1.1      | 1.25      | V                |
| 707                        | MDKM     | MDKx Measurement   | MDKx = 0.5 V, ADCCx(2:0) = 100, ADFNSx = 1  | 372      | 465      | 558       | LSB              |
| 708                        | VDDM     | VDD Measurement  | VDD = 3.3 V, ADCC2(2:0) = 101   | 312      | 390      | 468       | LSB              |
| 709                        | VBM      | VB Measurement   | VB = 11 V, ADCC1(2:0) = 101   | 744      | 930      | 1023      | LSB              |
| 710                        | VBLM     | VBLx Measurement   | VBLx = 11 V, ADCCx(2:0) = 110   | 744      | 930      | 1023      | LSB              |
| 711                        | LDAM     | LDAx Measurement   | LDAx = 11 V, ADCCx(2:0) = 111   | 744      | 930      | 1023      | LSB              |
| <b>Pulse Mode</b>          |          |  |   |          |          |           |                  |
| 801                        | Tdis     | Time to CI active discharge  | ENx high → low to Discharge CI activated  | 300      |          |           | $\mu\text{s}$    |
| 802                        | tr()     | Current rise time at LDA   | ENx low → high, Regulation active   |          |          | 2         | $\mu\text{s}$    |
| 803                        | tf()     | Current fall time at LDA   | ENx high → low, Regulation active   |          |          | 2         | $\mu\text{s}$    |
| <b>Overtemperature</b>     |          |  |   |          |          |           |                  |
| B01                        | Toff     | Overtemperature Shutdown   | Rising temperature  | 130      |          | 170       | $^\circ\text{C}$ |
| B02                        | Ton      | Overtemperature Release  | Falling temperature   | 125      |          | 165       | $^\circ\text{C}$ |
| B03                        | Thys     | Hysteresis   | Toff - Ton  | 3        |          |           | $^\circ\text{C}$ |
| <b>Temperature Monitor</b> |          |  |   |          |          |           |                  |
| C01                        | Trange   | Temperature Measurement Range  |   | -40      |          | 125       | $^\circ\text{C}$ |
| C02                        | Tresol   | Temperature Measurement Resolution   |   |          | 1        |           | $^\circ\text{C}$ |
| C03                        | Reading  | Temperature Value Ranges   | $T_j = 125 \text{ }^\circ\text{C}$<br>$T_j = -40 \text{ }^\circ\text{C}$                      | 170<br>0 |          | 210<br>45 | digits<br>digits |

\* Safe by design

† Safe by design



### ELECTRICAL CHARACTERISTICS

Operating Conditions:  $V_B = 2.8 \dots 11 \text{ V}$  (referenced to GND),  $T_j = -40 \dots 125 \text{ }^\circ\text{C}$  unless otherwise stated

| Item No.          | Symbol    | Parameter                  | Conditions  | Min. | Typ. | Max. | Unit          |
|-------------------|-----------|----------------------------|---|------|------|------|---------------|
|                   |           |                            |   |      |      |      |               |
| <b>DCO Output</b> |           |                            |   |      |      |      |               |
| D01               | Isc()hi   | DCO Output Current         | $V(VDD) = 3 \dots 3.5 \text{ V}$ , $V(DCO) = 0 \text{ V}$ , $RDCO = 0x3F$ | -175 | -130 | -85  | $\mu\text{A}$ |
| D02               | Ileak     | Leakage Current at DCO     | $RDCO = 0x00$ or $NSTBY = lo$ , $V(DCO) = 0 \text{ V}$                    | -1   |      | 1    | $\mu\text{A}$ |
| D03               | I(DCO)LSB | I(DCO) Resolution          | $V(DCO) = 0 \text{ V}$  | 1.3  | 2    | 2.7  | $\mu\text{A}$ |
| <b>Oscillator</b> |           |                            |   |      |      |      |               |
| E01               | Fosc      | Oscillator Frequency       | $NSTBY = hi$  | 100  | 200  | 300  | kHz           |
| E02               | T(cfgtmo) | Configuration Mode Timeout | $MODE(1:0) = 10$  | 40   | 82   | 164  | ms            |
| E03               | tWDT      | Watchdog Timeout           | $NSTBY = hi$  | 20   |      | 200  | $\mu\text{s}$ |

### OPERATING REQUIREMENTS: SPI and I<sup>2</sup>C Interface

Operating Conditions:  $V_B = 2.8 \dots 11 \text{ V}$ ,  $T_j = -40 \dots 125 \text{ }^\circ\text{C}$

| Item No.                                     | Symbol  | Parameter   | Conditions   | Min. | Max. | Unit |
|--|---------|---|--|------|------|------|
|  |         |   |  |      |      |      |
| <b>SPI / I<sup>2</sup>C Interface Timing</b> |         |   |  |      |      |      |
| I001   | tsCCL   | Setup Time:<br>NCS/A1 hi $\rightarrow$ lo before SCLK lo $\rightarrow$ hi | $INS/WKR = lo$   | 20   |      | ns   |
| I002   | tsDCL   | Setup Time:<br>MOSI/A0 stable before SCLK/SCL lo $\rightarrow$ hi         | $INS/WKR = lo$   | 20   |      | ns   |
| I003   | thDCL   | Hold Time:<br>MOSI/A0 stable after SCLK/SCL lo $\rightarrow$ hi           | $INS/WKR = lo$   | 20   |      | ns   |
| I004   | tCLH    | Signal Duration SCLK/SCL hi   | $INS/WKR = lo$   | 50   |      | ns   |
| I005   | tCLL    | Signal Duration SCLK/SCL lo   | $INS/WKR = lo$   | 50   |      | ns   |
| I006   | thCLC   | Hold Time:<br>NCS/A1 lo after SCLK/SCL hi $\rightarrow$ lo                | $INS/WKR = lo$   | 20   |      | ns   |
| I007   | tCSH    | Signal Duration NCS/A1 hi   | $INS/WKR = lo$   | 50   |      | ns   |
| I008   | tpCLD   | Propagation Delay:<br>MISO/SDA stable after SCLK/SCL hi $\rightarrow$ lo  | $INS/WKR = lo$ , $V(VDD) > 3 \text{ V}$ , $C_{load} = 10 \text{ pF}$ , no external pull-up | 0    | 30   | ns   |
| I009   | tHIZ    | MISO to HIZ delay   | $INS/WKR = lo$ , HIZ = high impedance state  | 0    | 25   | ns   |
| I010   | f(SCLK) | SPI clock frequency   |  |      | 10   | MHz  |
| I011   | f(SCL)  | I <sup>2</sup> C clock frequency  |  |      | 400  | kHz  |

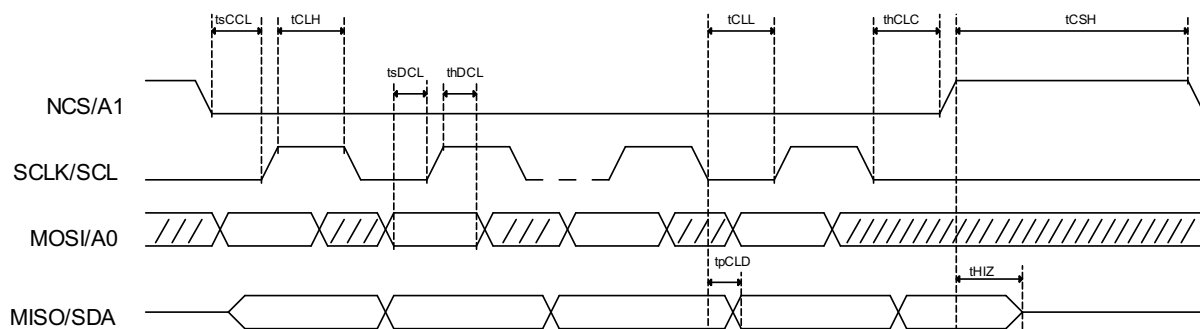


Figure 1: SPI interface timing

### OPERATING MODES AND STANDBY

iC-HTP has two operating modes:

#### iC-WK mode

iC-HTP operates as an Automatic Power Control (APC) laser controller, similar to iC-Haus' **iC-WKP**. iC-WKP mode is set by pin configuration and external resistor. Pin EMC is set to lo and pin INS/WKR selects the reference voltage. Floating pins EMC and INS/WKR are detected as faulty configuration and signaled at NCHK.

#### MCU mode

In microcontroller unit (MCU) mode, iC-HTP features two control modes: automatic power control (APC) and automatic current control (ACC). Pin EMC is set to hi and pin INS/WKR selects the serial communication interface protocol: hi for I<sup>2</sup>C and lo for SPI. Floating pins

EMC and INS/WKR are detected as faulty configuration and signaled at NCHK.

#### Standby

iC-HTP in standby has a very low current consumption and does retain its configuration. Standby will not reset the internal RAM.

In order to exit standby, pin NSTBY must be set to hi (e.g. VB). VDD is switched off in standby and can not be used to exit standby.

Clx, CIHx, VB, VBLx, NSTBY and LDAx withstand voltages up to 11 V, whereas the remaining input pins operate up to 5.5 V and do have high impedance at standby.

### LASER DIODE/LED TYPES AND OPERATION MODES

For automatic Power Control (APC) operation mode a monitor diode is required. This APC operation is possible in microcontroller unit (MCU) mode and in the iC-WK mode.

In iC-WK mode only P-type laser diodes are supported. In MCU mode P-type and M-type laser diodes are supported.

In automatic current control (ACC) operation there is no monitor diode and any diode can be operated.

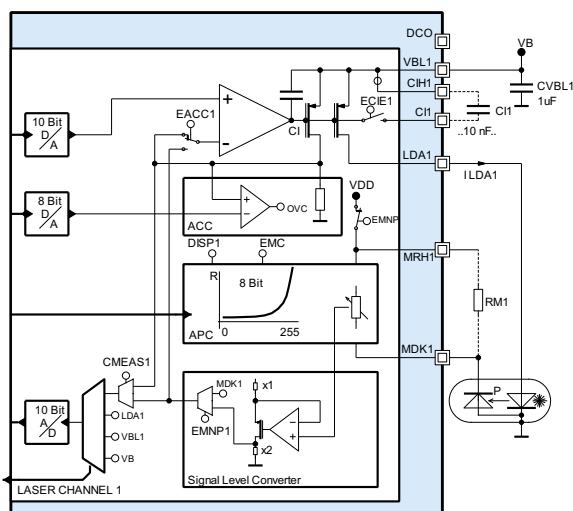


Figure 2: iC-HTP with P-type laser diode

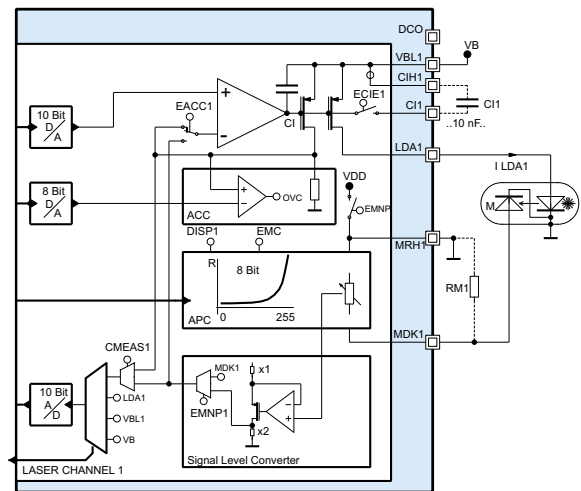


Figure 3: iC-HTP with M-type laser diode

|              |                       |       |
|--------------|-----------------------|-------|
| <b>EMNP1</b> | Addr. 0x1A; bit bit 3 | R/W 0 |
| <b>EMNP2</b> | Addr. 0x1A; bit bit 7 | R/W 0 |
| Code         | Function              |       |
| 0            | P-Laser Type          |       |
| 1            | M-Laser Type          |       |

Table 5: Laser Typ selection

# iC-HTP

## DUAL CW P-TYPE LASER DIODE DRIVER



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### iC-WK MODE

Setting pin EMC = Lo configures iC-HTP for iC-WK mode.

tors are disabled, therefore external resistors at pins MDKx are required.

| Reference voltage in iC-WK mode |                   |
|---------------------------------|-------------------|
| INS/WKR                         | Reference voltage |
| Lo                              | VDD – 0.125 V     |
| Hi                              | VDD – 0.250 V     |

Table 6: Reference selection (cf. *Electrical Characteristics No. 110*)

The APC reference can be set to two different values by means of pin INS/WKR, as shown in Table 6, and the overcurrent threshold is set to its maximum value of 750 mA (cf. *Electrical Characteristics No. 107*). In case of overcurrent, the respective channel is disabled. For re-enabling the channel, the corresponding ECx pin must be cycled.

In iC-WK mode both channels operate in APC mode. The internal programmable logarithmic monitor resis-

External CI capacitors must be added in this operation mode at pins C1x/CIHx. Figure 4 shows an example in iC-WK mode using a P-type laser diode, with VDD – 0.250 V reference selected.

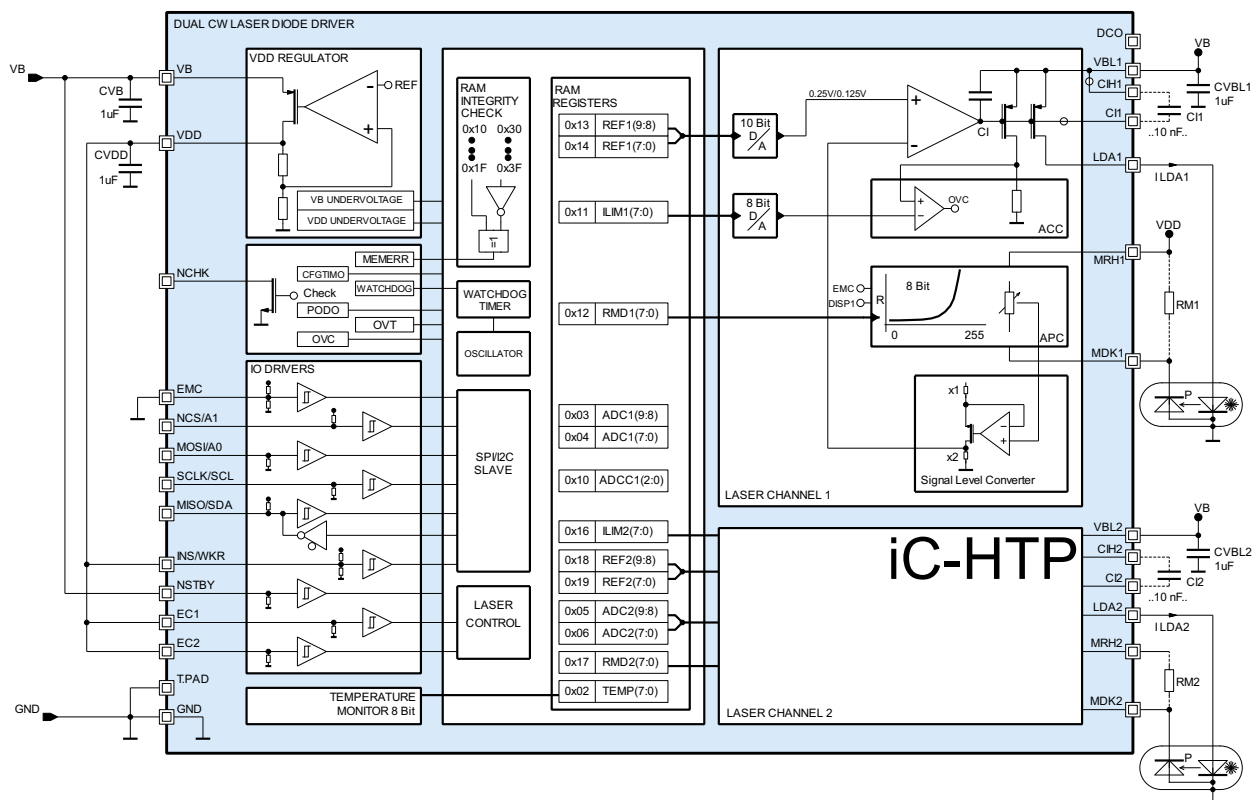


Figure 4: iC-HTP in iC-WK mode with P-type laser diode and reference VDD – 0.250V

In the configuration from Figure 4 pin NSTBY is connected to Vb. This is required to force iC-HTP leaving standby mode and starting normal operation.

#### Laser channel enabling

Setting pins EC1, EC2 to hi enables the corresponding channels. In order to ensure safe operation of iC-HTP, several events automatically disable both output channels:

- Pins INS/WKR or EMC left unconnected (INSOPEN, EMCOPEN): iC-HTP enters error mode and the laser channels cannot be enabled.
- Supply power down either at Vb (PDOVBLx) or VDD (PDOVDD): The laser channels are unconditionally disabled during the power down event.
- Overcurrent (OVC) or overtemperature (OVT): Laser channels are switched off. Cycling pins

# iC-HTP

## DUAL CW P-TYPE LASER DIODE DRIVER



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EC1, EC2 or a power-up is required to switch on the laser again.

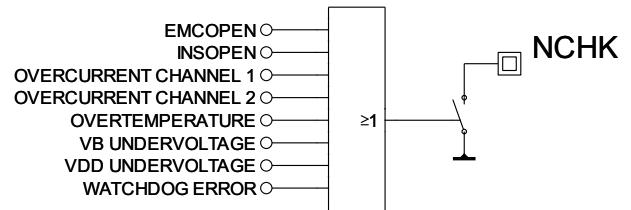


Figure 5: iC-HTP in iC-WK mode, NCHK behavior

### MICROCONTROLLER MODE

Setting pin EMC to hi configures iC-HTP for microcontroller mode (MCU mode) with I<sup>2</sup>C or SPI.

The configuration of the parameters of iC-HTP must be done in configuration mode. In this mode, the configuration memory can be written and read back without changing the current configuration of iC-HTP. Once the configuration is considered as valid, iC-HTP can be switched to operation mode. These two modes are configured by the MODE register. The time elapsed in configuration may not exceed 40 ms. If this timeout is exceeded, both channels will be switched off.

Each individual channel can be enabled by setting pin ECx to hi. Setting register bits DISCx to 1 disables the corresponding channel. If either pin ECx is lo or register bits DISCx is 1, the corresponding channel is disabled.

| DISC1 |  | Addr. 0x10; bit 3 | R/W 1 |
|-------|--|-------------------|-------|
| Code  | Function                               |                   |       |
| 0     | Channel 1 can be enabled by pin EC1    |                   |       |
| 1     | Channel 1 cannot be enabled by pin EC1 |                   |       |

Table 7: Disable channel 1

| DISC2 |  | Addr. 0x15; bit 3 | R/W 1 |
|-------|--|-------------------|-------|
| Code  | Function                               |                   |       |
| 0     | Channel 2 can be enabled by pin EC2    |                   |       |
| 1     | Channel 2 cannot be enabled by pin EC2 |                   |       |

Table 8: Disable channel 2

The following voltages can be measured using a 10 bit A/D converter with two resolutions:

- V(LDAx) up to 11 V with 11.81 mV resolution
- V(VDD) up to 8 V with 8.6 mV resolution
- V(VB) up to 11 V with 11.81 mV resolution
- V(VBLx) up to 11 V with 11.81 mV resolution
- V(MDKx) up to 1.1 V with 1.075 mV resolution
- V(PLRx) up to 1.1 V with 1.075 mV resolution
- V(RACC) up to 1.1 V with 1.075 mV resolution

The register bits ADCCx select the signal measured with the 10 bit A/D converter.

| ADCC1(2:0) |   | Addr. 0x10; bit 7:5 | R/W 000 |
|------------|---|---------------------|---------|
| Code       | Function  |                     |         |
| 0xx        | Channel 1 ADC disabled                                  |                     |         |
| 100        | Channel 1 ADC sourced by V(MDK1), ADFNS1 = 1, CMES1 = 0 |                     |         |
| 100        | Channel 1 ADC sourced by V(PLR1), ADFNS1 = 0, CMES1 = 0 |                     |         |
| 100        | Channel 1 ADC sourced by ACC current sensor, CMES1 = 1  |                     |         |
| 101        | Channel 1 ADC sourced by V(VB)                          |                     |         |
| 110        | Channel 1 ADC sourced by V(VBL1)                        |                     |         |
| 111        | Channel 1 ADC sourced by V(LDA1)                        |                     |         |

Table 9: ADC channel 1 source selection

| ADCC2(2:0) |   | Addr. 0x15; bit 7:5 | R/W 000 |
|------------|---|---------------------|---------|
| Code       | Function  |                     |         |
| 0xx        | Channel 2 ADC disabled                                  |                     |         |
| 100        | Channel 2 ADC sourced by V(MDK2), ADFNS2 = 1, CMES2 = 0 |                     |         |
| 100        | Channel 2 ADC sourced by V(PLR2), ADFNS2 = 0, CMES2 = 0 |                     |         |
| 100        | Channel 2 ADC sourced by ACC current sensor, CMES2 = 1  |                     |         |
| 101        | Channel 2 ADC sourced by V(VDD)                         |                     |         |
| 110        | Channel 2 ADC sourced by V(VBL2)                        |                     |         |
| 111        | Channel 2 ADC sourced by V(LDA2)                        |                     |         |

Table 10: ADC channel 2 source selection

With ADCCx(2:0) = 100, the signal to the A/D converter is selected by register bit ADFNSx. With ADFNSx = 0 the measuring point to the A/D converter is the internal sense node of the internal programmable logarithmic monitor resistor (PLR) after the x2 level shifting. With ADFNSx = 1 the sensing point is connected directly to the MDKx pin. Note that in this case, only voltages from 0 to 1.1 V can be monitored with the A/D converter. With the CMESx bit, the ADC can be used for laser current measurement in ACC mode. For this measurement, the ADCCx register must be set to 100. As shown in

Figure 8, a fraction of the current delivered by the driver to the laser is mirrored to a resistor. The voltage drop at this resistor is sourced to the ADC. For a more detailed explanation of the current measurement, please refer to the ADC chapter.

| ADFNS1 |  | Addr. 0x1A; bit 2 | R/W 0 |
|--------|--|-------------------|-------|
| Code   | Function   |                   |       |
| 0      | ADC measurement PLR1 after x2 level shifting (sense) |                   |       |
| 1      | ADC measurement MDK1 pad (force)                     |                   |       |

Table 11: ADC channel 1 force/sense selection

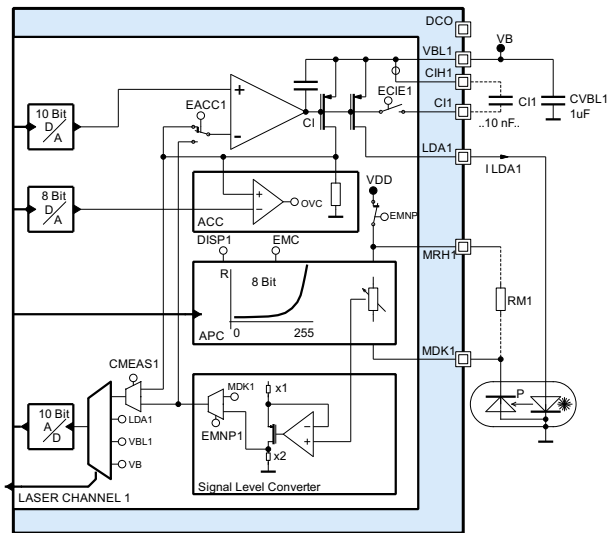


Figure 6: Channel 1 schematic

| ADFNS2 |  | Addr. 0x1A; bit 6 | R/W 0 |
|--------|--|-------------------|-------|
| Code   | Function   |                   |       |
| 0      | ADC measurement PLR2 after x2 level shifting (sense) |                   |       |
| 1      | ADC measurement MDK2 pad (force)                     |                   |       |

Table 12: ADC channel 2 force/sense selection

| CMES1 |                               | Addr. 0x1A; bit bit 1 | R/W 0 |
|-------|-------------------------------|-----------------------|-------|
| CMES2 |                               | Addr. 0x1A; bit bit 5 | R/W 0 |
| Code  | Function                      |                       |       |
| 0     | Optical Power selected for AD |                       |       |
| 1     | Laser current selected for AD |                       |       |

Table 13: AD selection with ADCCx(2:0)=100

Two different control modes can be configured independent for each channel: automatic power control (APC) and automatic current control (ACC). In both modes a 10 bit logarithmic D/A converter sets the reference voltage and an 8 bit programmable D/A converter configures the overcurrent threshold.

### APC mode

In APC mode the laser power is controlled. The monitor diode current ( $I_{mon}$ ) is used as feedback in the laser power control loop. APC mode is selected by setting the EACCx register bit to 0.

| EACC1 |   | Addr. 0x10; bit 0 | R/W 0 |
|-------|---|-------------------|-------|
| Code  | Function  |                   |       |
| 0     | APC mode enabled for channel 1 (light power regulation)   |                   |       |
| 1     | ACC mode enabled for channel 1 (laser current regulation) |                   |       |

Table 14: Enable APC/ACC channel 1

| EACC2 |   | Addr. 0x15; bit 0 | R/W 0 |
|-------|---|-------------------|-------|
| Code  | Function  |                   |       |
| 0     | APC mode enabled for channel 2 (light power regulation)   |                   |       |
| 1     | ACC mode enabled for channel 2 (laser current regulation) |                   |       |

Table 15: Enable APC/ACC channel 2

An example of APC with default configuration is shown in figure 7.

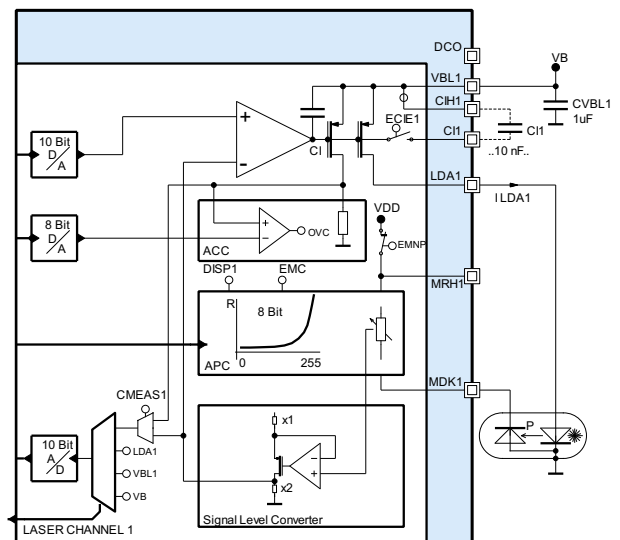


Figure 7: APC mode simplified

An internal 8 bit programmable logarithmic monitor resistor (PLR) can be used in APC mode. It is also possible to use an external monitor resistor connected to pin MDKx. If the register bit DISPx is 0, the PLR is present. If DISPx is 1, the PLR is disabled and an external monitor resistor must be used.

| DISP1 |                            | Addr. 0x10; bit 2 | R/W 0 |
|-------|----------------------------|-------------------|-------|
| Code  | Function                   |                   |       |
| 0     | PLR enabled for channel 1  |                   |       |
| 1     | PLR disabled for channel 1 |                   |       |

Table 16: Disable PLR channel 1

| DISP2 |                            | Addr. 0x15; bit 2 | R/W 0 |
|-------|----------------------------|-------------------|-------|
| Code  | Function                   |                   |       |
| 0     | PLR enabled for channel 2  |                   |       |
| 1     | PLR disabled for channel 2 |                   |       |

Table 17: Disable PLR channel 2

Both programmable logarithmic monitor resistors (PLR) feature a wide logarithmic resistor range from 100 Ω to 407 kΩ, in steps of typically 3.3%. This covers a wide range of monitor currents.

For fine-tuning the optical power, the reference voltage can be set with a 10 bit logarithmic D/A converter, which is configurable through register REFx. This converter has a voltage range that ranges typically from 0.1 to 1.1 V, allowing an operation resolution of typically 0.235% over the whole range. Optionally the reference voltage D/A converter can be configured as a linear one with the same voltage range. Linear or logarithmic D/A reference voltage can be set with register bit LINLOGx.

Inside the control loop there is the signal level converter, which references the values coming from the PLRx to GND. This is necessary because the logarithmic D/A is referenced to GND. In addition this signal level converter adds a 1:2 ratio between the voltage regulated at PLRx and the one regulated at the logarithmic D/A converter i.e. 1.1 V regulated at the logarithmic D/A side are 0.55 V regulated at the PLRx side.

For calculating the minimum value of the monitor current,  $I_{mon}$ ,  $V_{ref\_max}(0x00)$  (cf. *Electrical Characteristics No. 304*) and  $Rmda_{min}(RMDx = 0xFF)$  (cf. *Electrical Characteristics No. 201*) are used. Also the 1:2 ratio between PLRx regulation voltage and  $V_{ref}$  must be applied.

$$I_{mon\_min} = \frac{V_{ref\_max}(0x00)}{2 \cdot Rmda_{min}(RMDx=0xFF)} = \frac{0.11 \text{ V}}{2 \cdot 350000 \Omega} = 0.16 \mu\text{A}$$

It is not recommended to configure iC-HTP to such small  $I_{mon}$  values, otherwise the leakage current at MDKx may have an influence (cf. *Electrical Characteristics No. 204*), especially at high temperatures. To avoid this,  $I_{mon}$  should be much higher than the leakage current.

For calculating the maximum value of  $I_{mon}$ ,  $V_{ref\_min}(0x3FF)$  (cf. *Electrical Characteristics No. 304*)

and  $Rmda_{max}(RMDx = 0x00)$  (cf. *Electrical Characteristics No. 201*) are used. Also the 1:2 ratio between PLRx regulation voltage and  $V_{ref}$  must be applied. Since only the 4 MSB from PLR can be accessed at pin MDKx, the following formula needs to be used for calculating  $Rmda_{max}(RMDx = 0x00)$ :

$$Rmd = Rmd_0 \left(1 + \frac{\Delta Rmd(\%)}{100}\right)^{n+1}, n \text{ from } 0 \text{ to } 255$$

$$Rmda_{max}(RMDx = 0x00) = Rmd_0 \left(1 + \frac{\Delta Rmd(\%)}{100}\right)^{16}$$

$$286 = Rmd_0 \left(1 + \frac{3.3}{100}\right)^{16}$$

$$Rmd_0 = 170 \Omega$$

Therefore:

$$I_{mon\_max} = \frac{V_{ref\_min}(0x3FF)}{2 \cdot Rmd_0} = \frac{1.00 \text{ V}}{2 \cdot 170 \Omega} = 2.94 \text{ mA}$$

Any other  $I_{mon}$  value can be calculated using  $Rmd$  formula above. Due to its logarithmic characteristic, the steps between two consecutive values is kept within 3.3 % typical value.

A programmable overcurrent shutdown can be set to protect the laser by disabling the channel. The overcurrent protection value ( $I_{lim}$ ) must be configured in register ILIMx using the following equations:

$$I_{lim} = (\Delta I(LDA)_{max}) * n * k$$

$$n = \frac{I_{lim}}{k * \Delta I(LDA)_{max}}$$

with n from 1 to 255.

ILIM set to 0x00 disables the overcurrent protection in ACC mode. In APC mode, the overcurrent protection cannot be disabled with ILIM. In both modes (APC and ACC mode) overcurrent is disabled when using the linear reference D/A setting register bit LINLOGx.

Note: The accuracy of the overcurrent detection depends on the correct biasing of the driver stage. If the driver is saturated, the accuracy of the overcurrent detection is reduced and may not work as expected. Saturation voltage (*Electrical Characteristics No. 101*) must be ensured for a proper function of the overcurrent detection. LDASAT1 and LDASAT2 status bits can be used for anticipated saturation detection.

$\Delta I(LDA)_{max}$  is the shutdown current threshold resolution (maximum value) (cf. *Electrical Characteristics No. 108*). Its value depends on the current range defined by register bit RACCx. If RACCx = 1, the overcurrent threshold is in the low range and  $\Delta I(LDA)_{max} = 0.375 \text{ mA}$ . If RACCx = 0, the overcurrent threshold is in the high range and  $\Delta I(LDA)_{max} = 3 \text{ mA}$ .

| CRNG1(1:0) |   | Addr. 0x1E; bit 1:0 | R/W 00 |
|------------|---|---------------------|--------|
| Code       | Function  |                     |        |
| 00         | Output current range from 0 to 750 mA, RACC1 = 0, k factor set to 750/750 = 1     |                     |        |
| 01         | Output current range from 0 to 100 mA, RACC1 = 0, k factor set to 100/750, = 0.13 |                     |        |
| 10         | Output current range from 0 to 25 mA, RACC1 = 0, k factor set to 25/750 = 0.03    |                     |        |
| 11         | Output current range from 0 to 9 mA, RACC1 = 0, k factor set to 9/750 = 0.012     |                     |        |
| 00         | Output current range from 0 to 90 mA, RACC1 = 1, k factor set to 750/750 = 1      |                     |        |
| 01         | Output current range from 0 to 12 mA, RACC1 = 1, k factor set to 100/750 = 0.13   |                     |        |
| 10         | Output current range from 0 to 3 mA, RACC1 = 1, k factor set to 25/750 = 0.03     |                     |        |
| 11         | Output current range from 0 to 1.1 mA, RACC1 = 1, k factor set to 9/750 = 0.012   |                     |        |

Table 18: Current range channel 1

| CRNG2(1:0) |   | Addr. 0x1E; bit 5:4 | R/W 00 |
|------------|---|---------------------|--------|
| Code       | Function  |                     |        |
| 00         | Output current range from 0 to 750 mA, RACC2 = 0, k factor set to 750/750 = 1     |                     |        |
| 01         | Output current range from 0 to 100 mA, RACC2 = 0, k factor set to 100/750, = 0.13 |                     |        |
| 10         | Output current range from 0 to 25 mA, RACC2 = 0, k factor set to 25/750 = 0.03    |                     |        |
| 11         | Output current range from 0 to 9 mA, RACC2 = 0, k factor set to 9/750 = 0.012     |                     |        |
| 00         | Output current range from 0 to 90 mA, RACC2 = 1, k factor set to 750/750 = 1      |                     |        |
| 01         | Output current range from 0 to 12 mA, RACC2 = 1, k factor set to 100/750 = 0.13   |                     |        |
| 10         | Output current range from 0 to 3 mA, RACC2 = 1, k factor set to 25/750 = 0.03     |                     |        |
| 11         | Output current range from 0 to 1.1 mA, RACC2 = 1, k factor set to 9/750 = 0.012   |                     |        |

Table 19: Current range channel 2

Register CRNGx splits each current range into 4 additional current ranges. k is a current range factor with its value depending on the CRNGx(1:0) register:

| ILIM1 |   | Addr. 0x11; bit 7:0 | R/W 0xFF |
|-------|---|---------------------|----------|
| Code  | Function  |                     |          |
| 0x00  | Channel 1 overcurrent threshold set to the minimum current in APC mode (EACC1 = 0) or overcurrent protection disabled in ACC mode (EACC1 = 1) |                     |          |
| ...   | Channel 1 overcurrent threshold set to $I_{lim} = (\Delta I(LDA), max \cdot n \cdot k)$ , n from 0 to 255                                     |                     |          |
| 0xFF  | Channel 1 overcurrent threshold set to the maximum current  |                     |          |

Table 20: Overcurrent threshold configuration channel 1

| ILIM2 |   | Addr. 0x16; bit 7:0 | R/W 0xFF |
|-------|---|---------------------|----------|
| Code  | Function  |                     |          |
| 0x00  | Channel 2 overcurrent threshold set to the minimum current in APC mode (EACC2 = 0) or overcurrent protection disabled in ACC mode (EACC2 = 1) |                     |          |
| ...   | Channel 2 overcurrent threshold set to $I_{lim} = (\Delta I(LDA), max \cdot n \cdot k)$ , n from 0 to 255                                     |                     |          |
| 0xFF  | Channel 2 overcurrent threshold set to the maximum current  |                     |          |

Table 21: Overcurrent threshold configuration channel 2

An overcurrent event can be simulated using SOVCx. If SOVCx = 1, the corresponding overcurrent error bit OVCx will be set to 1, the error will be signaled at NCHx and the corresponding laser channel will be disabled. The overcurrent error will remain forced until SOVCx = 0.

| SOVC1 |  | Addr. 0x1D; bit 5 | R/W 0 |
|-------|--|-------------------|-------|
| Code  | Function                                       |                   |       |
| 0     | No Overcurrent event at channel 1 is simulated |                   |       |
| 1     | Overcurrent event at channel 1 simulated       |                   |       |

Table 22: Simulate overcurrent channel 1

| SOVC2 |  | Addr. 0x1D; bit 6 | R/W 0 |
|-------|--|-------------------|-------|
| Code  | Function                                       |                   |       |
| 0     | No overcurrent event at channel 2 is simulated |                   |       |
| 1     | Overcurrent event at channel 2 simulated       |                   |       |

Table 23: Simulate overcurrent channel 2

In APC mode the laser current can be measured setting register ADCCx(2:0) to 0x100 and the register bit CMESx to 1. See chapter 10 bit Linear A/D converter on page 29 for more information.

### ACC mode

In this mode, the laser diode current is controlled and no monitor diode is required. ACC mode is selected setting EACCx register bit to 1. Figure 8 shows an example of this configuration.

| EACC1 |   | Addr. 0x10; bit 0 | R/W 0 |
|-------|---|-------------------|-------|
| Code  | Function  |                   |       |
| 0     | APC mode enabled for channel 1 (light power regulation)   |                   |       |
| 1     | ACC mode enabled for channel 1 (laser current regulation) |                   |       |

Table 24: Enable APC/ACC channel 1

| <b>EACC2</b> |   | Addr. 0x15; bit 0 | R/W 0 |
|--------------|---|-------------------|-------|
| Code         | Function  |                   |       |
| 0            | APC mode enabled for channel 2 (light power regulation)   |                   |       |
| 1            | ACC mode enabled for channel 2 (laser current regulation) |                   |       |

Table 25: Enable APC/ACC channel 2

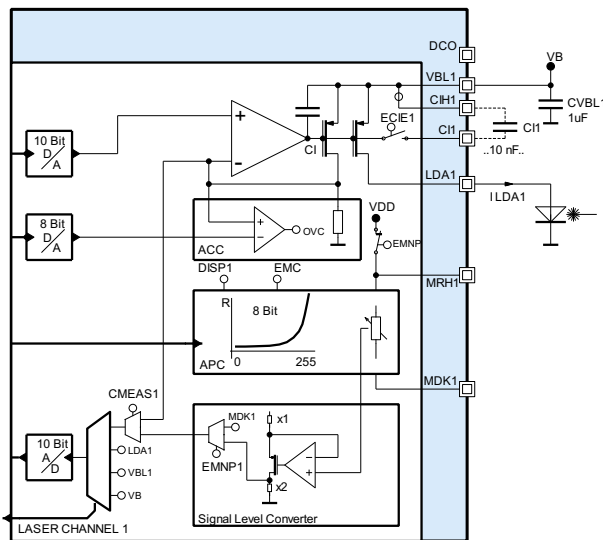


Figure 8: ACC mode simplified

In ACC mode an internal resistor (RACCx) is used instead of the internal programmable logarithmic monitor resistor (PLR). Different current ranges can be selected though register bits RACCx and CRNGx(1:0).

| <b>RACC1</b> |   | Addr. 0x1A; bit 0 | R/W 0 |
|--------------|---|-------------------|-------|
| Code         | Function  |                   |       |
| 0            | Current range high for channel 1, Current sensor resistor (Rsensex) set to 2 kΩ |                   |       |
| 1            | Current range low for channel 1, Current sensor resistor (Rsensex) set to 16 kΩ |                   |       |

Table 26: Current range configuration channel 1

| <b>RACC2</b> |   | Addr. 0x1A; bit 4 | R/W 0 |
|--------------|---|-------------------|-------|
| Code         | Function  |                   |       |
| 0            | Current range high for channel 2, Current sensor resistor (Rsensex) set to 2 kΩ |                   |       |
| 1            | Current range low for channel 2, Current sensor resistor (Rsensex) set to 16 kΩ |                   |       |

Table 27: Current range configuration channel 2

| <b>CRNG1(1:0)</b> |  | Addr. 0x1E; bit 1:0 | R/W 00 |
|-------------------|--|---------------------|--------|
| Code              | Function   |                     |        |
| 00                | Output current range from 0 to 750 mA, RACC1 = 0, k factor set to 750/750 = 1    |                     |        |
| 01                | Output current range from 0 to 100 mA, RACC1 = 0, k factor set to 100/750 = 0.13 |                     |        |
| 10                | Output current range from 0 to 25 mA, RACC1 = 0, k factor set to 25/750 = 0.03   |                     |        |
| 11                | Output current range from 0 to 9 mA, RACC1 = 0, k factor set to 9/750 = 0.012    |                     |        |
| 00                | Output current range from 0 to 90 mA, RACC1 = 1, k factor set to 750/750 = 1     |                     |        |
| 01                | Output current range from 0 to 12 mA, RACC1 = 1, k factor set to 100/750 = 0.13  |                     |        |
| 10                | Output current range from 0 to 3 mA, RACC1 = 1, k factor set to 25/750 = 0.03    |                     |        |
| 11                | Output current range from 0 to 1.1 mA, RACC1 = 1, k factor set to 9/750 = 0.012  |                     |        |

Table 28: Current range channel 1

| <b>CRNG2(1:0)</b> |  | Addr. 0x1E; bit 5:4 | R/W 00 |
|-------------------|--|---------------------|--------|
| Code              | Function   |                     |        |
| 00                | Output current range from 0 to 750 mA, RACC2 = 0, k factor set to 750/750 = 1    |                     |        |
| 01                | Output current range from 0 to 100 mA, RACC2 = 0, k factor set to 100/750 = 0.13 |                     |        |
| 10                | Output current range from 0 to 25 mA, RACC2 = 0, k factor set to 25/750 = 0.03   |                     |        |
| 11                | Output current range from 0 to 9 mA, RACC2 = 0, k factor set to 9/750 = 0.012    |                     |        |
| 00                | Output current range from 0 to 90 mA, RACC2 = 1, k factor set to 750/750 = 1     |                     |        |
| 01                | Output current range from 0 to 12 mA, RACC2 = 1, k factor set to 100/750 = 0.13  |                     |        |
| 10                | Output current range from 0 to 3 mA, RACC2 = 1, k factor set to 25/750 = 0.03    |                     |        |
| 11                | Output current range from 0 to 1.1 mA, RACC2 = 1, k factor set to 9/750 = 0.012  |                     |        |

Table 29: Current range channel 2

Table 30 shows a list with all selectable current ranges.

| <b>ACC current ranges</b> |       |          |
|---------------------------|-------|----------|
| CRNGx(1:0)                | RACCx | Idc(LDA) |
| 00                        | 0     | 750 mA   |
| 01                        | 0     | 100 mA   |
| 00                        | 1     | 90 mA    |
| 10                        | 0     | 25 mA    |
| 01                        | 1     | 12 mA    |
| 11                        | 0     | 9 mA     |
| 10                        | 1     | 3 mA     |
| 11                        | 1     | 1.1 mA   |

Table 30: ACC current ranges



For fine-tuning the regulated current, the reference voltage can be set with a 10 bit logarithmic D/A converter, which is configurable through the register REFx. This converter has a voltage range that goes typically from 0.1 to 1.1 V, allowing an operation resolution of typically 0.235%. Optionally the reference voltage D/A converter can be configured as a linear one with the same voltage range. Linear or logarithmic D/A reference voltage can be set with register bit LINLOGx.

A programmable overcurrent threshold is available in order to protect the laser diode during the power-on. The overcurrent protection value,  $I_{lim}$ , must be configured in the 8 bit register ILIMx using the following equations:

$$I_{lim} = (\Delta I(LDA)_{max}) * n * k$$

$$n = \frac{I_{lim}}{k * \Delta I(LDA)_{max}}$$

with n from 0 to 255.

If ILIM is set to 0 in ACC mode, the overcurrent protection is disconnected. Overcurrent protection is disabled when using the linear reference D/A setting register bit LINLOGx.

Note: The accuracy of the overcurrent detection depends on the correct biasing of the driver stage. If the driver is saturated, the accuracy of the overcurrent detection is reduced and may not work as expected. Saturation voltage (*Electrical Characteristics No. 101*) must be ensured for a proper function of the overcurrent detection. LDASAT1 and LDASAT2 status bits can be used for anticipated saturation detection.

$\Delta I(LDA)_{max}$  is the shutdown current threshold resolution (maximum value) (cf. *Electrical Characteristics No. 108*). Its value depends on the current range defined by register bit RACCx. If RACCx = 1, the overcurrent threshold is in the low range and  $\Delta I(LDA)_{max} = 0.375$  mA. If RACCx = 0, the overcurrent threshold is in the high range and  $\Delta I(LDA)_{max} = 3$  mA. k is a current range factor, with a value depending on the CRNGx(1:0) register.

| ILIM1 |   | Addr. 0x11; bit 7:0 | R/W 0xFF |
|-------|---|---------------------|----------|
| Code  | Function  |                     |          |
| 0x00  | Channel 1 overcurrent threshold set to the minimum current in APC mode (EACC1 = 0) or overcurrent protection disabled in ACC mode (EACC1 = 1) |                     |          |
| ...   | Channel 1 overcurrent threshold set to $I_{lim} = (\Delta I(LDA)_{max}) * n * k$ , n from 0 to 255  |                     |          |
| 0xFF  | Channel 1 overcurrent threshold set to the maximum current  |                     |          |

Table 31: Overcurrent threshold configuration channel 1

| ILIM2 |   | Addr. 0x16; bit 7:0 | R/W 0xFF |
|-------|---|---------------------|----------|
| Code  | Function  |                     |          |
| 0x00  | Channel 2 overcurrent threshold set to the minimum current in APC mode (EACC2 = 0) or overcurrent protection disabled in ACC mode (EACC2 = 1) |                     |          |
| ...   | Channel 2 overcurrent threshold set to $I_{lim} = (\Delta I(LDA)_{max}) * n * k$ , n from 0 to 255  |                     |          |
| 0xFF  | Channel 2 overcurrent threshold set to the maximum current  |                     |          |

Table 32: Overcurrent threshold configuration channel 2

An overcurrent event can be simulated using bit SOVCx. If SOVCx = 1, the corresponding overcurrent error bit OVCx will be set to 1, the error will be signaled through NCHK and the corresponding laser channel will be disabled. The overcurrent error will remain forced until SOVCx = 0.

| SOVC1 |  | Addr. 0x1D; bit 5 | R/W 0 |
|-------|--|-------------------|-------|
| Code  | Function                                       |                   |       |
| 0     | No Overcurrent event at channel 1 is simulated |                   |       |
| 1     | Overcurrent event at channel 1 simulated       |                   |       |

Table 33: Simulate overcurrent channel 1

| SOVC2 |  | Addr. 0x1D; bit 6 | R/W 0 |
|-------|--|-------------------|-------|
| Code  | Function                                       |                   |       |
| 0     | No overcurrent event at channel 2 is simulated |                   |       |
| 1     | Overcurrent event at channel 2 simulated       |                   |       |

Table 34: Simulate overcurrent channel 2

### Calculating the expected output current in ACC mode

The following formula can be used to estimate the expected current value for an ACC configuration. The resulting value is a typical value.

$$I_{lasertyp} = \frac{V_{refx}}{R_{sensex}} * MFACTx$$

Where

$$V_{refx} = V_{ref0} (1 + \frac{\Delta V_{ref}(\%)}{100})^{n+1}, n \text{ from } 0 \text{ to } 1023$$

$V_{ref0}$  is the minimum value (typically 0.1 V),  $\Delta V_{ref}(\%)$  is the step value (typically 0.235 %) and n is the value of REFx register in decimal.

Rsensex is 2 k $\Omega$  when RACCx = 0 or 16 k $\Omega$  when RACCx = 1.

MFACTx depends on several parameters as stated in the following table:

| ACC mirror factor |       |                           |
|-------------------|-------|---------------------------|
| MERGE             | CRNGx | Mirror factor             |
| 0                 | 00    | Mirror Factor set to 2500 |
| 0                 | 01    | Mirror Factor set to 333  |
| 0                 | 10    | Mirror Factor set to 83   |
| 0                 | 11    | Mirror Factor set to 30   |
| 1                 | 00    | Mirror Factor set to 5000 |
| 1                 | 01    | Mirror Factor set to 666  |
| 1                 | 10    | Mirror Factor set to 166  |
| 1                 | 11    | Mirror Factor set to 60   |

Table 35: Mirror factor

Table 36 shows some typical current settings. For detailed limits, please refer to *Electrical Characteristics No. 114*.

| ACC typical current settings |       |           |           |
|------------------------------|-------|-----------|-----------|
| CRNG(1:0)                    | REFx  | RACCx=0   | RACCx=1   |
| 00                           | 0x000 | 125.3 mA  | 15.66 mA  |
| 00                           | 0x001 | 125.6 mA  | 15.70 mA  |
| 00                           | 0x010 | 125.9 mA  | 15.73 mA  |
| ...                          | ...   | ...       | ...       |
| 00                           | 0x200 | 416.6 mA  | 52.08 mA  |
| 00                           | 0x201 | 417.6 mA  | 52.20 mA  |
| 00                           | 0x202 | 418.6 mA  | 52.33 mA  |
| ...                          | ...   | ...       | ...       |
| 00                           | 0x3FD | 1376.1 mA | 172.01 mA |
| 00                           | 0x3FE | 1379.3 mA | 172.41 mA |
| 00                           | 0x3FF | 1382.6 mA | 172.82 mA |

Table 36: ACC typical current settings

In ACC mode, the MDKx pin can be monitored through a 10 bit A/D converter from 0 up to 1.1 V. This can be used for measuring the laser light power, if a photodiode is connected to pin MDKx, as shown in Figure 9. This allows adjusting the voltage reference in order to set the laser current and obtain the desired laser light power.

The internal programmable logarithmic monitor resistor (PLR), if enabled (DISPx = 0), gives feedback for the current control through the 10 bit A/D converter. Register bit ADFNSx must be set to 0 in order to measure the internal sense node, after the x2 level shifting. An external monitor resistor can be used to measure the optical power by setting DISPx to 1. Therefore register bit ADFNSx must be set to 1 in order to measure directly at pin MDKx.

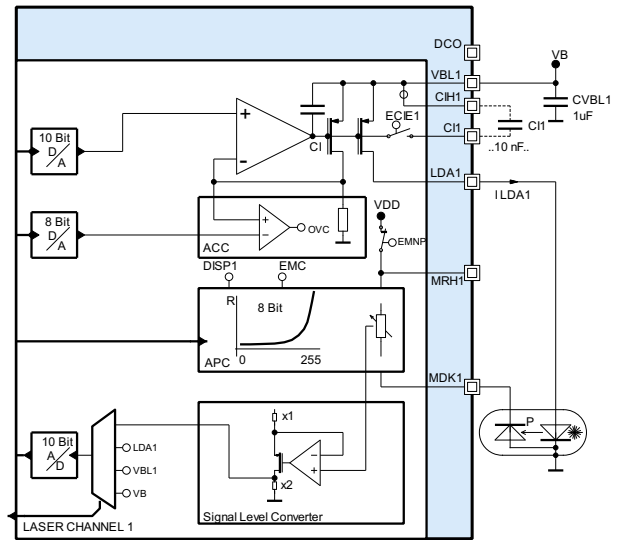


Figure 9: ACC with monitor photodiode

ACC mode permits combining both channels in one iC-HTP (see chapter COMBINING BOTH CHANNELS) and several iC-HTP in parallel. When both channels are combined the programmable overcurrent shutdown is carried out per each channel. If both channels are configured in ACC mode, LDA1 and LDA2 can be connected together. Each channel can be configured with a different current range, yielding different granularity in steps regulation for each channel.

### The Regulator

In MCU mode the control can be carried out without the need of external capacitor. This allows a fast response of the regulator. The speed of the regulator's response and stability can be configured using three bits (COMPx), providing a current compensation factor.

| COMP1 |   | Addr. 0x13; bit 6:4 | R/W 011 |
|-------|---|---------------------|---------|
| Code  | Function  |                     |         |
| 000   | Minimum compensation current for the channel 1 regulator, slower response |                     |         |
| ...   |   |                     |         |
| 111   | Maximum compensation current for the channel 1 regulator, faster response |                     |         |

Table 37: Current compensation channel 1

| COMP2 |   | Addr. 0x18; bit 6:4 | R/W 011 |
|-------|---|---------------------|---------|
| Code  | Function  |                     |         |
| 000   | Minimum compensation current for the channel 2 regulator, slower response |                     |         |
| ...   |   |                     |         |
| 111   | Maximum compensation current for the channel 2 regulator, faster response |                     |         |

Table 38: Current compensation channel 2

Alternatively it is possible to use external capacitors connected to pins Clx and CIHx. In this case, register bit ECIE<sub>x</sub> should be set to 1 and COMP<sub>x</sub> to its highest value, "111".

| ECIE1 |  | Addr. 0x10; bit 1 | R/W 0 |
|-------|--|-------------------|-------|
| Code  | Function   |                   |       |
| 0     | External CI capacitor for channel 1 disconnected |                   |       |
| 1     | External CI capacitor for channel 1 connected    |                   |       |

Table 39: Enable external CI capacitor channel 1

| ECIE2 |  | Addr. 0x15; bit 1 | R/W 0 |
|-------|--|-------------------|-------|
| Code  | Function   |                   |       |
| 0     | External CI capacitor for channel 2 disconnected |                   |       |
| 1     | External CI capacitor for channel 2 connected    |                   |       |

Table 40: Enable external CI capacitor channel 2

The regulator is offset compensated in order to prevent optical power drifts.

An internal oscillator is used for the offset compensation. A watchdog timer (WDT) is included in order to monitor proper function of the oscillator. If an error is detected by the WDT, the laser channels are operated with an offset to ensure a safe power level, OSCERR error bit is set in STATUS0 register and the error event is signaled at pin NCHK. This error signaling can be suppressed using the mask register bit MOSCERR (set to 1).

| MOSCERR |  | Addr. 0x1D; bit 0 | R/W 0 |
|---------|--|-------------------|-------|
| Code    | Function   |                   |       |
| 0       | Oscillator error (watchdog) will be signaled at NCHK     |                   |       |
| 1       | Oscillator error (watchdog) will not be signaled at NCHK |                   |       |

Table 41: Oscillator watchdog error mask

iC-HTP monitors the saturation voltage of the regulator's output transistor at pin LD<sub>Ax</sub>. The LDA saturation threshold can be configured through register bits RL<sub>DASx</sub>.

| RLDAS1 |   | Addr. 0x13; bit 3:2 | R/W 00 |
|--------|---|---------------------|--------|
| Code   | Function  |                     |        |
| 00     | V(LDA1) > VBL1-0.5 V sets the LDASAT1 alarm bit |                     |        |
| 01     | V(LDA1) > VBL1-0.8 V sets the LDASAT1 alarm bit |                     |        |
| 10     | V(LDA1) > VBL1-1.0 V sets the LDASAT1 alarm bit |                     |        |
| 11     | V(LDA1) > VBL1-1.2 V sets the LDASAT1 alarm bit |                     |        |

Table 42: LDA saturation threshold selection channel 1

| RLDAS2 |   | Addr. 0x18; bit 3:2 | R/W 00 |
|--------|---|---------------------|--------|
| Code   | Function  |                     |        |
| 00     | V(LDA2) > VBL2-0.5 V sets the LDASAT2 alarm bit |                     |        |
| 01     | V(LDA2) > VBL2-0.8 V sets the LDASAT2 alarm bit |                     |        |
| 10     | V(LDA2) > VBL2-1.0 V sets the LDASAT2 alarm bit |                     |        |
| 11     | V(LDA2) > VBL2-1.2 V sets the LDASAT2 alarm bit |                     |        |

Table 43: LDA saturation threshold selection channel 2

If the LD<sub>Ax</sub> voltage goes higher than the LDA saturation threshold the LDASAT<sub>x</sub> error bit in STATUS1 register will be set and it will be signaled through output pin NCHK. Setting the mask register bit ML<sub>DASATx</sub> to 1 suppresses the signaling at NCHK.

| MLDASAT1 |  | Addr. 0x1D; bit 2 | R/W 1 |
|----------|--|-------------------|-------|
| Code     | Function                                   |                   |       |
| 0        | LDASAT1 event will be signaled at NCHK     |                   |       |
| 1        | LDASAT1 event will not be signaled at NCHK |                   |       |

Table 44: LDA saturation error mask channel 1

| MLDASAT2 |  | Addr. 0x1D; bit 3 | R/W 1 |
|----------|--|-------------------|-------|
| Code     | Function                                   |                   |       |
| 0        | LDASAT2 event will be signaled at NCHK     |                   |       |
| 1        | LDASAT2 event will not be signaled at NCHK |                   |       |

Table 45: LDA saturation error mask channel 2

### Laser channel enabling and error handling

With pin INS/WKR or EMC unconnected, a corresponding error signal will be generated (INSOPEN, EMCOPEN). Any of these error signals will disable the laser channels.

Setting DISC1 and DISC2 to 1 (default) disables the corresponding channel.

The errors in STATUS0 and STATUS1 registers disable the laser channels. Every change in the STATUS registers is signaled at pin NCHK, unless the error event is masked by the corresponding error mask bit.

| Register | Address | Bits | Default | Description   |
|----------|---------|------|---------|---|
| INITRAM  | 0x00    | 0    | R/O     | RAM initialized   |
| PDOVDD   | 0x00    | 1    | R/O     | Power down at VDD   |
| MEMERR   | 0x00    | 2    | R/O     | RAM memory validation error   |
| OVT      | 0x00    | 3    | R/O     | Overtemperature   |
| OVC2     | 0x00    | 4    | R/O     | Overcurrent at channel 2  |
| OVC1     | 0x00    | 5    | R/O     | Overcurrent at channel 1  |
| OSCERR   | 0x00    | 6    | R/O     | Oscillator error (watchdog set)                                       |
| CFGTIMO  | 0x00    | 7    | R/O     | Configuration mode timeout  |
| MAPC1    | 0x01    | 0    | R/O     | Channel 1 current state   |
| MONC1    | 0x01    | 1    | R/O     | Monitor channel 1 enabled at least once (latched)                     |
| LDASAT1  | 0x01    | 2    | R/O     | Channel 1 LDA saturation  |
| PDOVBL1  | 0x01    | 3    | R/O     | Power down at VBL1 or Power down in any of VBL1 or VBL2 in merge mode |
| MAPC2    | 0x01    | 4    | R/O     | Channel 2 current state   |
| MONC2    | 0x01    | 5    | R/O     | Monitor channel 2 enabled at least once (latched)                     |
| LDASAT2  | 0x01    | 6    | R/O     | Channel 2 LDA saturation  |
| PDOVBL2  | 0x01    | 7    | R/O     | Power down at VBL2 or VBL1 not equal to VBL2 in merge mode            |

Table 46: Status registers overview

In order to enable the channels, the error events must be acknowledged. Acknowledging an error is accomplished by reading the STATUS register. After a power-on PDOVDD, PDOVBL1, PDOVBL2 and INITRAM errors will be set, therefore it is required to read STATUS0 and STATUS1 registers after each power-on.

Exiting standby mode will not reset the RAM but will set the PDOVDD status bit. Therefore STATUS0 must

be read once after each standby to re-enable the laser channels.

In case of an overcurrent (OVC) or an overtemperature (OVT), the laser outputs are disabled.

A memory error and a configuration timeout error will also disable the laser outputs. The conditions to enable each laser output are shown in Figure 10.

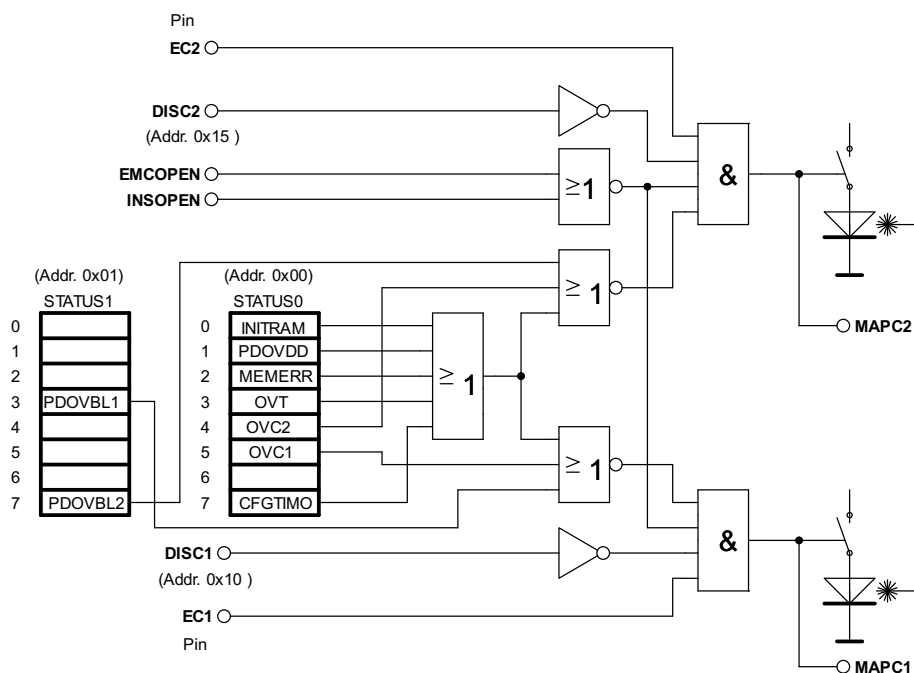


Figure 10: Laser control logic in MCU mode

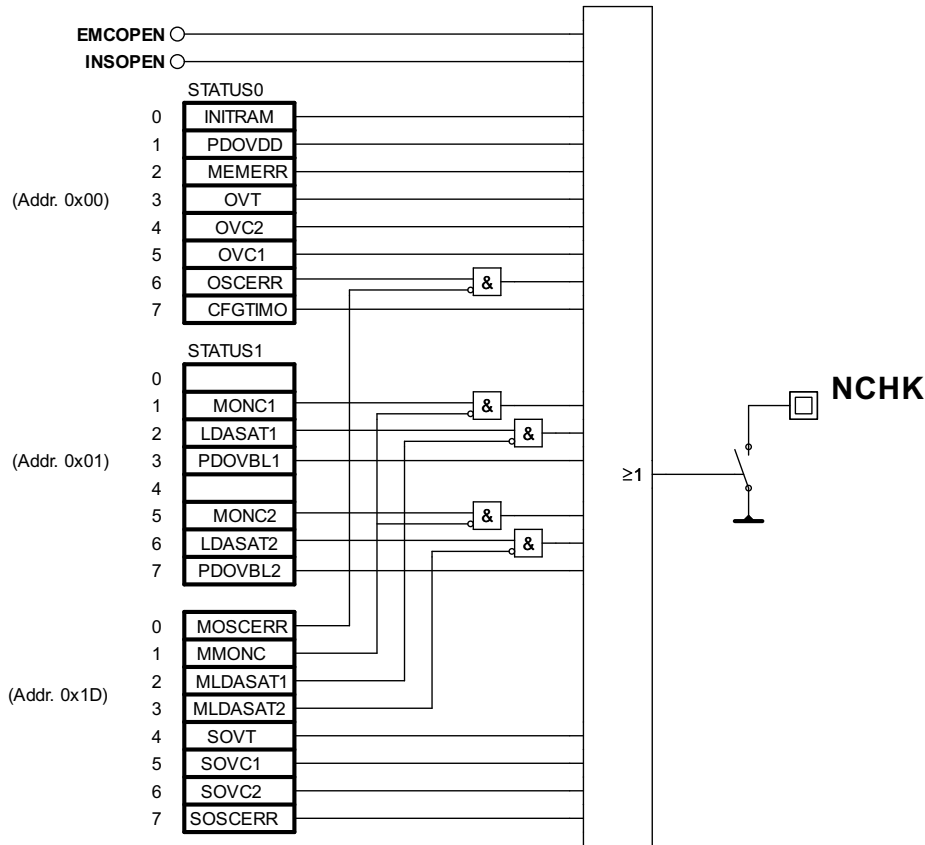


Figure 11: NCHK behavior in MCU mode

### PULSED MODE

The Pulsed Mode is a particular mode of microcontroller mode. It is enabled with EPULx and in this mode it is strongly recommended to use an external CI capacitor.

|              |                       |       |
|--------------|-----------------------|-------|
| <b>EPUL1</b> | Addr. 0x13; bit bit 7 | R/W 0 |
| <b>EPUL2</b> | Addr. 0x18; bit bit 7 | R/W 0 |
| Code         | Function              |       |
| 0            | Pulsed mode disabled  |       |
| 1            | Pulsed Mode enabled   |       |

Table 47: Enable Pulse Mode

The iC-HTP can be pulsed up to 300 kHz. In Pulsed Mode the laser current can be enabled and disabled using the pin ECx, while the regulator keeps its operation point stored in the CI capacitor.

Working in APC mode the average value of light is regulated. If the laser is switched off for a long period of time

the regulator tends to increase the set point of the current. To avoid laser damages a timeout is implemented in APC mode and the regulation will be automatically disconnected. The minimum pulse frequency in APC mode is 2 kHz.

Working in ACC mode no time out is implemented and the laser can be pulsed with frequencies from CW up to 300 kHz.

If a long laser pulse pause is required in APC mode (burst pulses), the current at the laser can be measured while the laser is on (see 10 bit linear A/D converter on page 29), and the ACC mode can be set during the laser-off period, thus avoiding the regulator to loose its operation point. The timeout duration (min. 300  $\mu$ s) allows the activation of the ACC mode after switching the laser off without interruption of the regulation. The procedure is described on figure 12, 13 and 14.

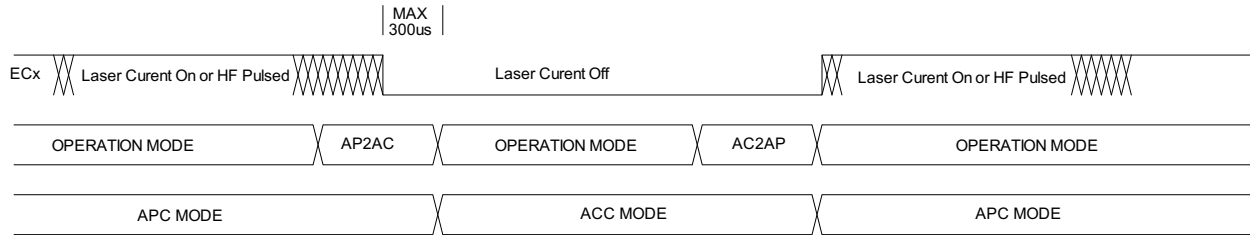


Figure 12: Working in APC with long pause

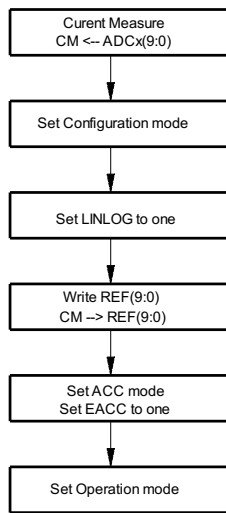


Figure 13: AP2AC procedure

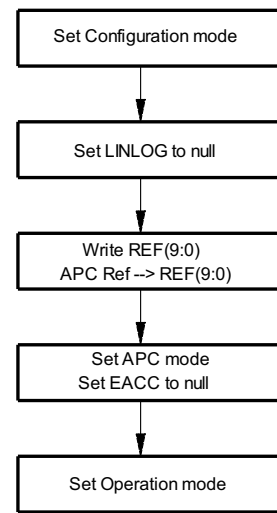


Figure 14: AC2AP procedure

Pulsed mode affects the overcurrent detection:

| Overcurrent in Pulsed Mode |       |            |                 |
|----------------------------|-------|------------|-----------------|
| EPULx                      | EACCx | ILIMx(7:0) | OVC             |
| 1                          | 0     | 0x00       | Disabled        |
| 1                          | 1     | –          | Disabled        |
| 1                          | 0     | > 0x00     | Normal function |

Table 48: Overcurrent detection in Pulsed Mode

Note: Overcurrent is also disabled when using the linear reference D/A setting register bit LINLOGx.

### COMBINING BOTH CHANNELS

iC-HTP can drive one laser diode with up to 1500 mA and both channels combined. Therefore register bit MERGE must be set to 1. Disable channel register bits DISC1 and DISC2 must both be set to 0 and both enable channel pins EC1 and EC2 must be set hi.

| MERGE | Addr. 0x1B; bit 6   | R/W 0 |
|-------|---|-------|
| Code  | Function  |       |
| 0     | Channel 1 and 2 operate independently   |       |
| 1     | Power transistor from channel 2 usable in parallel with channel 1, regulation made by channel 1 |       |

Table 49: Channel combination

Different current ranges can be configured using CRNG1 and CRNG2. The resulting range is the addition of both configured ranges.

| CRNG1(1:0) |   | Addr. 0x1E; bit 1:0 | R/W 00 |
|------------|---|---------------------|--------|
| Code       | Function  |                     |        |
| 00         | Output current range from 0 to 750 mA, RACC1 = 0, k factor set to 750/750 = 1     |                     |        |
| 01         | Output current range from 0 to 100 mA, RACC1 = 0, k factor set to 100/750, = 0.13 |                     |        |
| 10         | Output current range from 0 to 25 mA, RACC1 = 0, k factor set to 25/750 = 0.03    |                     |        |
| 11         | Output current range from 0 to 9 mA, RACC1 = 0, k factor set to 9/750 = 0.012     |                     |        |
| 00         | Output current range from 0 to 90 mA, RACC1 = 1, k factor set to 750/750 = 1      |                     |        |
| 01         | Output current range from 0 to 12 mA, RACC1 = 1, k factor set to 100/750 = 0.13   |                     |        |
| 10         | Output current range from 0 to 3 mA, RACC1 = 1, k factor set to 25/750 = 0.03     |                     |        |
| 11         | Output current range from 0 to 1.1 mA, RACC1 = 1, k factor set to 9/750 = 0.012   |                     |        |

Table 50: Current range channel 1

| CRNG2(1:0) |   | Addr. 0x1E; bit 5:4 | R/W 00 |
|------------|---|---------------------|--------|
| Code       | Function  |                     |        |
| 00         | Output current range from 0 to 750 mA, RACC2 = 0, k factor set to 750/750 = 1     |                     |        |
| 01         | Output current range from 0 to 100 mA, RACC2 = 0, k factor set to 100/750, = 0.13 |                     |        |
| 10         | Output current range from 0 to 25 mA, RACC2 = 0, k factor set to 25/750 = 0.03    |                     |        |
| 11         | Output current range from 0 to 9 mA, RACC2 = 0, k factor set to 9/750 = 0.012     |                     |        |
| 00         | Output current range from 0 to 90 mA, RACC2 = 1, k factor set to 750/750 = 1      |                     |        |
| 01         | Output current range from 0 to 12 mA, RACC2 = 1, k factor set to 100/750 = 0.13   |                     |        |
| 10         | Output current range from 0 to 3 mA, RACC2 = 1, k factor set to 25/750 = 0.03     |                     |        |
| 11         | Output current range from 0 to 1.1 mA, RACC2 = 1, k factor set to 9/750 = 0.012   |                     |        |

Table 51: Current range channel 2

In ACC mode, only RACC1 modifies the current range and for both channels the same.

When both channels are combined the control is done by channel 1. APC and ACC can both be used with both channels combined.

| Current ranges in merge mode for ACC |       |       |               |
|--------------------------------------|-------|-------|---------------|
| RACC1                                | CRNG1 | CRNG2 | Current range |
| 0                                    | 00    | 00    | 1500 mA       |
| 0                                    | 00    | 01    | 850 mA        |
| 0                                    | 00    | 10    | 775 mA        |
| 0                                    | 00    | 11    | 759 mA        |
| 0                                    | 01    | 00    | 850 mA        |
| ...                                  | ...   | ...   | ...           |
| 1                                    | 00    | 00    | 180 mA        |
| 1                                    | 00    | 01    | 102 mA        |
| 1                                    | 00    | 10    | 93 mA         |
| 1                                    | 00    | 11    | 91.1 mA       |
| 1                                    | 01    | 00    | 102 mA        |
| ...                                  | ...   | ...   | ...           |

Table 52: Merge mode current ranges

In ACC mode, the reference needs to be configured according to the selected current range (if both CRNG1 and CRNG2 are the same, set to 50% of the equivalent value for a single channel operation). This is not required for APC.

Both VBL1 and VBL2 must be connected to the same voltage level. If voltages at VBL1 and VBL2 are different, PODOVBL2 bit in status register will be set and laser will be shut down. In merge mode, the PODOVBL1 bit is used to monitor both VBL1 and VBL2 voltages for power down. If any of the VBL1 or VBL2 are in power down, this bit will be set.

| PDOVBL1 |   | Addr. 0x01; bit 3 | R |
|---------|---|-------------------|---|
| Code    | Function  |                   |   |
| 0       | VBL1 power down not occurred since last read. If MERGE = 1, VBL1 and VBL2 had no power down since last read |                   |   |
| 1       | VBL1 power down event has occurred. If MERGE = 1, VBL1 or VBL2 had a power down event. Cleared on read      |                   |   |

Table 53: VBL1 power down

| PDOVBL2 |   | Addr. 0x01; bit 7 | R |
|---------|---|-------------------|---|
| Code    | Function  |                   |   |
| 0       | VBL2 power down not occurred since last read. If MERGE = 1, VBL1 voltage level equals VBL2 voltage level            |                   |   |
| 1       | VBL2 power down event has occurred. If MERGE = 1, VBL1 voltage level not equals VBL2 voltage level. Cleared on read |                   |   |

Table 54: VBL2 power down

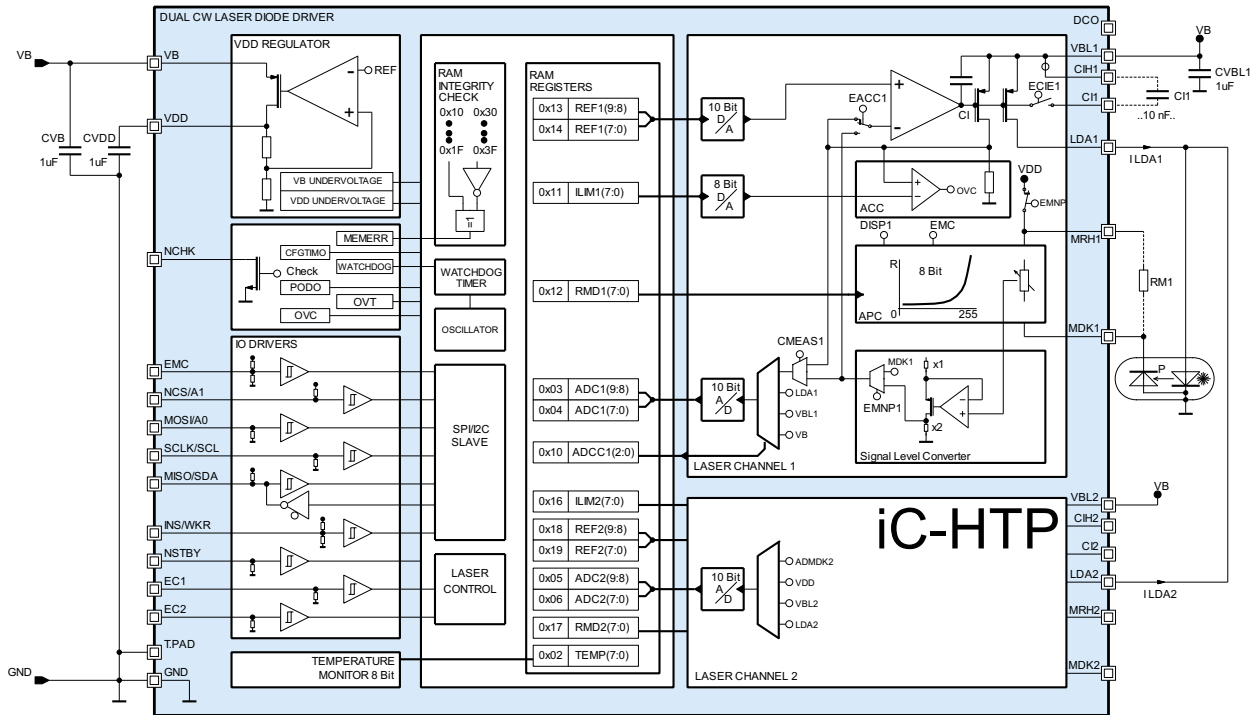


Figure 15: Combining both channels

In combined mode, the internal CI nodes of both channels are connected together. If required, an external capacitor on channel 1 can be used for improved stability. It is possible to have an additional external capacitor on channel 2 if ECIE2 bit is set to 1. Having an external capacitor on channel 2 and none on channel 1 is invalid.

On combined operation both overcurrent thresholds are active. The overcurrent threshold channel 1, ILIM1, needs to be set accordingly to the selected current range as stated below. If both CRNG1 and CRNG2 are the same, set to 50% of the equivalent value for a single channel operation.

$$Ilim(merge) = (\Delta I(LDA), max) \cdot n \cdot (k1 + k2)$$

Where k1 depends on CRNG1 and k2 depends on CRNG2.

$$n = \frac{Ilim(merge)}{(k1 + k2) \cdot \Delta I(LDA), max}$$

with n from 1 to 255.

The overcurrent threshold channel 2, ILIM2, must be set to its maximum or disabled with any of the following procedures:

**ACC mode** Setting it to its maximum value (0xFF) or setting it to its minimum value (0x00) (disconnected)

**APC mode** Setting it to its maximum value (0xFF)

| ILIM1 | Addr. 0x11; bit 7:0   | R/W 0xFF |
|-------|---|----------|
| Code  | Function  |          |
| 0x00  | Channel 1 overcurrent threshold set to the minimum current in APC mode (EACC1 = 0) or overcurrent protection disabled in ACC mode (EACC1 = 1) |          |
| ...   | Channel 1 overcurrent threshold set to $Ilim = (\Delta I(LDA), max) \cdot n \cdot k$ , n from 0 to 255  |          |
| 0xFF  | Channel 1 overcurrent threshold set to the maximum current  |          |

Table 55: Overcurrent threshold configuration channel 1

| ILIM2 | Addr. 0x16; bit 7:0   | R/W 0xFF |
|-------|---|----------|
| Code  | Function  |          |
| 0x00  | Channel 2 overcurrent threshold set to the minimum current in APC mode (EACC2 = 0) or overcurrent protection disabled in ACC mode (EACC2 = 1) |          |
| ...   | Channel 2 overcurrent threshold set to $Ilim = (\Delta I(LDA), max) \cdot n \cdot k$ , n from 0 to 255  |          |
| 0xFF  | Channel 2 overcurrent threshold set to the maximum current  |          |

Table 56: Overcurrent threshold configuration channel 2

It is possible to use a second photodiode connected to channel 2 (e.g. as a safety supervisor). The ADC on channel 2 can be used to monitor the voltage at pin MDK2, as it is shown in Figure 16.



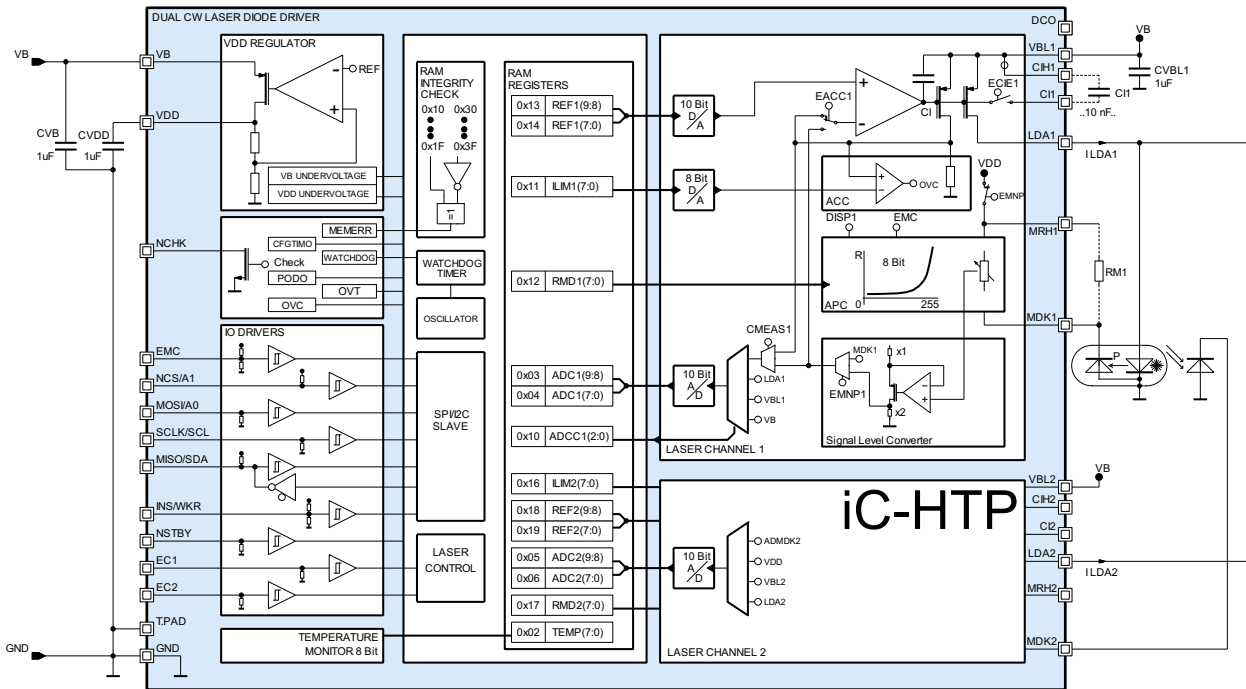


Figure 16: Additional photodiode in combined configuration

### SERIAL COMMUNICATION INTERFACES

#### SPI slave interface

The SPI slave interface is enabled by setting pin **INS/WKR** to **lo** and uses pins **NCS/A1**, **SCLK/SCL**, **MISO/SDA** and **MOSI/A0**. Pin **NCS/A1** is the chip select pin and must be set **lo** by the SPI master in order to start communication. Pins **MISO/SDA** and **MOSI/A0** are the data communication lines and pin **SCLK/SCL** is the clock line generated by the SPI master (e.g. microcontroller). The SPI protocol frames are shown in Figure 17.

A communication frame consists of one address byte and at least one data byte. Bits 7:6 of the address byte is the opcode used for selecting a read operation (set to "10") or a write (set to "01") operation. The remaining 6 bits are used for register addressing.

It is possible to transmit several bytes consecutively, if the **NCS** signal is not reset and **SCLK/SCL** keeps clocking, as shown in Figure 17. The address is internally incremented after each transmitted byte. Once the address reaches the last register (0x3F), it is reset back to 0x00.

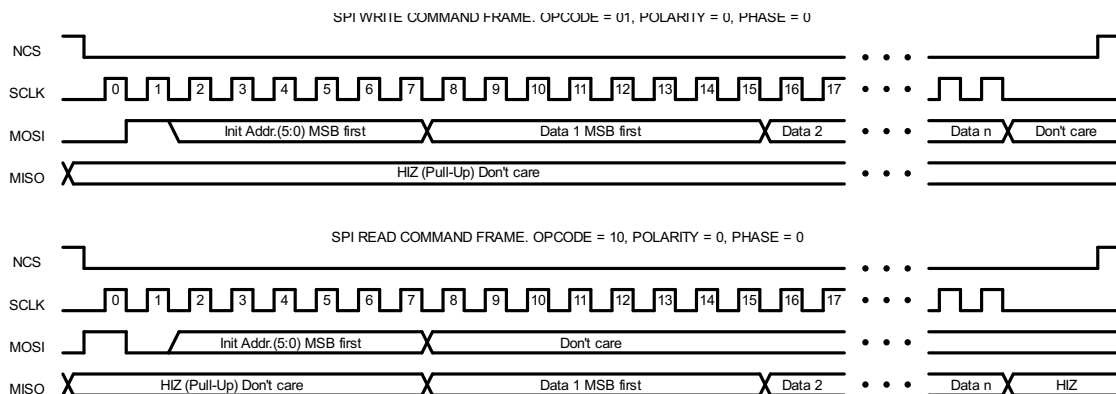


Figure 17: SPI read and write commands

### I<sup>2</sup>C slave interface

The I<sup>2</sup>C slave interface is enabled by setting pin INS/WKR to hi and uses pins NCS/A1, SCLK/SCL, MISO/SDA and MOSI/A0. The protocol frames are shown in Figure 18.

ID consists of 7 bits. The five most significant bits are fixed by default to value 0b10000. Pins MOSI/A0 and NCS/A1 are used to set the remaining slave ID bits (see Table 57 and 58).

| Action          | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|-----------------|----|----|----|----|----|----|----|----|
| Write to slave  | 1  | 0  | 0  | 0  | 0  | A1 | A0 | 0  |
| Read from slave | 1  | 0  | 0  | 0  | 0  | A1 | A0 | 1  |

Table 57: I<sup>2</sup>C write/read byte

A communication frame consists of one slave address byte, one register address byte and at least one data byte. Bits 7:1 of the slave address byte form the slave identification code (ID) and bit 0 is used for specification of the data direction (0 for write, 1 for read). The slave

| Action            | A1 | A0 | Slave ID | Address byte |
|-------------------|----|----|----------|--------------|
| Write to slave 0  | lo | lo | 0x40     | 0x80         |
| Read from slave 0 | lo | lo | 0x40     | 0x81         |
| Write to slave 1  | lo | hi | 0x41     | 0x82         |
| Read from slave 1 | lo | hi | 0x41     | 0x83         |
| Write to slave 2  | hi | lo | 0x42     | 0x84         |
| Read from slave 2 | hi | lo | 0x42     | 0x85         |
| Write to slave 3  | hi | hi | 0x43     | 0x86         |
| Read from slave 3 | hi | hi | 0x43     | 0x87         |

Table 58: I<sup>2</sup>C write/read address

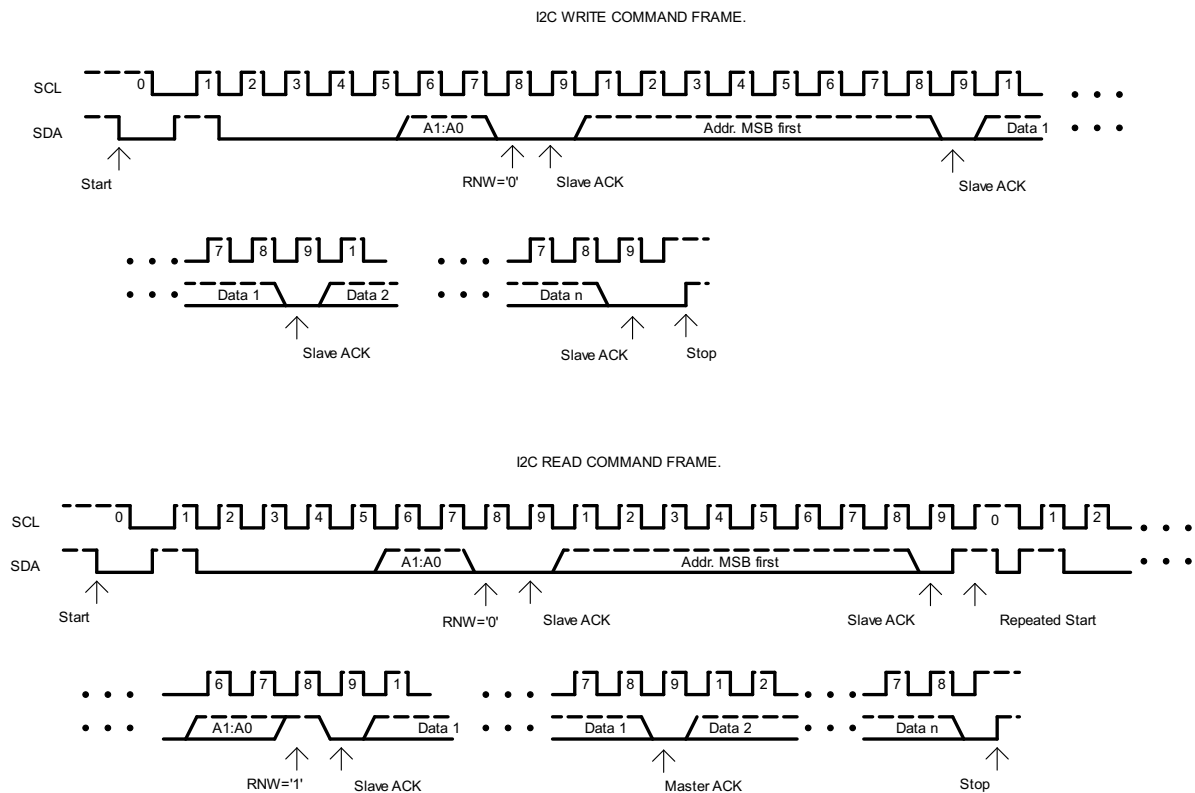


Figure 18: I<sup>2</sup>C read and write commands

### 8 BIT INTERNAL PROGRAMMABLE LOGARITHMIC MONITOR RESISTORS

In MCU mode internal 8 bit programmable logarithmic monitor resistors (PLRx) are provided for APC.

| RMD1 |  | Addr. 0x12; bit 7:0 | R/W 0xFF |
|------|--|---------------------|----------|
| Code | Function   |                     |          |
| 0x00 | PLR1 resistor set to the minimum resistance  |                     |          |
| ...  | PLR1 resistor set to $Rmd = Rmd_0(1 + \frac{\Delta Rmd(\%)}{100})^{n+1}$ , n from 0 to 255 |                     |          |
| 0xFF | PLR1 resistor set to the maximum resistance  |                     |          |

Table 59: MDK resistor channel 1

| RMD2 |  | Addr. 0x17; bit 7:0 | R/W 0xFF |
|------|--|---------------------|----------|
| Code | Function   |                     |          |
| 0x00 | PLR2 resistor set to the minimum resistance  |                     |          |
| ...  | PLR2 resistor set to $Rmd = Rmd_0(1 + \frac{\Delta Rmd(\%)}{100})^{n+1}$ , n from 0 to 255 |                     |          |
| 0xFF | PLR2 resistor set to the maximum resistance  |                     |          |

Table 60: MDK resistor channel 2

The resistor value can be selected from 256 values, ranging from 100 Ω to 407 kΩ, following logarithmic increments with a typical step width of 3.3%. The resistors are configured with registers RMDx(7:0).

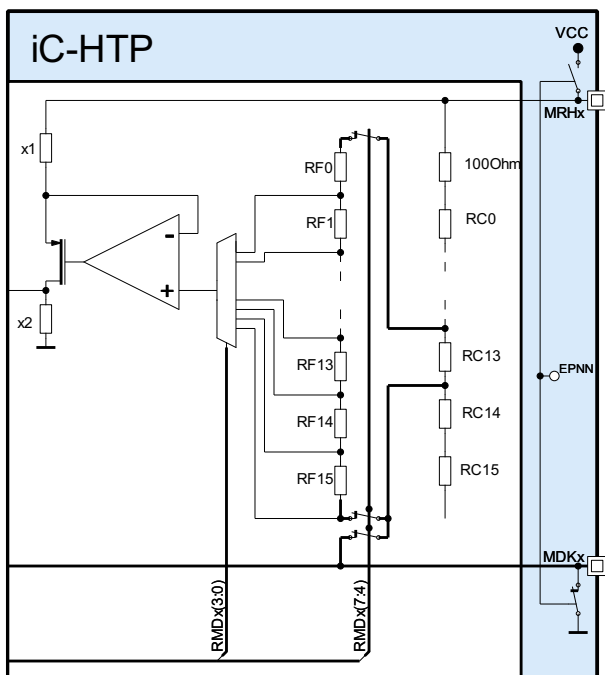


Figure 19: PLR internal node regulation

The following formula calculates the register RMDx in order to set the desired resistor value:

$$Rmd = Rmd_0(1 + \frac{\Delta Rmd(\%)}{100})^{n+1}, n \text{ from } 0 \text{ to } 255$$

Where  $Rmd_0$  is the minimum resistor value (typically 100 Ω),  $\Delta Rmd(\%)$  is the step between two consecutive resistor values (typically 3.3%) and  $n$  is the value of RMDx register in decimal.

In APC mode the regulation node is the internal connection to PLR, it is not the MDAx pin. Voltage present at pin MDKx may differ from the internal regulation node (see details in Figure 19). This regulation node can be sensed through the 10 bit A/D converter and read at register ADCx. Register bit ADFNSx must be set to 0 for this purpose. If ADFNSx is set to 1, MDKx pin will be the input of the A/D converter.

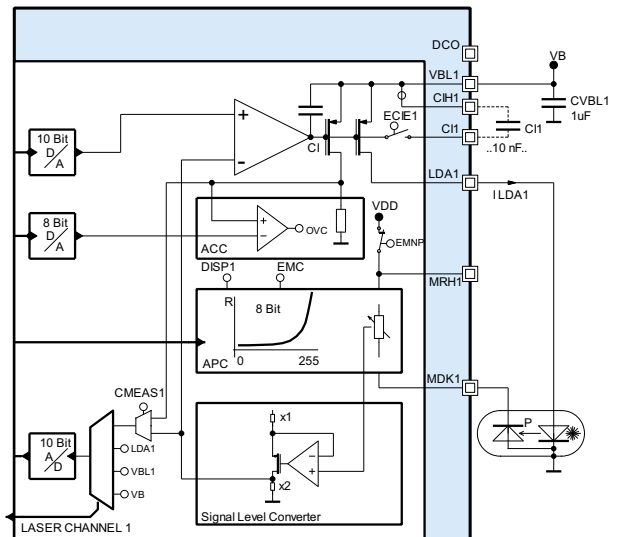


Figure 20: PLR in APC

At pin MDKx only the 4 MSB of the RMDx configuration from PLRx are measurable. The 8 bits of the PLRx configuration RMDx can be measured with the A/D converter setting ADFNSx to 0.

The PLRx can be disabled using register bit DISPx. With DISPx = 0 the PLRx is enabled and DISPx = 1 disables the PLRx.

| DISP1 |                            | Addr. 0x10; bit 2 | R/W 0 |
|-------|----------------------------|-------------------|-------|
| Code  | Function                   |                   |       |
| 0     | PLR enabled for channel 1  |                   |       |
| 1     | PLR disabled for channel 1 |                   |       |

Table 61: Disable PLR channel 1

| DISP2 |                            | Addr. 0x15; bit 2 | R/W 0 |
|-------|----------------------------|-------------------|-------|
| Code  | Function                   |                   |       |
| 0     | PLR enabled for channel 2  |                   |       |
| 1     | PLR disabled for channel 2 |                   |       |

Table 62: Disable PLR channel 2

In ACC mode the PLR is not used in the control circuit. Instead, the internal RACCx resistor is used in the control loop.

Even though the PLR is not in the control circuit, it can be enabled (DISPx = 0) in order to give feedback through the 10 bit A/D converter for the controlling light power if a monitor diode is connected.

Register bit ADFNSx is set to 0 to measure the internal sense node. Alternatively, an external monitor resistor can be used to measure the optical power, by setting DISPx to 1. Then register bit ADFNSx must be set to 1 in order to measure directly at pin MDKx.

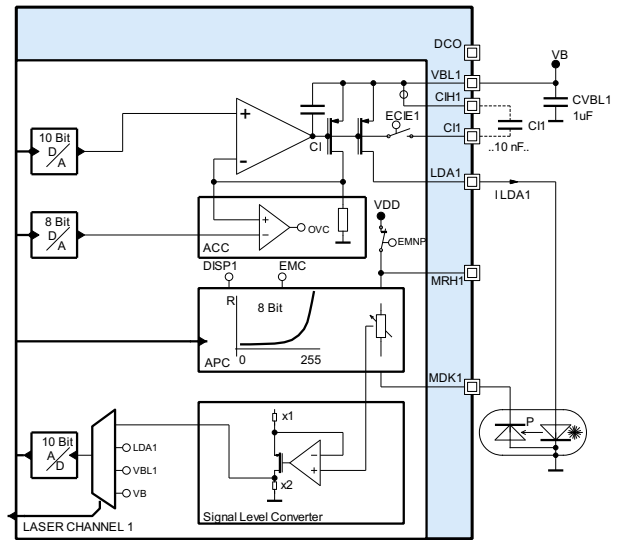


Figure 21: ACC with monitor photodiode

### 10 BIT LOGARITHMIC D/A CONVERTER

The 10 bit logarithmic D/A converter is used for setting the regulator's voltage reference. The D/A converter is active in all operating modes. In iC-WK mode only two values are available: 0.25 V (INS/WKR = lo) and 0.5 V (INS/WKR = hi). In MCU mode both APC and ACC use the D/A converter. With a range from 0.1 to 1.1 V and a typical step width of 0.235%.

| REF1  |  | Addr. 0x13/14; bit 9:0 | R/W 0x000 |
|-------|--|------------------------|-----------|
| Code  | Function   |                        |           |
| 0x000 | Channel 1 regulator reference voltage set to minimum voltage   |                        |           |
| ...   | Channel 1 regulator reference voltage set to $Vref = Vref_0(1 + \frac{\Delta Vref(\%)}{100})^{n+1}$ , n from 0 to 1023 |                        |           |
| 0x3FF | Channel 1 regulator reference voltage set to maximum voltage   |                        |           |

Table 63: Regulator voltage reference channel 1

| REF2  |  | Addr. 0x18/19; bit 9:0 | R/W 0x000 |
|-------|--|------------------------|-----------|
| Code  | Function   |                        |           |
| 0x000 | Channel 2 regulator reference voltage set to minimum voltage   |                        |           |
| ...   | Channel 2 regulator reference voltage set to $Vref = Vref_0(1 + \frac{\Delta Vref(\%)}{100})^{n+1}$ , n from 0 to 1023 |                        |           |
| 0x3FF | Channel 2 regulator reference voltage set to maximum voltage   |                        |           |

Table 64: Regulator voltage reference channel 2

The D/A converter is configured through register REFx(9:0). With REFx(9:0) = 0x000, the D/A output value is set to 0.1 V and for REFx(9:0) = 0x3FF to 1.1 V.

To calculate the D/A converter value for each REFx value, use the following expression:

$$Vref = Vref_0(1 + \frac{\Delta Vref(\%)}{100})^{n+1}, n \text{ from } 0 \text{ to } 1023$$

Where  $Vref_0$  is the minimum value (typically 0.1 V),  $\Delta Vref(\%)$  is the step value (typically 0.235 %) and  $n$  is the value of register REFx in decimal.

#### Linear mode

The reference voltage for the regulation can be chosen from a 10 bit logarithmic DAC or a 10 bit linear DAC with the LINLOGx register.

$$VDAClinear = REF * \frac{VFS}{1024}$$

| LINLOG1 |                                 | Addr. 0x1E; bit bit 3 | R/W 0 |
|---------|---------------------------------|-----------------------|-------|
| LINLOG2 |                                 | Addr. 0x1E; bit bit 7 | R/W 0 |
| Code    | Function                        |                       |       |
| 0       | Logarithmic 10 bit DAC selected |                       |       |
| 1       | Linear 10 bit DAC selected      |                       |       |

Table 65: Linear or Logarithmic reference selection

LINLOGx affects the Overcurrent detection:

| LINLOGx | OVC             |
|---------|-----------------|
| 0       | Normal function |
| 1       | Disabled        |

Table 66: Overcurrent detection in linear/logarithmic mode

### 10 BIT LINEAR A/D CONVERTER

A 10 bit linear A/D converter is available for each channel when working in MCU mode. A variety of voltages can be measured by the converter with two resolutions:

- V(LDAx) up to 11 V with 11.81 mV resolution
- V(VDD) up to 8 V with 8.6 mV resolution
- V(VB) up to 11 V with 11.81 mV resolution
- V(VBLx) up to 11 V with 11.81 mV resolution
- V(MDKx) up to 1.1 V with 1.075 mV resolution
- V(RACC) up to 1.1 V with 1.075 mV resolution
- V(PLRx) up to 1.1 V with 1.075 mV resolution

The register bits ADCCx select the signal measured with the 10 bit A/D converter.

| ADCC1(2:0) |   | Addr. 0x10; bit 7:5 | R/W 000 |
|------------|---|---------------------|---------|
| Code       | Function  |                     |         |
| 0xx        | Channel 1 ADC disabled                                  |                     |         |
| 100        | Channel 1 ADC sourced by V(MDK1), ADFNS1 = 1, CMES1 = 0 |                     |         |
| 100        | Channel 1 ADC sourced by V(PLR1), ADFNS1 = 0, CMES1 = 0 |                     |         |
| 100        | Channel 1 ADC sourced by ACC current sensor, CMES1 = 1  |                     |         |
| 101        | Channel 1 ADC sourced by V(VB)                          |                     |         |
| 110        | Channel 1 ADC sourced by V(VBL1)                        |                     |         |
| 111        | Channel 1 ADC sourced by V(LDA1)                        |                     |         |

Table 67: ADC channel 1 source selection

| ADCC2(2:0) |   | Addr. 0x15; bit 7:5 | R/W 000 |
|------------|---|---------------------|---------|
| Code       | Function  |                     |         |
| 0xx        | Channel 2 ADC disabled                                  |                     |         |
| 100        | Channel 2 ADC sourced by V(MDK2), ADFNS2 = 1, CMES2 = 0 |                     |         |
| 100        | Channel 2 ADC sourced by V(PLR2), ADFNS2 = 0, CMES2 = 0 |                     |         |
| 100        | Channel 2 ADC sourced by ACC current sensor, CMES2 = 1  |                     |         |
| 101        | Channel 2 ADC sourced by V(VDD)                         |                     |         |
| 110        | Channel 2 ADC sourced by V(VBL2)                        |                     |         |
| 111        | Channel 2 ADC sourced by V(LDA2)                        |                     |         |

Table 68: ADC channel 2 source selection

With ADCCx(2:0) = 0x100, the signal to the A/D converter is selected by register bit ADFNSx. With

ADFNSx = 0 the measuring point to the A/D converter is the internal sense node of the programmable logarithmic monitor resistor (PLR) after the x2 level shifting. With ADFNSx = 1 the sensing point is connected directly to MDKx pin.

| ADFNS1 |  | Addr. 0x1A; bit 2 | R/W 0 |
|--------|--|-------------------|-------|
| Code   | Function   |                   |       |
| 0      | ADC measurement PLR1 after x2 level shifting (sense) |                   |       |
| 1      | ADC measurement MDK1 pad (force)                     |                   |       |

Table 69: ADC channel 1 force/sense selection

| ADFNS2 |  | Addr. 0x1A; bit 6 | R/W 0 |
|--------|--|-------------------|-------|
| Code   | Function   |                   |       |
| 0      | ADC measurement PLR2 after x2 level shifting (sense) |                   |       |
| 1      | ADC measurement MDK2 pad (force)                     |                   |       |

Table 70: ADC channel 2 force/sense selection

With the CMESx bit, the ADC can be used for laser current measurement in ACC mode. For this measurement, ADCCx register must be set to 0x100.

| CMES1 |                               | Addr. 0x1A; bit bit 1 | R/W 0 |
|-------|-------------------------------|-----------------------|-------|
| CMES2 |                               | Addr. 0x1A; bit bit 5 | R/W 0 |
| Code  | Function                      |                       |       |
| 0     | Optical Power selected for AD |                       |       |
| 1     | Laser current selected for AD |                       |       |

Table 71: AD selection with ADCCx(2:0)=100

As shown in Figure 8, a fraction of the current delivered by the driver to the laser is mirrored to a resistor. The voltage drop at this resistor is sourced to the ADC. For a given value of the ADC, the current can be calculated as follows

$$I(LDAx) = \frac{VFS * ADCx}{1023 * R} * MFACT$$

VFS is the full scale voltage of the A/D converter (cf. *Electrical Characteristics No. 706*), typically 1.1 V. MFACT is the mirror factor between the LDA driver and

the measurement. This Factor depends on the selected current range (CRNG(1:0)) as per Table below:

| ACC mirror factor |       |                           |
|-------------------|-------|---------------------------|
| MERGE             | CRNGx | Mirror factor             |
| 0                 | 00    | Mirror Factor set to 2500 |
| 0                 | 01    | Mirror Factor set to 333  |
| 0                 | 10    | Mirror Factor set to 83   |
| 0                 | 11    | Mirror Factor set to 30   |
| 1                 | 00    | Mirror Factor set to 5000 |
| 1                 | 01    | Mirror Factor set to 666  |
| 1                 | 10    | Mirror Factor set to 166  |
| 1                 | 11    | Mirror Factor set to 60   |

Table 72: Mirror factor

R is the value of the measurement resistance, this value depends on RACC as per Table below:

| RACC1 |   | Addr. 0x1A; bit 0 | R/W 0 |
|-------|---|-------------------|-------|
| Code  | Function  |                   |       |
| 0     | Current range high for channel 1, Current sensor resistor (Rsensex) set to 2 kΩ |                   |       |
| 1     | Current range low for channel 1, Current sensor resistor (Rsensex) set to 16 kΩ |                   |       |

Table 73: Current range configuration channel 1

| RACC2 |   | Addr. 0x1A; bit 4 | R/W 0 |
|-------|---|-------------------|-------|
| Code  | Function  |                   |       |
| 0     | Current range high for channel 2, Current sensor resistor (Rsensex) set to 2 kΩ |                   |       |
| 1     | Current range low for channel 2, Current sensor resistor (Rsensex) set to 16 kΩ |                   |       |

Table 74: Current range configuration channel 2

Since all of the above values are typical, a calibration measurement is recommended to calculate the offset of each device.

When enabled, the A/D converter is continuously acquiring the signal selected by register ADCCx. The conversion time is 140 μs. Changing the source with ADCCx may require up to 500 μs settling time of the sampling capacitors. Every time a conversion is finished the bit DRDYx is set. The MCU can poll the registers DRDYx and when a conversion is ready, read the correspondent data registers. The registers DRDYx are cleared when read and set back to one after a new conversion is ready.

### Sampling input signals at a certain moment

To perform a conversion of an input signal at a certain moment (sampling), procedure can be as follows:

1. Set ADCCx to the desired input source and wait for the settling time (up to 500 μs)
2. Disable ADC if not already disabled (ADCCx(2) set to 0). This will cause DRDYx to be cleared
3. Enable ADC at the desired measurement moment to hold the input signal (ADCCx(2) set to 1)
4. Poll DRDYx register until set to one and read ADC data
5. Repeat from point 2

As the A/D converter is 10 bit long, the results are split into two byte wide separated registers: ADCxh containing channel x ADC MSBs values while ADCxl stores the LSBs. The A/D converter must be stopped before the result can be read to prevent measurement change during MSB and LSB readout. The procedure is as follows:

1. Set ADCCx to the desired input source with the ADC disabled (ADCCx, bit 2 set to 0) and wait for the settling time (Item. 701, up to 500 us)
2. Start ADC conversion (ADCCx, bit 2 set to 1)
3. Wait for DRDYx set to 1
4. Stop the ADC (ADCCx, bot 2 set to 0)
5. Read the ADC data
6. If ADC input source doesn't need to be changed, repeat from 2

| ADC1  |                   | Addr. 0x03/04; bit 9:0 | R |
|-------|-------------------|------------------------|---|
| Code  | Function          |                        |   |
| 0x000 | ADC minimum value |                        |   |
| 0x3FF | ADC maximum value |                        |   |

Table 75: ADC channel 1

| ADC2  |                   | Addr. 0x05/06; bit 9:0 | R |
|-------|-------------------|------------------------|---|
| Code  | Function          |                        |   |
| 0x000 | ADC minimum value |                        |   |
| 0x3FF | ADC maximum value |                        |   |

Table 76: ADC channel 2

| DRDY1 |                                 | Addr. 0x07; bit bit 0 | R |
|-------|---------------------------------|-----------------------|---|
| DRDY2 |                                 | Addr. 0x07; bit bit 1 | R |
| Code  | Function                        |                       |   |
| 0     | No new ADC data since last read |                       |   |
| 1     | New ADC data available          |                       |   |

Table 77: ADC data ready

The voltage corresponding to the measured digital value can be directly obtained through the following formula:

$$V(LDAx, VB, VBLx) = 11 * \frac{VFS}{1023} * ADCx$$

$$V(VDD) = 8 * \frac{VFS}{1023} * ADCx$$

$$V(MDKx, PLRx) = \frac{VFS}{1023} * ADCx$$

VFS is the full scale voltage of the A/D converter (cf. *Electrical Characteristics No. 706*), typically 1.1 V. For a more precise measurement, the A/D converter can be calibrated by measuring a known VB voltage and calculate the VFS.

With ADFNSx = 1 the sensing point is connected directly to pin MDKx. Depending on the regulation voltage, it is possible that V(MDKx) is higher than 1.1 V. When pin MDKx is the source of the A/D converter, saturation of the converter will occur. When monitoring pin MDKx with the A/D converter, V(MDKx) must be lower than 1.1 V.

### DC/DC CONVERTER OPTIMIZATION

iC-HTP provides a 6 bit configurable current at pin DCO that can be used to trim the output voltage of a DC/DC converter. In stand-by mode the DCO current source is disconnected and set to high impedance.

Possible application which benefit from using DCO:

- DC/DC step down operation: regulation at voltages lower than power supply
- DC/DC step up operation: regulation at voltages higher than power supply
- Efficiency enhancement

The proposed applications can be demonstrated with a standard DC/DC converter e.g. TPS63060DSC from

Texas Instruments. This converter allows an input voltage ranging from 2.5 to 12 V and offers an output voltage from 2.5 to 8 V. It is capable of delivering up to 2 A current, depending on the output voltage. Figure 22 shows a possible configuration.

| RDCO |  | Addr. 0x1B; bit 5:0 | R/W 0x02 |
|------|--|---------------------|----------|
| Code | Function   |                     |          |
| 0x00 | No current   |                     |          |
| ...  |  |                     |          |
| 0x3F | Typ. 130 µA (cf. <i>Electrical Characteristics No. D01</i> ) |                     |          |

Table 78: Digital current output register

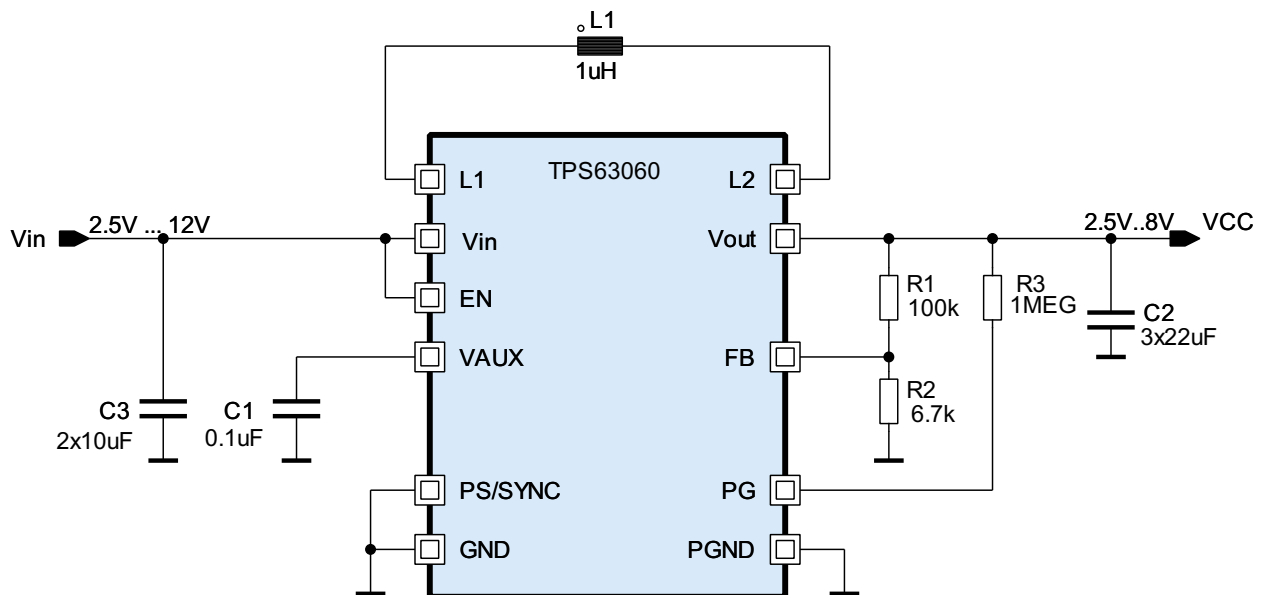


Figure 22: TPS63063 DC/DC converter from TI

#### DC/DC step down operation

The resistors R1 and R2 in the feedback path allow setting the desired output value, Vout. The DC/DC converter drives pin Vout in order to yield 0.5 V at feedback pin FB. The DCO output signal from iC-HTP is con-

nected to pin FB. Vout is controlled with the internal register RDCO.

The DCO current into FB controls the voltages of the divider R1 and R2 and Vout changes in order to maintain 0.5 V at pin FB. Selecting R1 and R2 needs to consider:

- Resistors values:  $R1 = R2(\frac{V_{out}}{V_{fb}} - 1)$
- Current of the voltage divider should be high enough, in comparison to the current from the pin DCO, to offer acceptable resolution. The programmable current resolution from register RDCO is  $2 \mu A$ .
- DCO current into the voltage divider will lower  $V_{out}$ , which is 8 V with no current at DCO.

$$RDCO = \frac{I_{dco}}{2 \mu A} = \frac{IR2 - IR1}{2 \mu A} = \frac{0.5 V}{6.7 k\Omega} - \frac{V_{out} - 0.5 V}{100 k\Omega}$$

The resulting value will vary slightly depending on the tolerances of the selected resistors and DCO current.

The voltage is reduced from 8 V ( $RDCO = 0$ ) to 2.5 V, when  $RDCO = 27$ .

Choosing  $R1$  to  $100 k\Omega$ , the value of  $R2$  can be calculated:

$$R2 = \frac{R1}{\frac{V_{out}}{V_{fb}} - 1} = \frac{100 k\Omega}{\frac{8 V}{0.5 V} - 1} = 6.7 k\Omega$$

With this configuration the current through the voltage divider is  $75 \mu A$  at 8 V. The resolution of each  $RDCO$  step then is 200 mV.

The value in  $RDCO$  register needed in order to have the desired output voltage can be calculated using the following formula:

### DC/DC step up operation

A practical application of the present case is the control of blue lasers. This type of laser present a forward voltage around 5 V, which demands an LDA voltage of about 6 V. If the system is supplied with a 3 V LiPo battery, it is necessary to use a the DC/DC in order to step up and drive the laser diode and driver with a sufficient voltage. Figure 23 shows this application:

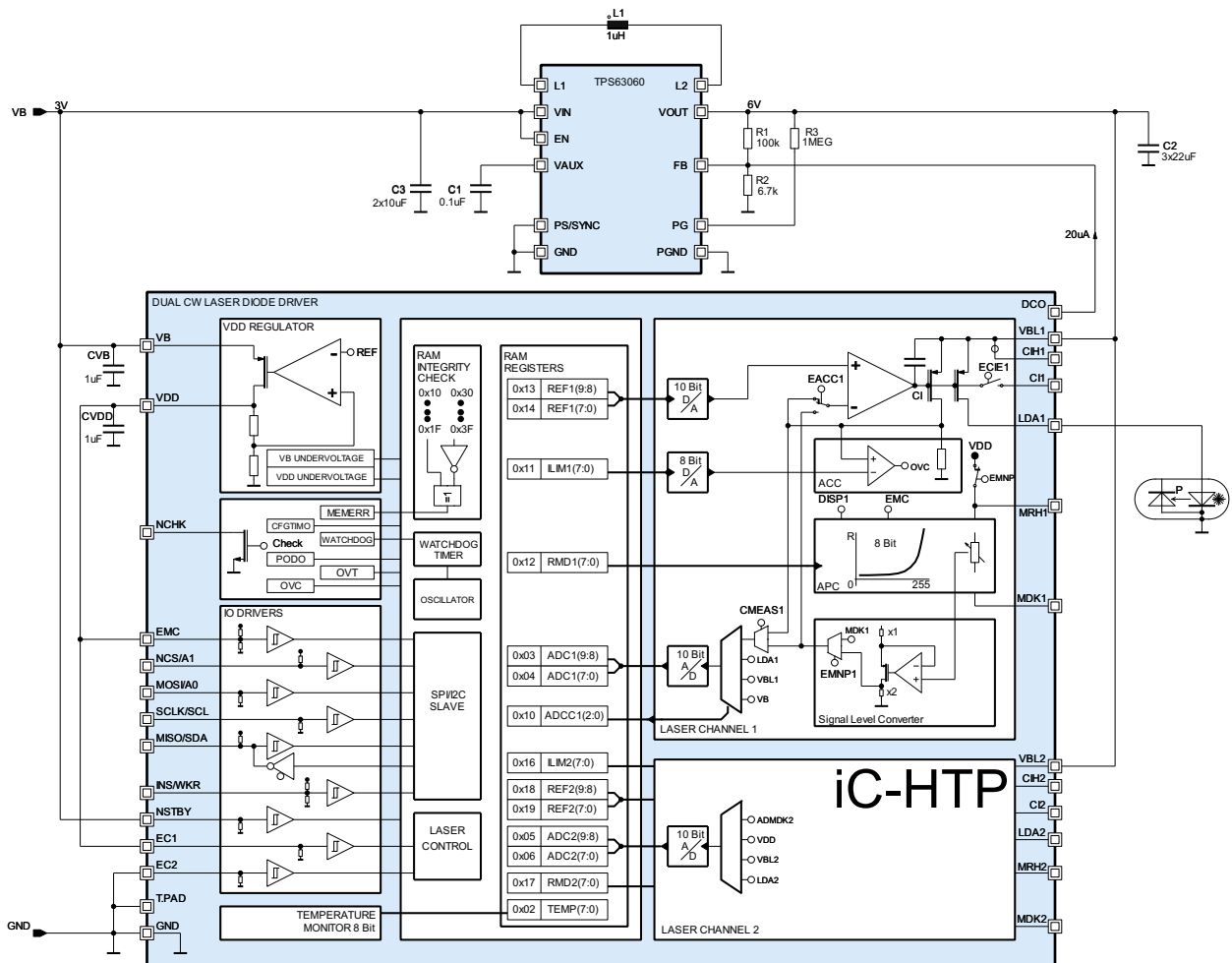


Figure 23: Regulation at voltage greater than power supply

Setting register  $RDCO$  to 10 yields  $20 \mu A$  and 6 V at  $V_{out}$ .

### Extension of system working voltage range

$iC-HTP$  must be supplied from a voltage within the threshold values of 2.8 and 11 V. It is possible to con-



control the DC/DC output in a voltage range of 2.5 to 12 V, if the DC/DC converter, controlled by output signal DCO, is included in the system, as shown in Figure 24:

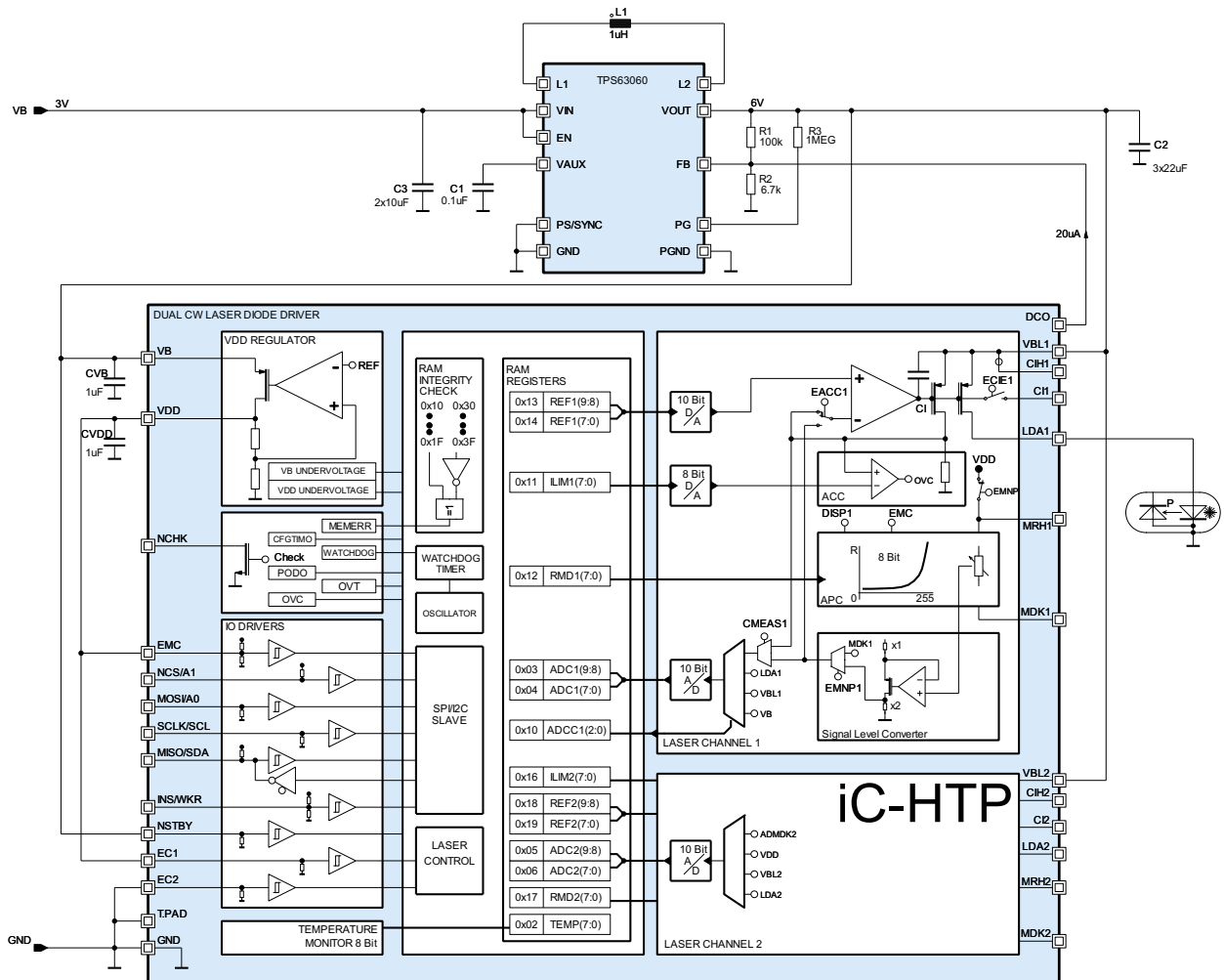


Figure 24: Extension of working voltage range

In Figure 24 both the laser and the iC-HTP are supplied by the DC/DC converter. The register RDCO is set to 23, which forces 48 µA to be output to the voltage divider. A system voltage of 3.3V is obtained at Vout.

### Efficiency enhancement

If iC-HTP and the laser diode are supplied with the same power supply, the efficiency of the driver can be

improved, depending on the supply voltage, the saturation voltage and the laser diodes forward voltage. Power dissipation of the driver can be reduced if LDAx is fed through the DC/DC converter configured to deliver a lower voltage than the power supply as shown in Figure 25.

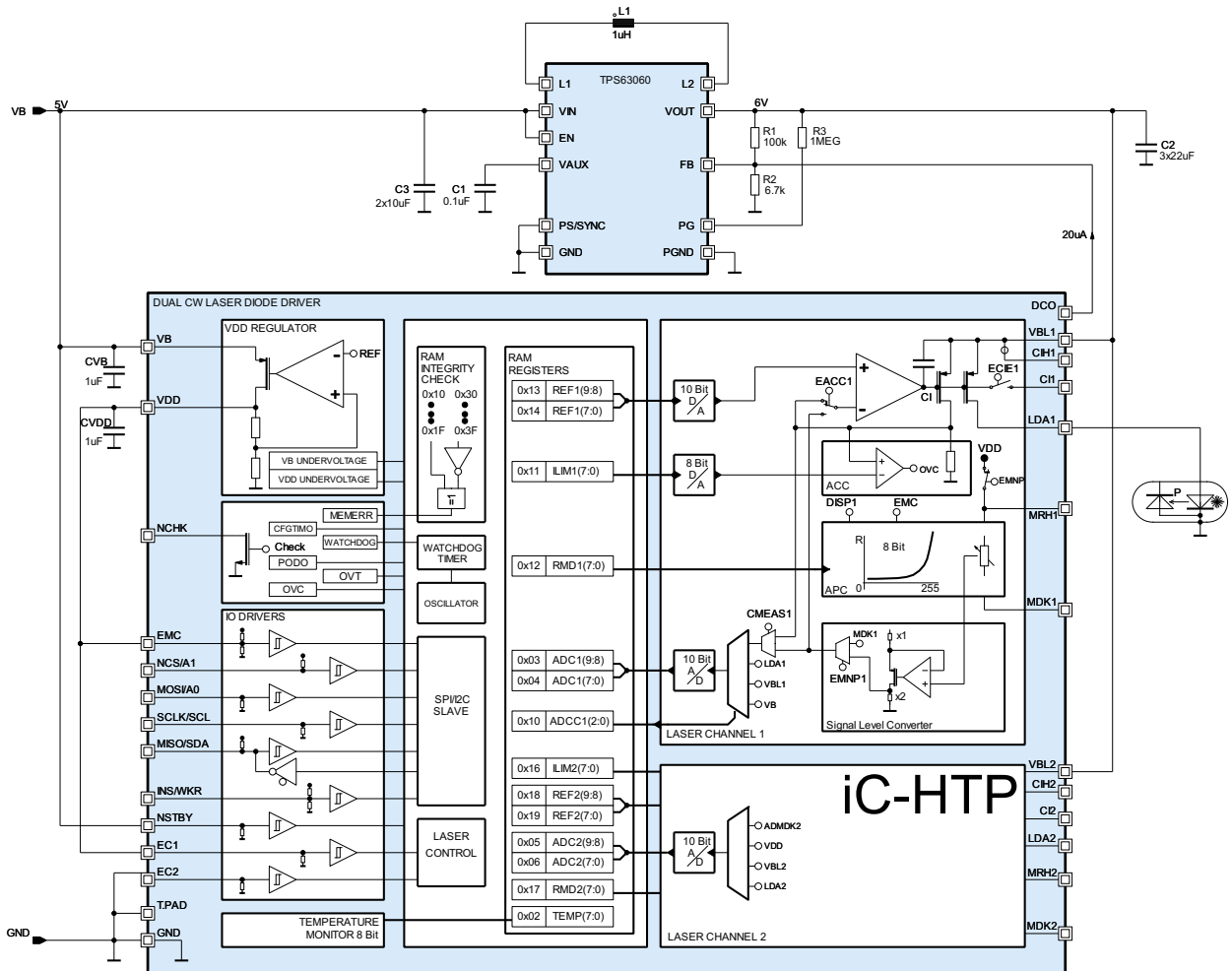


Figure 25: System efficiency enhancement

Register RDCO is set to 23 to provide a laser diode supply voltage of 3.3 V at Vout.

### WATCHDOG TIMER

The internal 200 kHz oscillator is monitored by the Watchdog Timer (WDT).

| OSCERR |   | Addr. 0x00; bit 6 | R |
|--------|---|-------------------|---|
| Code   | Function  |                   |   |
| 0      | Oscillator functioning OK                             |                   |   |
| 1      | Watchdog timeout, oscillator failure; cleared on read |                   |   |

Table 79: Oscillator watchdog

The state of OSCERR is signaled at pin NCHK. Setting MOSCERR to 1 masks the oscillator error and OSCERR will not be signaled at NCHK.

| MOSCERR |  | Addr. 0x1D; bit 0 | R/W 0 |
|---------|--|-------------------|-------|
| Code    | Function   |                   |       |
| 0       | Oscillator error (watchdog) will be signaled at NCHK     |                   |       |
| 1       | Oscillator error (watchdog) will not be signaled at NCHK |                   |       |

Table 80: Oscillator watchdog error mask

If the oscillator remains longer than the maximum time of tWDT (cf. *Electrical Characteristics No. E03*) without activity, an oscillator error is generated which sets OSCERR error bit to 1. The automatic offset compensation of the laser control requires the oscillator.

It is possible to simulate an error of the oscillator using bit SOSCERR. With OSCERR set to 1 the error will be signaled through NCHK, depending on the state of MOSCERR.

| <b>SOSCERR</b> |   | Addr. 0x1D; bit 7 | R/W 0 |
|----------------|---|-------------------|-------|
| Code           | Function                                      |                   |       |
| 0              | No oscillator error simulated                 |                   |       |
| 1              | Oscillator error simulated (watchdog timeout) |                   |       |

Table 81: Simulate oscillator error

### TEMPERATURE MONITOR AND PROTECTION

iC-HTP includes an 8 bit temperature monitor that allows to measure the internal chip temperature going from  $-40$  to  $125^{\circ}\text{C}$ . The resolution is  $1^{\circ}\text{C}/\text{LSB}$ . The internal temperature can be obtained by reading TEMP register. The TEMP register is a read-only register.

| <b>TEMP</b> |                     | Addr. 0x02; bit 7:0 | R |
|-------------|---------------------|---------------------|---|
| Code        | Function            |                     |   |
| 0x00        | Minimum temperature |                     |   |
| ...         |                     |                     |   |
| 0xFF        | Maximum temperature |                     |   |

Table 82: Chip temperature

Absolute read values may differ from one chip to another. **An individual initial calibration of the temperature monitor is recommended.** The TEMP register must be read at a known temperature. Using the resolution value of  $1^{\circ}\text{C}/\text{LSB}$ , the internal temperature can be calculated.

The temperature monitor can be used to compensate temperature effects of the laser diode. The MCU can use a laser diode characteristics formula or a look-up table combined with the measured temperature value. The reference voltage can be configured accordingly in order to compensate temperature effects.

iC-HTP is protected against overtemperature. In iC-WK mode, if the internal temperature value exceeds the overtemperature threshold, an OVT error event will be triggered and signaled at pin NCHK. Both laser channels will be disabled. Pin NCHK will keep signaling the error although the internal temperature falls to a safe value below the overtemperature threshold value. If the temperature has exceeded the overtemperature

threshold value, pins EC1 and EC2 have to be pulled lo in order to stop signaling the error. Setting pin ECx back hi will re-enable the corresponding channel.

In MCU mode, if the internal temperature exceeds a safety value, the overtemperature error bit OVT will be set to 1. With  $\text{OVT} = 1$ , both channels will be disabled and the error event will be signaled at pin NCHK. If the internal temperature falls to a safe value below the overtemperature threshold value, OVT will remain at value 1. Reading the OVT bit resets it and stops signaling this error at pin NCHK. Cycling pin ECx will re-enable the corresponding channel.

The overtemperature threshold value can not be configured.

| <b>OVT</b> |   | Addr. 0x00; bit 3 | R |
|------------|---|-------------------|---|
| Code       | Function  |                   |   |
| 0          | No overtemperature event has occurred since last read |                   |   |
| 1          | Overtemperature event has occurred. Cleared on read   |                   |   |

Table 83: Overtemperature

In MCU mode it is possible to simulate an overtemperature event setting SOVT to 1. The overtemperature error flag OVT will be set to 1. iC-HTP will remain in error state until SOVT is set back to 0.

| <b>SOVT</b> |                                       | Addr. 0x1D; bit 4 | R/W 0 |
|-------------|---------------------------------------|-------------------|-------|
| Code        | Function                              |                   |       |
| 0           | No overtemperature event is simulated |                   |       |
| 1           | Overtemperature event simulated       |                   |       |

Table 84: Simulate overtemperature

### DIGITAL INTERFACE AND MEMORY INTEGRITY MONITOR

iC-HTP provides a microcontroller slave interface by selection on pin EMC. SPI or I<sup>2</sup>C are selected by pin INS/WKR.

| EMC  | Addr. Pin;                                      |
|------|---|
| lo   | iC-WK-mode, digital interfaces disabled         |
| Open | Not allowed, error signaled                     |
| hi   | MCU mode, interface selected by INS/WKR enabled |

Table 85: Enable microcontroller

| INS/WKR | Addr. Pin;                          |
|---------|-------------------------------------|
| lo      | SPI interface selected              |
| Open    | Not allowed, error signaled         |
| hi      | I <sup>2</sup> C interface selected |

Table 86: Interface selection I<sup>2</sup>C or SPI

The configuration memory is integrity monitored and **atomic executable** (all at once: changes of the configurations without any direct effects, the changes are executed at once by command) to the functional blocks of iC-HTP.

Integrity monitoring is implemented by a duplication of the configuration registers into a validation page (see description below) where the registers are automatically copied with inverted values. Every register bit is compared with its validation copy and in case of difference, a memory error is generated and both laser channels are switched off.

Atomic appliance is achieved by latching the configuration registers. This permits a full configuration (different registers) to be made prior to applying it to the laser

channels. iC-HTP has two different modes selectable by the MODE(1:0) register (addr. 0x1C).

| MODE(1:0) | Addr. 0x1C; bit 1:0   | R/W 01 |
|-----------|---|--------|
| Code      | Function  |        |
| 00        | Not allowed   |        |
| 01        | Chip set in operation mode (apply configuration, latch transparent) |        |
| 10        | Chip set in configuration mode (hold previous configuration)        |        |
| 11        | Not allowed   |        |

Table 87: Configuration and operation mode

In **Configuration Mode** the *configuration memory* (addr. 0x10 to 0x1F) can be written and read back to check a correct communication without changing the present configuration of the iC-HTP. In this mode, the memory integrity check is disabled.

iC-HTP will monitor the time elapsed in configuration mode and automatically switch the laser off, if it exceeds the configuration mode timeout. The time in configuration mode must be less than 40 ms for ensuring that no configuration timeout occurs during configuration (cf. *Electrical Characteristics No. E02*). The timeout can be up to 164 ms.

When writing the configuration is completed, iC-HTP is switched to **Operation Mode** by writing 0b01 into register MODE (addr. 0x1C). The configuration is applied to the iC-HTP and the memory integrity check activated. Configuration registers can only be read (except register MODE(1:0), which is always accessible). Figure 26 shows the interface to the memory structure.

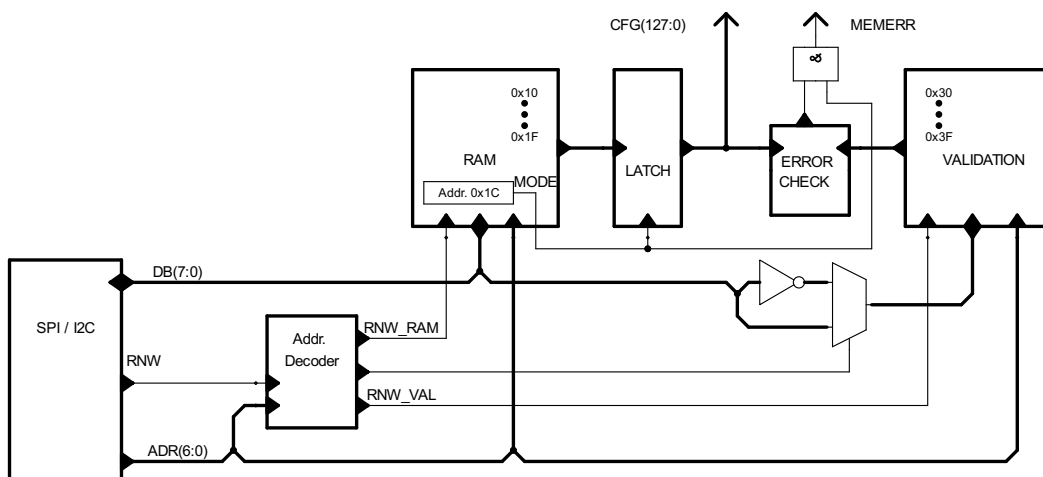


Figure 26: Interface, RAM integrity monitoring and configuration latching

### Register map description

The register map consists of 64 addresses subdivided in three different pages:

- Read-only page, addr. 0x00 to 0x0F: iC-HTP status, ADC readouts, temperature sensor readout and chip revision
- Configuration page (integrity monitored), read-write registers, addr. 0x10 to 0x1F
- Validation page, read-write registers, addr. 0x30 to 0x3F

### Read-only registers

Read-only registers are sub-divided as well into status registers (addr. 0x00 to 0x01) and measurement registers. Status registers are normally latched to 1 on events and cleared on read (see individual register description). Measurement registers are dual-port and can be accessed simultaneously with the measurements in progress. ADC1 (addr. 0x03 to 0x04) and ADC2 (addr. 0x05 to 0x06) are 10 bit registers split into two 8 bit registers each and must be accessed in block mode (automatic address increment) to ensure data not changing during read.

### Configuration page (integrity monitored)

The configuration page (addr. 0x10 to 0x1F) contains the registers that control the driver. Every write operation to any of the registers of this page will be internally duplicated to the correspondent register at the validation page. After the write operation, the correspondent validation register will contain the inverted value of the configuration register.

### Validation page

The validation page (addr. 0x30 to 0x3F) can be read or written normally. Only when a write procedure is made to any of the configuration registers, the correspondent validation pair will be written with the inverted value of the configuration register as well.

Both the configuration and validation pages are initialized during power-up. This event is signaled at the STATUS0 register (bit 0, INITRAM). In standby mode (NSTBY = lo) the RAM is not reset if any write command has been executed and therefore, configuration and validation pages keep the stored information and INITRAM remains unset. Entering standby mode after power-up without any write command, the RAM will be initialized again and the INITRAM bit will be set to 1 again. Any VDD power-down event signaled at the STATUS0 register outside the standby mode (NSTBY = hi) requires a RAM content check regardless of the state of the INITRAM bit to ensure data is not corrupted.

### Possible start-up sequence

1. iC-HTP starts in operation mode with default configuration. INITRAM, PDOVBLx and PDOVDD error bits must be set in STATUSx, DISC1 (addr. 0x10, bit 3) and DISC2 (addr. 0x15, bit 3) are set to 1.
2. Write MODE(1:0) = 10 register (addr. 0x1C) to enable the configuration mode.
3. Configure the laser channels.
4. Read back to verify a correct data transfer.
5. Set the DISC1, DISC2 bits to 0 on used channels.
6. Read the status registers (addr. 0x00, 0x01, 0x02) to detect possible errors and validate status. If any error exists, read again to ensure its validity.
7. Write MODE(1:0) = 01 register (addr. 0x1C) to apply the configuration and enable the memory integrity check.
8. During operation: monitor the status registers checking for errors. Pin NCHK signals any set status bit if not masked. This pin can be used to trigger an microcontroller interrupt line.

### START-UP AND STANDBY

Setting pin NSTBY to lo puts iC-HTP into standby. In standby with VDD disabled the current consumption on VB is reduced to less than 10  $\mu$ A (cf. *Electrical Characteristics No. 002*).

After wake-up (rising edge at pin NSTBY), the internal regulated supply VDD is supplied again. The required time TVdd depends on the capacitor connected to pin VDD (cf. *Electrical Characteristics No. 504*).

Once the VDD voltage level is correct, iC-HTP enters an offset compensation procedure regardless of the state of the laser enable pins (EC1, EC2). During this time (Ten), EC1 and EC2 are ignored and laser cannot be switched on (cf. *Electrical Characteristics No. 111*).

The switch-on procedure needs an initial time (Tci) to reach the 80% of the target light power (in APC mode) or laser current (in ACC mode) (cf. *Electrical Characteristics No. 112*) and an additional time (Tcio) to reach the 99% of the value (cf. *Electrical Characteristics No. 113*).

Figure 27 illustrates an startup example for channel 1 in iC-WK mode.

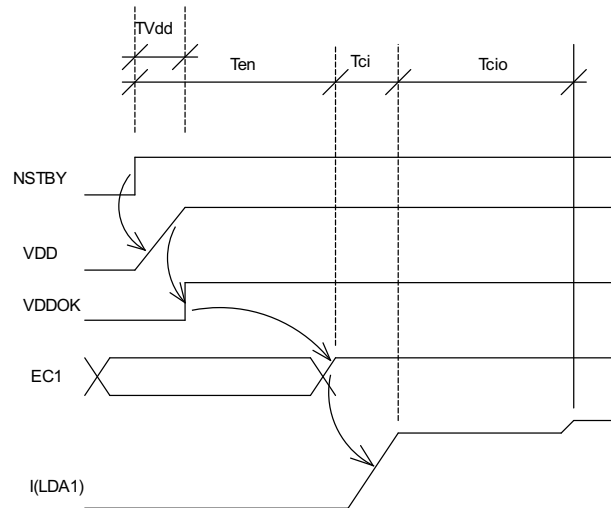


Figure 27: Startup timing diagram

### REGISTER OVERVIEW

| OVERVIEW |  |            |            |       |             |          |            |         |
|----------|--|------------|------------|-------|-------------|----------|------------|---------|
| Addr     | Bit 7  | Bit 6      | Bit 5      | Bit 4 | Bit 3       | Bit 2    | Bit 1      | Bit 0   |
| 0x00 R   | CFGTIMO                                      | OSCERR     | OVC1       | OVC2  | OVT         | MEMERR   | PDOVDD     | INITRAM |
| 0x01 R   | PDOVBL2                                      | LDASAT2    | MONC2      | MAPC2 | PDOVBL1     | LDASAT1  | MONC1      | MAPC1   |
| 0x02 R   | TEMP(7:0)                                    |            |            |       |             |          |            |         |
| 0x03 R   |  |            |            |       |             |          | ADC1(9:8)  |         |
| 0x04 R   | ADC1(7:0)                                    |            |            |       |             |          |            |         |
| 0x05 R   |  |            |            |       |             |          | ADC2(9:8)  |         |
| 0x06 R   | ADC2(7:0)                                    |            |            |       |             |          |            |         |
| 0x07     |  |            |            |       |             |          | DRDY2      | DRDY1   |
| 0x08 R   | Not implemented                              |            |            |       |             |          |            |         |
| ...      | Not implemented                              |            |            |       |             |          |            |         |
| 0x0E R   | Not implemented                              |            |            |       |             |          |            |         |
| 0x0F R   | CHIPREV(7:0)                                 |            |            |       |             |          |            |         |
| 0x10     | ADCC1(2:0)                                   |            |            | 1     | DISC1       | DISP1    | ECIE1      | EACC1   |
| 0x11     | ILIM1(7:0)                                   |            |            |       |             |          |            |         |
| 0x12     | RMD1(7:0)                                    |            |            |       |             |          |            |         |
| 0x13     | EPUL1  | COMP1(2:0) |            |       | RLDAS1(1:0) |          | REF1(9:8)  |         |
| 0x14     | REF1(7:0)                                    |            |            |       |             |          |            |         |
| 0x15     | ADCC2(2:0)                                   |            |            | 1     | DISC2       | DISP2    | ECIE2      | EACC2   |
| 0x16     | ILIM2(7:0)                                   |            |            |       |             |          |            |         |
| 0x17     | RMD2(7:0)                                    |            |            |       |             |          |            |         |
| 0x18     | EPUL2  | COMP2(2:0) |            |       | RLDAS2(1:0) |          | REF2(9:8)  |         |
| 0x19     | REF2(7:0)                                    |            |            |       |             |          |            |         |
| 0x1A     | EMNP2  | ADFNS2     | CMES2      | RACC2 | EMNP1       | ADFNS1   | CMES1      | RACC1   |
| 0x1B     |  | MERGE      | RDCO(5:0)  |       |             |          |            |         |
| 0x1C     | Not implemented                              |            |            |       |             |          | MODE(1:0)  |         |
| 0x1D     | SOSCERR                                      | SOVC2      | SOVC1      | SOVT  | MLDASAT2    | MLDASAT1 | MMONC      | MOSCERR |
| 0x1E     | LINLOG2                                      | 1          | CRNG2(1:0) |       | LINLOG1     | 1        | CRNG1(1:0) |         |
| 0x1F     | Reserved register(Factory test). Set to zero |            |            |       |             |          |            |         |
| 0x20     | Not implemented                              |            |            |       |             |          |            |         |
| ...      | Not implemented                              |            |            |       |             |          |            |         |
| 0x30     | Validation content for 0x10, inverted        |            |            |       |             |          |            |         |
| 0x31     | Validation content for 0x11, inverted        |            |            |       |             |          |            |         |
| ...      | ...  |            |            |       |             |          |            |         |
| 0x3F     | Validation content for 0x1F, inverted        |            |            |       |             |          |            |         |

Table 88: Register layout

### STATUS AND PARAMETERS

iC-HTP contains identification, status information, converted data information, and parameters.

The status information represents the accessible state of iC-HTP at this time. Reading status may change the state itself e.g. resetting a read state.

| Register | Address | Bits | Default | Description   |
|----------|---------|------|---------|---|
| INITRAM  | 0x00    | 0    | R/O     | RAM initialized.  |
| PDOVDD   | 0x00    | 1    | R/O     | Power-down event at VDD   |
| MEMERR   | 0x00    | 2    | R/O     | RAM memory validation error   |
| OVT      | 0x00    | 3    | R/O     | Overtemperature event   |
| OVC2     | 0x00    | 4    | R/O     | Overcurrent at channel 2  |
| OVC1     | 0x00    | 5    | R/O     | Overcurrent at channel 1  |
| OSCERR   | 0x00    | 6    | R/O     | Oscillator error (watchdog set)   |
| CFGTIMO  | 0x00    | 7    | R/O     | Configuration mode timeout event  |
| MAPC1    | 0x01    | 0    | R/O     | Channel 1 current state   |
| MONC1    | 0x01    | 1    | R/O     | Monitor channel 1 enabled at least once (latched)                           |
| LDASAT1  | 0x01    | 2    | R/O     | Channel 1 LDA saturation event  |
| PDOVBL1  | 0x01    | 3    | R/O     | Power down event at VBL1 or power down in any of VBL1 or VBL2 in merge mode |
| MAPC2    | 0x01    | 4    | R/O     | Channel 2 current state   |
| MONC2    | 0x01    | 5    | R/O     | Monitor channel 2 enabled at least once (latched)                           |
| LDASAT2  | 0x01    | 6    | R/O     | Channel 2 LDA saturation event  |
| PDOVBL2  | 0x01    | 7    | R/O     | Power down event at VBL2 or VBL1 not equal to VBL2 in merge mode            |

Table 89: Status overview

The converted data information represents the signals that have been selected and converted by iC-HTP, its multiplexer and the ADC. Reading a value represents the last converted signal.

| Register | Address | Bits | Default | Description                  |
|----------|---------|------|---------|------------------------------|
| TEMP     | 0x02    | 7:0  | R/O     | Chip temperature measurement |
| ADC1h    | 0x03    | 1:0  | R/O     | Channel 1 ADC 9:8 readout    |
| ADC1l    | 0x04    | 7:0  | R/O     | Channel 1 ADC 7:0 readout    |
| ADC2h    | 0x05    | 1:0  | R/O     | Channel 2 ADC 9:8 readout    |
| ADC2l    | 0x06    | 7:0  | R/O     | Channel 2 ADC 7:0 readout    |
| DRDY     | 0x07    | 1:0  | R/O     | ADC Data ready               |

Table 90: Measurement overview

The identification information indicates the chip revision of an iC-HTP.

| Register | Address | Bits | Default | Description                  |
|----------|---------|------|---------|------------------------------|
| CHIPREV  | 0x0F    | 7:0  | R/O     | Chip revision identification |

Table 91: Identification



# iC-HTP

## DUAL CW P-TYPE LASER DIODE DRIVER



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| Register  | Address   | Bits | Default | Description  |
|-----------|-----------|------|---------|--|
| ADCC1     | 0x10      | 7:5  | 000     | Configuration for ADC from channel 1               |
| ADCC2     | 0x15      | 7:5  | 000     | Configuration for ADC from channel 2               |
| ADFNS1    | 0x1A      | 2    | 0       | MDK force/sense for ADC measurement in channel 1   |
| ADFNS2    | 0x1A      | 6    | 0       | MDK force/sense for ADC measurement in channel 2   |
| CMES1     | 0x1A      | 1    | 0       | Enable current measurement for ADC in channel 1    |
| CMES2     | 0x1A      | 5    | 0       | Enable current measurement for ADC in channel 2    |
| RACC1     | 0x1A      | 0    | 0       | Channel 1 ACC resistor mirror factor               |
| RACC2     | 0x1A      | 4    | 0       | Channel 2 ACC resistor mirror factor               |
| COMP1     | 0x13      | 6:4  | 011     | Channel 1 regulator compensation current           |
| EPUL1     | 0x13      | 7    | 0       | Channel 1 pulsed mode                              |
| EPUL2     | 0x18      | 7    | 0       | Channel 2 pulsed mode                              |
| COMP2     | 0x18      | 6:4  | 011     | Channel 2 regulator compensation current           |
| CRNG1     | 0x1E      | 5:4  | 00      | Channel 1 current range                            |
| CRNG2     | 0x1E      | 1:0  | 00      | Channel 2 current range                            |
| DISC1     | 0x10      | 3    | 1       | Software disable for channel 1                     |
| DISC2     | 0x15      | 3    | 1       | Software disable for channel 2                     |
| DISP1     | 0x10      | 2    | 0       | Disable PLR for channel 1                          |
| DISP2     | 0x15      | 2    | 0       | Disable PLR for channel 2                          |
| EACC1     | 0x10      | 0    | 0       | Enable ACC mode for channel 1                      |
| EACC2     | 0x15      | 0    | 0       | Enable ACC mode for channel 2                      |
| ECIE1     | 0x10      | 1    | 0       | Enable external CI capacitor for channel 1         |
| ECIE2     | 0x15      | 1    | 0       | Enable external CI capacitor for channel 2         |
| ILIM1     | 0x11      | 7:0  | 0xFF    | Current limit at channel 1                         |
| ILIM2     | 0x16      | 7:0  | 0xFF    | Current limit at channel 2                         |
| MERGE     | 0x1B      | 6    | 0       | MERGE channels 1 and 2, controlled by channel 1    |
| MLDASAT1  | 0x1D      | 2    | 1       | LDASAT1 error mask                                 |
| MLDASAT2  | 0x1D      | 3    | 1       | LDASAT2 error mask                                 |
| MMONC     | 0x1D      | 1    | 1       | MONC error mask                                    |
| MODE      | 0x1C      | 1:0  | 01      | Configuration / operation mode selection           |
| MOSCERR   | 0x1D      | 0    | 0       | OSCERR error mask                                  |
| RDCO      | 0x1B      | 5:0  | 0x02    | DC converter set point                             |
| REF1      | 0x13/0x14 | 9:0  | 0x000   | Voltage reference at channel 1                     |
| REF2      | 0x18/0x19 | 9:0  | 0x000   | Voltage reference at channel 2                     |
| RLDAS1    | 0x13      | 3:2  | 00      | Channel 1 LDA saturation detector threshold        |
| RLDAS2    | 0x18      | 3:2  | 00      | Channel 2 LDA saturation detector threshold        |
| RMD1      | 0x12      | 7:0  | 0xFF    | Resistor at channel 1                              |
| RMD2      | 0x17      | 7:0  | 0xFF    | Resistor at channel 2                              |
| SOSCERR   | 0x1D      | 7    | 0       | Oscillator error simulation (watchdog timeout)     |
| SOVC1     | 0x1D      | 5    | 0       | Overcurrent event at channel 1 simulation          |
| SOVC2     | 0x1D      | 6    | 0       | Overcurrent event at channel 2 simulation          |
| SOVT      | 0x1D      | 4    | 0       | Overtemperature event simulation                   |
| CRNG1     | 0x1E      | 1:0  | 00      | Channel 1 current range                            |
| CRNG2     | 0x1E      | 5:4  | 00      | Channel 2 current range                            |
| EMNP1     | 0x1A      | 3    | 0       | Channel 1 laser diode selection                    |
| EMNP2     | 0x1A      | 7    | 0       | Channel 2 laser diode selection                    |
| LINLOG1   | 0x1E      | 3    | 0       | Channel 1 linear / logarithmic reference selection |
| LINLOG2   | 0x1E      | 7    | 0       | Channel 2 linear / logarithmic reference selection |
| Reserved  | 0x1F      | 7:0  | 0x00    | Reserved   |
| Reserved  | 0x1A      | 7    | 0       | Reserved   |
| Reserved  | 0x1A      | 3    | 0       | Reserved   |
| Reserved1 | 0x15      | 4    | 1       | Reserved   |
| Reserved1 | 0x10      | 4    | 1       | Reserved   |

Table 92: Parameter overview

### Status

| INITRAM |                                     | Addr. 0x00; bit 0 | R |
|---------|-------------------------------------|-------------------|---|
| Code    | Function                            |                   |   |
| 0       | RAM not initialized since last read |                   |   |
| 1       | RAM initialized. Cleared on read    |                   |   |

Table 93: RAM initialization

| PDOVDD |  | Addr. 0x00; bit 1 | R |
|--------|--|-------------------|---|
| Code   | Function   |                   |   |
| 0      | VDD power down not occurred since last read        |                   |   |
| 1      | VDD power down event has occurred. Cleared on read |                   |   |

Table 94: VDD power down

| MEMERR |  | Addr. 0x00; bit 2 | R |
|--------|--|-------------------|---|
| Code   | Function                                       |                   |   |
| 0      | RAM has not been changed since last validation |                   |   |
| 1      | RAM has changed and has not been validated     |                   |   |

Table 95: Memory validation

| OVT  |   | Addr. 0x00; bit 3 | R |
|------|---|-------------------|---|
| Code | Function  |                   |   |
| 0    | No overtemperature event has occurred since last read |                   |   |
| 1    | Overtemperature event has occurred. Cleared on read   |                   |   |

Table 96: Overtemperature

| OVC2 |  | Addr. 0x00; bit 4 | R |
|------|--|-------------------|---|
| Code | Function   |                   |   |
| 0    | No overcurrent event at channel 2 has occurred since last read |                   |   |
| 1    | Overcurrent event at channel 2 has occurred. Cleared on read   |                   |   |

Table 97: Overcurrent channel 2

| OVC1 |  | Addr. 0x00; bit 5 | R |
|------|--|-------------------|---|
| Code | Function   |                   |   |
| 0    | No overcurrent event at channel 1 has occurred since last read |                   |   |
| 1    | Overcurrent event at channel 1 has occurred. Cleared on read   |                   |   |

Table 98: Overcurrent channel 1

| OSCERR |   | Addr. 0x00; bit 6 | R |
|--------|---|-------------------|---|
| Code   | Function  |                   |   |
| 0      | Oscillator functioning OK                             |                   |   |
| 1      | Watchdog timeout, oscillator failure; cleared on read |                   |   |

Table 99: Oscillator watchdog

| CFGTIMO |   | Addr. 0x00; bit 7 | R |
|---------|---|-------------------|---|
| Code    | Function  |                   |   |
| 0       | iC-HTP not in <i>Configuration Mode</i> or <i>Timeout</i> did not happen till now   |                   |   |
| 1       | iC-HTP in <i>Configuration Mode</i> and <i>Timeout</i> happened. Laser switched off |                   |   |

Table 100: Configuration timeout

| MAPC1 |  | Addr. 0x01; bit 0 | R |
|-------|--|-------------------|---|
| Code  | Function                               |                   |   |
| 0     | EC1 is 0 at the precise reading moment |                   |   |
| 1     | EC1 is 1 at the precise reading moment |                   |   |

Table 101: EC1 pin state

| MONC1 |  | Addr. 0x01; bit 1 | R |
|-------|--|-------------------|---|
| Code  | Function   |                   |   |
| 0     | EC1 has not been set to 1 since last read            |                   |   |
| 1     | EC1 has been set to 1 at least once. Cleared on read |                   |   |

Table 102: Monitor channel 1

| LDASAT1 |   | Addr. 0x01; bit 2 | R |
|---------|---|-------------------|---|
| Code    | Function  |                   |   |
| 0       | Channel 1 LDA saturation voltage not reached                            |                   |   |
| 1       | Channel 1 LDA saturation voltage reached at least once, cleared on read |                   |   |

Table 103: LDA1 saturation

| PDOVBL1 |   | Addr. 0x01; bit 3 | R |
|---------|---|-------------------|---|
| Code    | Function  |                   |   |
| 0       | VBL1 power down not occurred since last read. If MERGE = 1, VBL1 and VBL2 had no power down since last read |                   |   |
| 1       | VBL1 power down event has occurred. If MERGE = 1, VBL1 or VBL2 had a power down event. Cleared on read      |                   |   |

Table 104: VBL1 power down

| MAPC2 |  | Addr. 0x01; bit 4 | R |
|-------|--|-------------------|---|
| Code  | Function                               |                   |   |
| 0     | EC2 is 0 at the precise reading moment |                   |   |
| 1     | EC2 is 1 at the precise reading moment |                   |   |

Table 105: EC2 pin state

| <b>MONC2</b> |  | Addr. 0x01; bit 5 | R |
|--------------|--|-------------------|---|
| Code         | Function   |                   |   |
| 0            | EC2 has not been set to 1 since last read            |                   |   |
| 1            | EC2 has been set to 1 at least once. Cleared on read |                   |   |

Table 106: Monitor channel 2

| <b>LDASAT2</b> |   | Addr. 0x01; bit 6 | R |
|----------------|---|-------------------|---|
| Code           | Function  |                   |   |
| 0              | Channel 2 LDA saturation voltage not reached.                           |                   |   |
| 1              | Channel 2 LDA saturation voltage reached at least once. Cleared on read |                   |   |

Table 107: LDA2 saturation

| <b>PDOVBL2</b> |   | Addr. 0x01; bit 7 | R |
|----------------|---|-------------------|---|
| Code           | Function  |                   |   |
| 0              | VBL2 power down not occurred since last read. If MERGE = 1, VBL1 voltage level equals VBL2 voltage level            |                   |   |
| 1              | VBL2 power down event has occurred. If MERGE = 1, VBL1 voltage level not equals VBL2 voltage level. Cleared on read |                   |   |

Table 108: VBL2 power down

| <b>TEMP</b> |                     | Addr. 0x02; bit 7:0 | R |
|-------------|---------------------|---------------------|---|
| Code        | Function            |                     |   |
| 0x00        | Minimum temperature |                     |   |
| 0xFF        | Maximum temperature |                     |   |

Table 109: Chip temperature

| <b>ADC1</b> |                   | Addr. 0x03/04; bit 9:0 | R |
|-------------|-------------------|------------------------|---|
| Code        | Function          |                        |   |
| 0x000       | ADC minimum value |                        |   |
| 0x3FF       | ADC maximum value |                        |   |

Table 110: ADC channel 1

| <b>ADC2</b> |                   | Addr. 0x05/06; bit 9:0 | R |
|-------------|-------------------|------------------------|---|
| Code        | Function          |                        |   |
| 0x000       | ADC minimum value |                        |   |
| 0x3FF       | ADC maximum value |                        |   |

Table 111: ADC channel 2

| <b>DRDY1</b> |                                 | Addr. 0x07; bit bit 0 | R |
|--------------|---------------------------------|-----------------------|---|
| <b>DRDY2</b> |                                 | Addr. 0x07; bit bit 1 | R |
| Code         | Function                        |                       |   |
| 0            | No new ADC data since last read |                       |   |
| 1            | New ADC data available          |                       |   |

Table 112: ADC data ready

### Device identification

| <b>CHIPREV</b> |                        | Addr. 0x0F; bit 7:0 | R |
|----------------|------------------------|---------------------|---|
| Code           | Identification         |                     |   |
| 0x00           | Reserved               |                     |   |
| ...0x07        |                        |                     |   |
| 0x08           | Initial version iC-HTP |                     |   |
| 0x09           | iC-HTP rev Z           |                     |   |
| 0x0A           | iC-HTP rev Z1          |                     |   |
| 0x0B           | iC-HTP rev Y           |                     |   |
| 0x0C           | iC-HTP rev Y1          |                     |   |
| 0x0D           | iC-HTP rev X           |                     |   |
| 0x0E           | iC-HTP rev X1          |                     |   |
| 0x0F           | iC-HTP rev W           |                     |   |
| 0x10           | Reserved               |                     |   |
| ...0xFF        |                        |                     |   |

Table 113: Device identification

### Channel 1 configuration registers

| <b>EACC1</b> |   | Addr. 0x10; bit 0 | R/W 0 |
|--------------|---|-------------------|-------|
| Code         | Function  |                   |       |
| 0            | APC mode enabled for channel 1 (light power regulation)   |                   |       |
| 1            | ACC mode enabled for channel 1 (laser current regulation) |                   |       |

Table 114: Enable APC/ACC channel 1

| <b>ECIE1</b> |  | Addr. 0x10; bit 1 | R/W 0 |
|--------------|--|-------------------|-------|
| Code         | Function   |                   |       |
| 0            | External CI capacitor for channel 1 disconnected |                   |       |
| 1            | External CI capacitor for channel 1 connected    |                   |       |

Table 115: Enable external CI capacitor channel 1

| <b>DISP1</b> |                            | Addr. 0x10; bit 2 | R/W 0 |
|--------------|----------------------------|-------------------|-------|
| Code         | Function                   |                   |       |
| 0            | PLR enabled for channel 1  |                   |       |
| 1            | PLR disabled for channel 1 |                   |       |

Table 116: Disable PLR channel 1

| <b>DISC1</b> |  | Addr. 0x10; bit 3 | R/W 1 |
|--------------|--|-------------------|-------|
| Code         | Function                               |                   |       |
| 0            | Channel 1 can be enabled by pin EC1    |                   |       |
| 1            | Channel 1 cannot be enabled by pin EC1 |                   |       |

Table 117: Disable channel 1

| ADCC1(2:0) |   | Addr. 0x10; bit 7:5 | R/W 000 |
|------------|---|---------------------|---------|
| Code       | Function  |                     |         |
| 0xx        | Channel 1 ADC disabled                                  |                     |         |
| 100        | Channel 1 ADC sourced by V(MDK1), ADFNS1 = 1, CMES1 = 0 |                     |         |
| 100        | Channel 1 ADC sourced by V(PLR1), ADFNS1 = 0, CMES1 = 0 |                     |         |
| 100        | Channel 1 ADC sourced by ACC current sensor, CMES1 = 1  |                     |         |
| 101        | Channel 1 ADC sourced by V(VB)                          |                     |         |
| 110        | Channel 1 ADC sourced by V(VBL1)                        |                     |         |
| 111        | Channel 1 ADC sourced by V(LDA1)                        |                     |         |

Table 118: ADC channel 1 source selection

| ILIM1 |   | Addr. 0x11; bit 7:0 | R/W 0xFF |
|-------|---|---------------------|----------|
| Code  | Function  |                     |          |
| 0x00  | Channel 1 overcurrent threshold set to the minimum current in APC mode (EACC1 = 0) or overcurrent protection disabled in ACC mode (EACC1 = 1) |                     |          |
| ...   | Channel 1 overcurrent threshold set to $l_{lim} = (\Delta I(LDA), max \cdot n \cdot k)$ , n from 0 to 255                                     |                     |          |
| 0xFF  | Channel 1 overcurrent threshold set to the maximum current  |                     |          |

Table 119: Overcurrent threshold configuration channel 1

| RMD1 |  | Addr. 0x12; bit 7:0 | R/W 0xFF |
|------|--|---------------------|----------|
| Code | Function   |                     |          |
| 0x00 | PLR1 resistor set to the minimum resistance  |                     |          |
| ...  | PLR1 resistor set to $Rmd = Rmd_0(1 + \frac{\Delta Rmd(\%)}{100})^{n+1}$ , n from 0 to 255 |                     |          |
| 0xFF | PLR1 resistor set to the maximum resistance  |                     |          |

Table 120: MDK resistor channel 1

| COMP1 |   | Addr. 0x13; bit 6:4 | R/W 011 |
|-------|---|---------------------|---------|
| Code  | Function  |                     |         |
| 000   | Minimum compensation current for the channel 1 regulator, slower response |                     |         |
| ...   |   |                     |         |
| 111   | Maximum compensation current for the channel 1 regulator, faster response |                     |         |

Table 121: Current compensation channel 1

| RLDAS1 |  | Addr. 0x13; bit 3:2 | R/W 00 |
|--------|--|---------------------|--------|
| Code   | Function                                       |                     |        |
| 00     | V(LDA1) > VBL1-0.5V sets the LDASAT1 alarm bit |                     |        |
| 01     | V(LDA1) > VBL1-0.8V sets the LDASAT1 alarm bit |                     |        |
| 10     | V(LDA1) > VBL1-1.0V sets the LDASAT1 alarm bit |                     |        |
| 11     | V(LDA1) > VBL1-1.2V sets the LDASAT1 alarm bit |                     |        |

Table 122: LDA saturation threshold selection channel 1

| REF1  |   | Addr. 0x13/14; bit 9:0 | R/W 0x000 |
|-------|---|------------------------|-----------|
| Code  | Function  |                        |           |
| 0x000 | Channel 1 regulator reference voltage set to minimum voltage  |                        |           |
| ...   | Channel 1 regulator reference voltage set to $V_{ref} = V_{ref_0}(1 + \frac{\Delta V_{ref}(\%)}{100})^{n+1}$ , n from 0 to 1023 |                        |           |
| 0x3FF | Channel 1 regulator reference voltage set to maximum voltage  |                        |           |

Table 123: Regulator voltage reference channel 1

| RACC1 |   | Addr. 0x1A; bit 0 | R/W 0 |
|-------|---|-------------------|-------|
| Code  | Function  |                   |       |
| 0     | Current range high for channel 1, Current sensor resistor (Rsensex) set to 2 kΩ |                   |       |
| 1     | Current range low for channel 1, Current sensor resistor (Rsensex) set to 16 kΩ |                   |       |

Table 124: Current range configuration channel 1

| ADFNS1 |  | Addr. 0x1A; bit 2 | R/W 0 |
|--------|--|-------------------|-------|
| Code   | Function   |                   |       |
| 0      | ADC measurement PLR1 after x2 level shifting (sense) |                   |       |
| 1      | ADC measurement MDK1 pad (force)                     |                   |       |

Table 125: ADC channel 1 force/sense selection

| CMES1 |  | Addr. 0x1A; bit 1 | R/W 0 |
|-------|--|-------------------|-------|
| Code  | Function                                       |                   |       |
| 0     | ADC current measurement disabled for channel 1 |                   |       |
| 1     | ADC current measurement enabled for channel 1  |                   |       |

Table 126: ADC current measurement for channel 1 selection

| CRNG1(1:0) |   | Addr. 0x1E; bit 1:0 | R/W 00 |
|------------|---|---------------------|--------|
| Code       | Function  |                     |        |
| 00         | Output current range from 0 to 750 mA, RACC1 = 0, k factor set to 750/750 = 1     |                     |        |
| 01         | Output current range from 0 to 100 mA, RACC1 = 0, k factor set to 100/750, = 0.13 |                     |        |
| 10         | Output current range from 0 to 25 mA, RACC1 = 0, k factor set to 25/750 = 0.03    |                     |        |
| 11         | Output current range from 0 to 9 mA, RACC1 = 0, k factor set to 9/750 = 0.012     |                     |        |
| 00         | Output current range from 0 to 90 mA, RACC1 = 1, k factor set to 750/750 = 1      |                     |        |
| 01         | Output current range from 0 to 12 mA, RACC1 = 1, k factor set to 100/750 = 0.13   |                     |        |
| 10         | Output current range from 0 to 3 mA, RACC1 = 1, k factor set to 25/750 = 0.03     |                     |        |
| 11         | Output current range from 0 to 1.1 mA, RACC1 = 1, k factor set to 9/750 = 0.012   |                     |        |

Table 127: Current range channel 1

| <b>EMNP1</b> |              | Addr. 0x1A; bit bit 3 | R/W 0 |
|--------------|--------------|-----------------------|-------|
| <b>EMNP2</b> |              | Addr. 0x1A; bit bit 7 | R/W 0 |
| Code         | Function     |                       |       |
| 0            | P-Laser Type |                       |       |
| 1            | M-Laser Type |                       |       |

Table 128: Laser Typ selection

| <b>EPUL1</b> |                      | Addr. 0x13; bit bit 7 | R/W 0 |
|--------------|----------------------|-----------------------|-------|
| <b>EPUL2</b> |                      | Addr. 0x18; bit bit 7 | R/W 0 |
| Code         | Function             |                       |       |
| 0            | Pulsed mode disabled |                       |       |
| 1            | Pulsed Mode enabled  |                       |       |

Table 129: Enable Pulse Mode

| <b>LINLOG1</b> |                                 | Addr. 0x1E; bit bit 3 | R/W 0 |
|----------------|---------------------------------|-----------------------|-------|
| <b>LINLOG2</b> |                                 | Addr. 0x1E; bit bit 7 | R/W 0 |
| Code           | Function                        |                       |       |
| 0              | Logarithmic 10 bit DAC selected |                       |       |
| 1              | Linear 10 bit DAC selected      |                       |       |

Table 130: Linear or Logarithmic reference selection

### Channel 2 configuration registers

| <b>EACC2</b> |   | Addr. 0x15; bit 0 | R/W 0 |
|--------------|---|-------------------|-------|
| Code         | Function  |                   |       |
| 0            | APC mode enabled for channel 2 (light power regulation)   |                   |       |
| 1            | ACC mode enabled for channel 2 (laser current regulation) |                   |       |

Table 131: Enable APC/ACC channel 2

| <b>ECIE2</b> |  | Addr. 0x15; bit 1 | R/W 0 |
|--------------|--|-------------------|-------|
| Code         | Function   |                   |       |
| 0            | External CI capacitor for channel 2 disconnected |                   |       |
| 1            | External CI capacitor for channel 2 connected    |                   |       |

Table 132: Enable external CI capacitor channel 2

| <b>DISP2</b> |                            | Addr. 0x15; bit 2 | R/W 0 |
|--------------|----------------------------|-------------------|-------|
| Code         | Function                   |                   |       |
| 0            | PLR enabled for channel 2  |                   |       |
| 1            | PLR disabled for channel 2 |                   |       |

Table 133: Disable PLR channel 2

| <b>DISC2</b> |  | Addr. 0x15; bit 3 | R/W 1 |
|--------------|--|-------------------|-------|
| Code         | Function                               |                   |       |
| 0            | Channel 2 can be enabled by pin EC2    |                   |       |
| 1            | Channel 2 cannot be enabled by pin EC2 |                   |       |

Table 134: Disable channel 2

| <b>ADCC2(2:0)</b> |   | Addr. 0x15; bit 7:5 | R/W 000 |
|-------------------|---|---------------------|---------|
| Code              | Function  |                     |         |
| 0xx               | Channel 2 ADC disabled                                  |                     |         |
| 100               | Channel 2 ADC sourced by V(MDK2), ADFNS2 = 1, CMES2 = 0 |                     |         |
| 100               | Channel 2 ADC sourced by V(PLR2), ADFNS2 = 0, CMES2 = 0 |                     |         |
| 100               | Channel 2 ADC sourced by ACC current sensor, CMES2 = 1  |                     |         |
| 101               | Channel 2 ADC sourced by V(VDD)                         |                     |         |
| 110               | Channel 2 ADC sourced by V(VBL2)                        |                     |         |
| 111               | Channel 2 ADC sourced by V(LDA2)                        |                     |         |

Table 135: ADC channel 2 source selection

| <b>ILIM2</b> |   | Addr. 0x16; bit 7:0 | R/W 0xFF |
|--------------|---|---------------------|----------|
| Code         | Function  |                     |          |
| 0x00         | Channel 2 overcurrent threshold set to the minimum current in APC mode (EACC2 = 0) or overcurrent protection disabled in ACC mode (EACC2 = 1) |                     |          |
| ...          | Channel 2 overcurrent threshold set to $I_{lim} = (\Delta I(LDA), max \cdot n \cdot k)$ , n from 0 to 255                                     |                     |          |
| 0xFF         | Channel 2 overcurrent threshold set to the maximum current  |                     |          |

Table 136: Overcurrent threshold configuration channel 2

| <b>RMD2</b> |   | Addr. 0x17; bit 7:0 | R/W 0xFF |
|-------------|---|---------------------|----------|
| Code        | Function  |                     |          |
| 0x00        | PLR2 resistor set to the minimum resistance   |                     |          |
| ...         | PLR2 resistor set to $R_{md} = R_{md0} (1 + \frac{\Delta R_{md}(\%)}{100})^{n+1}$ , n from 0 to 255 |                     |          |
| 0xFF        | PLR2 resistor set to the maximum resistance   |                     |          |

Table 137: MDK resistor channel 2

| <b>COMP2</b> |   | Addr. 0x18; bit 6:4 | R/W 011 |
|--------------|---|---------------------|---------|
| Code         | Function  |                     |         |
| 000          | Minimum compensation current for the channel 2 regulator, slower response |                     |         |
| ...          |   |                     |         |
| 111          | Maximum compensation current for the channel 2 regulator, faster response |                     |         |

Table 138: Current compensation channel 2

| <b>RLDAS2</b> |   | Addr. 0x18; bit 3:2 | R/W 00 |
|---------------|---|---------------------|--------|
| Code          | Function  |                     |        |
| 00            | V(LDA2) > VBL2-0.5 V sets the LDASAT2 alarm bit |                     |        |
| 01            | V(LDA2) > VBL2-0.8 V sets the LDASAT2 alarm bit |                     |        |
| 10            | V(LDA2) > VBL2-1.0 V sets the LDASAT2 alarm bit |                     |        |
| 11            | V(LDA2) > VBL2-1.2 V sets the LDASAT2 alarm bit |                     |        |

Table 139: LDA saturation threshold selection channel 2

| REF2  |  | Addr. 0x18/19; bit 9:0 | R/W 0x000 |
|-------|--|------------------------|-----------|
| Code  | Function   |                        |           |
| 0x000 | Channel 2 regulator reference voltage set to minimum voltage   |                        |           |
| ...   | Channel 2 regulator reference voltage set to $V_{ref} = V_{ref0}(1 + \frac{\Delta V_{ref}(\%)}{100})^{n+1}$ , n from 0 to 1023 |                        |           |
| 0x3FF | Channel 2 regulator reference voltage set to maximum voltage   |                        |           |

Table 140: Regulator voltage reference channel 2

| RACC2 |   | Addr. 0x1A; bit 4 | R/W 0 |
|-------|---|-------------------|-------|
| Code  | Function  |                   |       |
| 0     | Current range high for channel 2, Current sensor resistor (Rsensex) set to 2 kΩ |                   |       |
| 1     | Current range low for channel 2, Current sensor resistor (Rsensex) set to 16 kΩ |                   |       |

Table 141: Current range configuration channel 2

| ADFNS2 |  | Addr. 0x1A; bit 6 | R/W 0 |
|--------|--|-------------------|-------|
| Code   | Function   |                   |       |
| 0      | ADC measurement PLR2 after x2 level shifting (sense) |                   |       |
| 1      | ADC measurement MDK2 pad (force)                     |                   |       |

Table 142: ADC channel 2 force/sense selection

| CMES2 |  | Addr. 0x1A; bit 5 | R/W 0 |
|-------|--|-------------------|-------|
| Code  | Function                                       |                   |       |
| 0     | ADC current measurement disabled for channel 2 |                   |       |
| 1     | ADC current measurement enabled for channel 2  |                   |       |

Table 143: ADC current measurement for channel 2 selection

| CRNG2(1:0) |  | Addr. 0x1E; bit 5:4 | R/W 00 |
|------------|--|---------------------|--------|
| Code       | Function   |                     |        |
| 00         | Output current range from 0 to 750 mA, RACC2 = 0, k factor set to $750/750 = 1$    |                     |        |
| 01         | Output current range from 0 to 100 mA, RACC2 = 0, k factor set to $100/750 = 0.13$ |                     |        |
| 10         | Output current range from 0 to 25 mA, RACC2 = 0, k factor set to $25/750 = 0.03$   |                     |        |
| 11         | Output current range from 0 to 9 mA, RACC2 = 0, k factor set to $9/750 = 0.012$    |                     |        |
| 00         | Output current range from 0 to 90 mA, RACC2 = 1, k factor set to $750/750 = 1$     |                     |        |
| 01         | Output current range from 0 to 12 mA, RACC2 = 1, k factor set to $100/750 = 0.13$  |                     |        |
| 10         | Output current range from 0 to 3 mA, RACC2 = 1, k factor set to $25/750 = 0.03$    |                     |        |
| 11         | Output current range from 0 to 1.1 mA, RACC2 = 1, k factor set to $9/750 = 0.012$  |                     |        |

Table 144: Current range channel 2

| EMNP1 |              | Addr. 0x1A; bit bit 3 | R/W 0 |
|-------|--------------|-----------------------|-------|
| EMNP2 |              | Addr. 0x1A; bit bit 7 | R/W 0 |
| Code  | Function     |                       |       |
| 0     | P-Laser Type |                       |       |
| 1     | M-Laser Type |                       |       |

Table 145: Laser Typ selection

| EPUL1 |                      | Addr. 0x13; bit bit 7 | R/W 0 |
|-------|----------------------|-----------------------|-------|
| EPUL2 |                      | Addr. 0x18; bit bit 7 | R/W 0 |
| Code  | Function             |                       |       |
| 0     | Pulsed mode disabled |                       |       |
| 1     | Pulsed Mode enabled  |                       |       |

Table 146: Enable Pulse Mode

| LINLOG1 |                                 | Addr. 0x1E; bit bit 3 | R/W 0 |
|---------|---------------------------------|-----------------------|-------|
| LINLOG2 |                                 | Addr. 0x1E; bit bit 7 | R/W 0 |
| Code    | Function                        |                       |       |
| 0       | Logarithmic 10 bit DAC selected |                       |       |
| 1       | Linear 10 bit DAC selected      |                       |       |

Table 147: Linear or Logarithmic reference selection

### General configuration registers

| RDCO |  | Addr. 0x1B; bit 5:0 | R/W 0x02 |
|------|--|---------------------|----------|
| Code | Function   |                     |          |
| 0x00 | No current   |                     |          |
| ...  |  |                     |          |
| 0x3F | Typ. 130 μA (cf. <i>Electrical Characteristics No. D01</i> ) |                     |          |

Table 148: Digital current output register

| MERGE |   | Addr. 0x1B; bit 6 | R/W 0 |
|-------|---|-------------------|-------|
| Code  | Function  |                   |       |
| 0     | Channel 1 and 2 operate independently   |                   |       |
| 1     | Power transistor from channel 2 usable in parallel with channel 1, regulation made by channel 1 |                   |       |

Table 149: Channel combination

| MODE(1:0) |   | Addr. 0x1C; bit 1:0 | R/W 01 |
|-----------|---|---------------------|--------|
| Code      | Function  |                     |        |
| 00        | Not allowed   |                     |        |
| 01        | Chip set in operation mode (apply configuration, latch transparent) |                     |        |
| 10        | Chip set in configuration mode (hold previous configuration)        |                     |        |
| 11        | Not allowed   |                     |        |

Table 150: Configuration and operation mode

| <b>MOSCERR</b> |  | Addr. 0x1D; bit 0 | R/W 0 |
|----------------|--|-------------------|-------|
| Code           | Function   |                   |       |
| 0              | Oscillator error (watchdog) will be signaled at NCHK     |                   |       |
| 1              | Oscillator error (watchdog) will not be signaled at NCHK |                   |       |

Table 151: Oscillator watchdog error mask

| <b>MMONC</b> |  | Addr. 0x1D; bit 1 | R/W 1 |
|--------------|--|-------------------|-------|
| Code         | Function   |                   |       |
| 0            | MONC1 and MONC2 event will be signaled at NCHK     |                   |       |
| 1            | MONC1 and MONC2 event will not be signaled at NCHK |                   |       |

Table 152: Monitor channel 1 and 2 event mask

| <b>MLDASAT1</b> |  | Addr. 0x1D; bit 2 | R/W 1 |
|-----------------|--|-------------------|-------|
| Code            | Function                                   |                   |       |
| 0               | LDASAT1 event will be signaled at NCHK     |                   |       |
| 1               | LDASAT1 event will not be signaled at NCHK |                   |       |

Table 153: LDA saturation error mask channel 1

| <b>MLDASAT2</b> |  | Addr. 0x1D; bit 3 | R/W 1 |
|-----------------|--|-------------------|-------|
| Code            | Function                                   |                   |       |
| 0               | LDASAT2 event will be signaled at NCHK     |                   |       |
| 1               | LDASAT2 event will not be signaled at NCHK |                   |       |

Table 154: LDA saturation error mask channel 2

| <b>SOVT</b> |                                       | Addr. 0x1D; bit 4 | R/W 0 |
|-------------|---------------------------------------|-------------------|-------|
| Code        | Function                              |                   |       |
| 0           | No overtemperature event is simulated |                   |       |
| 1           | Overtemperature event simulated       |                   |       |

Table 155: Simulate overtemperature

| <b>SOVC1</b> |  | Addr. 0x1D; bit 5 | R/W 0 |
|--------------|--|-------------------|-------|
| Code         | Function                                       |                   |       |
| 0            | No Overcurrent event at channel 1 is simulated |                   |       |
| 1            | Overcurrent event at channel 1 simulated       |                   |       |

Table 156: Simulate overcurrent channel 1

| <b>SOVC2</b> |  | Addr. 0x1D; bit 6 | R/W 0 |
|--------------|--|-------------------|-------|
| Code         | Function                                       |                   |       |
| 0            | No overcurrent event at channel 2 is simulated |                   |       |
| 1            | Overcurrent event at channel 2 simulated       |                   |       |

Table 157: Simulate overcurrent channel 2

| <b>SOSCERR</b> |   | Addr. 0x1D; bit 7 | R/W 0 |
|----------------|---|-------------------|-------|
| Code           | Function                                      |                   |       |
| 0              | No oscillator error simulated                 |                   |       |
| 1              | Oscillator error simulated (watchdog timeout) |                   |       |

Table 158: Simulate oscillator error

### DESIGN REVIEW: Notes On Chip Functions

| iC-HTP Z, Z1 |                          |   |
|--------------|--------------------------|---|
| No.          | Function, Parameter/Code | Description and Application Notes   |
| 1            | Power-up                 | Supplying VBL1 or VBL2 before VB is over the power-up level is not permitted in iC-HTP Z1 since undesired laser spikes might be caused. |
| 2            | CHIPREV                  | For iC-HTP chip releases see Table 113.   |

Table 159: Notes on chip functions regarding iC-HTP chip release Z and Z1

| iC-HTP Y |                          |   |
|----------|--------------------------|---|
| No.      | Function, Parameter/Code | Description and Application Notes   |
| 1        | Power-up                 | Sporadically the register thermometer will not be updated with the temperature                  |
| 2        | LDASAT                   | Spec 102 Saturation detection threshold Conditions: RLDASDx = 00, VBL = 11 V Value: 0.2 to 1 mV |
| 3        | LDASAT                   | Spec 102 Saturation detection threshold Conditions: RLDASDx = 01, VBL = 11 V Value: up to 1.2 V |
| 4        | LDASAT                   | Spec 102 Saturation detection threshold Conditions: RLDASDx = 10, VBL = 11 V Value: up to 1.3 V |
| 5        | IVB                      | Spec 003 Power Supply Conditions: VBL = 11 V, High Temperature. Value: up to 5.2 mA             |
| 6        | CHIPREV                  | For iC-HTP chip releases see Table 113.   |

Table 160: Notes on chip functions regarding iC-HTP chip release Y

| iC-HTP X1 |                          |   |
|-----------|--------------------------|---|
| No.       | Function, Parameter/Code | Description and Application Notes   |
| 1         | DRDY                     | Data Ready Status Register for A/D Synchronisation. More information on page 29 |
| 2         | LINLOG                   | Logarithmic DA converter can be set as linear one. More information on page 28  |
| 3         | EPUL                     | Puls and Burst mode. More information on page 21                                |
| 4         | EMNP                     | Possibility of driving M-Typ Laser. More information on page 10                 |
| 5         | EOCx                     | Not Supported   |
| 6         | EXTTxx                   | Not Supported   |
| 7         | WK Mode                  | MRH has to be connected to VDD  |
| 8         | NSTBY                    | Vthlo, spec point 602 with VB = 2.8 V may be down to 0.45 V                     |
| 9         | CHIPREV                  | For iC-HTP chip releases see Table 113.   |

Table 161: Notes on chip functions regarding iC-HTP chip release X1

| iC-HTP W |                          |   |
|----------|--------------------------|---|
| No.      | Function, Parameter/Code | Description and Application Notes       |
| 1        | CHIPREV                  | For iC-HTP chip releases see Table 113. |

Table 162: Notes on chip functions regarding iC-HTP chip release W



# iC-HTP

## DUAL CW P-TYPE LASER DIODE DRIVER



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### REVISION HISTORY

| Rel. | Rel. Date <sup>†</sup> | Chapter | Modification    | Page |
|------|------------------------|---------|-----------------|------|
| A1   | 2015-06-19             |         | Initial release | all  |

| Rel. | Rel. Date <sup>†</sup> | Chapter                            | Modification   | Page      |
|------|------------------------|------------------------------------|--|-----------|
| B1   | 2017-03-20             | ELECTRICAL CHARACTERISTICS         | Item 4 + 5: Turn-off threshold updated   | 6         |
|      |                        | ELECTRICAL CHARACTERISTICS         | Item 110: V(MDK) updated   | 6         |
|      |                        | ELECTRICAL CHARACTERISTICS         | Item 114: I <sub>dc</sub> (LDA) typical values on LD <sub>Ax</sub> ACC mode current updated  | 7         |
|      |                        | ELECTRICAL CHARACTERISTICS         | Item 202: TK added   | 7         |
|      |                        | MICROCONTROLLER MODE               | Figure 10 added: NCHK behavior in MCU mode   | 21        |
|      |                        | SERIAL COMMUNICATION INTERFACES    | Figure 14: I2C timing updated  | 25        |
|      |                        | 10 BIT LINEAR A/D CONVERTER        | CRNG <sub>x</sub> and Mirror factor MFACT <sub>x</sub> added   | 28        |
|      |                        | REGISTER OVERVIEW                  | CHIPREV table updated  | 41        |
|      |                        | PARAMETERS                         | ILIM <sub>x</sub> = 0x00 disables OVC protection in ACC mode added   | 43, 45    |
|      |                        | PARAMETERS                         | CMES <sub>x</sub> added  | 43 ... 46 |
|      |                        | PARAMETERS                         | PDOVB1 and PDOVB2 in MERGE mode description updated  | 45        |
|      |                        | PARTICULAR REQUIREMENTS: iC-HTP Z1 | Special requirements for HTP_Z1 added: "Supplying VBL1 or VBL2 before VB is over the power-up level is not permitted in iC-HTP_Z1 since undesired laser spikes could be caused." | 50        |

| Rel. | Rel. Date <sup>†</sup> | Chapter                                   | Modification   | Page |
|------|------------------------|---|--|------|
| C1   | 2018-12-04             | ELECTRICAL CHARACTERISTICS                | Item 002: Conditions / limit updated                                 | 6    |
|      |                        | ELECTRICAL CHARACTERISTICS                | Item 004, 005: Min. limit updated                                    | 6    |
|      |                        | ELECTRICAL CHARACTERISTICS                | Item 108, 110 limits updated   | 6    |
|      |                        | ELECTRICAL CHARACTERISTICS                | Item 116 Min and max step defined (Logarithmic). New limit items.    | 7    |
|      |                        | ELECTRICAL CHARACTERISTICS                | Item 3xx conditions with LINLOG updated                              | 7    |
|      |                        | ELECTRICAL CHARACTERISTICS                | Item 605 limit updated   | 8    |
|      |                        | ELECTRICAL CHARACTERISTICS                | Item 702 conditions with DRDY updated                                | 8    |
|      |                        | ELECTRICAL CHARACTERISTICS                | Item 8xx added for pulse mode  | 8    |
|      |                        | ELECTRICAL CHARACTERISTICS                | Item B02 limit updated   | 8    |
|      |                        | LASER DIODE/LED TYPES AND OPERATION MODES | Description of Register EPNN for selection of M-Type laser           | 10   |
|      |                        | PULSED MODE                               | Description of Pulsed Mode added                                     | 21   |
|      |                        | 10 BIT LINEAR A/D CONVERTER               | Synchronisation procedure described. Register description RDDY added | 29   |
|      |                        | 10 BIT LOGARITHMIC D/A CONVERTER          | LINLOG register description added. (Linear Reference)                | 28   |
|      |                        | REGISTER OVERVIEW                         | EPUL1, EPUL2, LINLOG1, LINLOG2, EPNN1, EPNN2 new in register map     | 39   |
|      |                        | iC-WK MODE                                | Figures Updated. MRH to VDD  |      |

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| Rel. | Rel. Date <sup>‡</sup> | Chapter                                | Modification                           | Page       |
|------|------------------------|--|--|------------|
| D1   | 2020-07-10             | ELECTRICAL CHARACTERISTICS             | Item 001: VBLx added                   | 6          |
|      |                        | ELECTRICAL CHARACTERISTICS             | Item 002 updated                       | 6          |
|      |                        | ELECTRICAL CHARACTERISTICS             | Item 011 deleted                       | 6          |
|      |                        | ELECTRICAL CHARACTERISTICS             | Item 101: conditions updated           | 6          |
|      |                        | ELECTRICAL CHARACTERISTICS             | Item 105 updated                       | 6          |
|      |                        | ELECTRICAL CHARACTERISTICS             | Item 106, 107: conditions updated      | 6          |
|      |                        | ELECTRICAL CHARACTERISTICS             | Item 109 updated                       | 6          |
|      |                        | ELECTRICAL CHARACTERISTICS             | Item 111 updated                       | 7          |
|      |                        | ELECTRICAL CHARACTERISTICS             | Item 114: conditions updated           | 7          |
|      |                        | ELECTRICAL CHARACTERISTICS             | Item 116, 205 updated                  | 7          |
|      |                        | ELECTRICAL CHARACTERISTICS             | Item 501: conditions updated           | 7          |
|      |                        | ELECTRICAL CHARACTERISTICS             | Item 602 updated                       | 7          |
|      |                        | ELECTRICAL CHARACTERISTICS             | Item C03 updated                       | 8          |
|      |                        | ELECTRICAL CHARACTERISTICS             | Item D01, D02, D03: conditions updated | 9          |
|      |                        | ELECTRICAL CHARACTERISTICS             | Item E03 updated                       | 9          |
|      |                        | MICROCONTROLLER MODE                   | Minor corrections and additions        | 13, 18, 29 |
|      |                        | PULSED MODE                            | Minor corrections and additions        | 21         |
|      |                        | COMBINING BOTH CHANNELS                | Minor corrections and additions        | 22-24      |
|      |                        | 10 BIT LOGARITHMIC D/A CONVERTER       | Minor corrections and additions        | 28         |
|      |                        | DESIGN REVIEW: Notes On Chip Functions | Updated                                | 48         |

| Rel. | Rel. Date <sup>‡</sup> | Chapter                                   | Modification                     | Page |
|------|------------------------|---|----------------------------------|------|
| D2   | 2021-01-11             | LASER DIODE/LED TYPES AND OPERATION MODES | Figure 3 updated                 | 10   |
|      |                        | 10 BIT LINEAR A/D CONVERTER               | Hints on ADC readout added       | 30   |
|      |                        | STATUS AND PARAMETERS                     | Table 113: Chip revision W added | 43   |

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<sup>‡</sup> Release Date format: YYYY-MM-DD

# iC-HTP

## DUAL CW P-TYPE LASER DIODE DRIVER



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### ORDERING INFORMATION

| Type             | Package                   | Order Designation |
|------------------|---------------------------|-------------------|
| iC-HTP           | QFN28 5 mm x 5 mm         | iC-HTP QFN28-5x5  |
| Evaluation Board | 100 mm x 80 mm eval board | iC-HTP EVAL HTP1D |

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