iC-MNF 26-BIT NONIUS ENCODER WITH 3-CH. SAMPLING 14-BIT Sin/D INTERPOLATION

preliminary

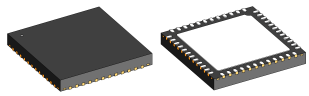
FEATURES

- Fast 14-bit sine-to-digital conversion within 2.3 µs
- Simultaneous sampling of 3 channels
- 2 or 3 track nonius calculation of up to 26 bit singleturn position
- BiSS C, SSI and SPI interface for position data
- Fail-safe RS422 transceiver for BiSS C, SSI
- Differential 1 Vpp sin/cos outputs to 100 Ω, short-circuit-proof
- Differential and single-ended PGA inputs for up to 200 kHz
- Input adaptation to current or voltage signals
- Adjustable signal conditioning for offset, amplitude and phase
- Input signal stabilization by LED or MR bridge current control
- Serial 2-wire interface to multiturn sensors (BiSS, SSI, 2-bit)
- Position preset function, selectable up/down code direction
- Signal and system monitoring with diagnosis memory
- Device setup via I/O interface (BiSS or SPI)
- CRC-protected configuration, OEM and USER data from external EEPROM (I2C)
- Reverse-polarity-proof and tolerant against faulty output wiring
- Power-good switch protecting the peripheral circuitry
- Single 5 V supply, operation from -40 to +125 °C

APPLICATIONS

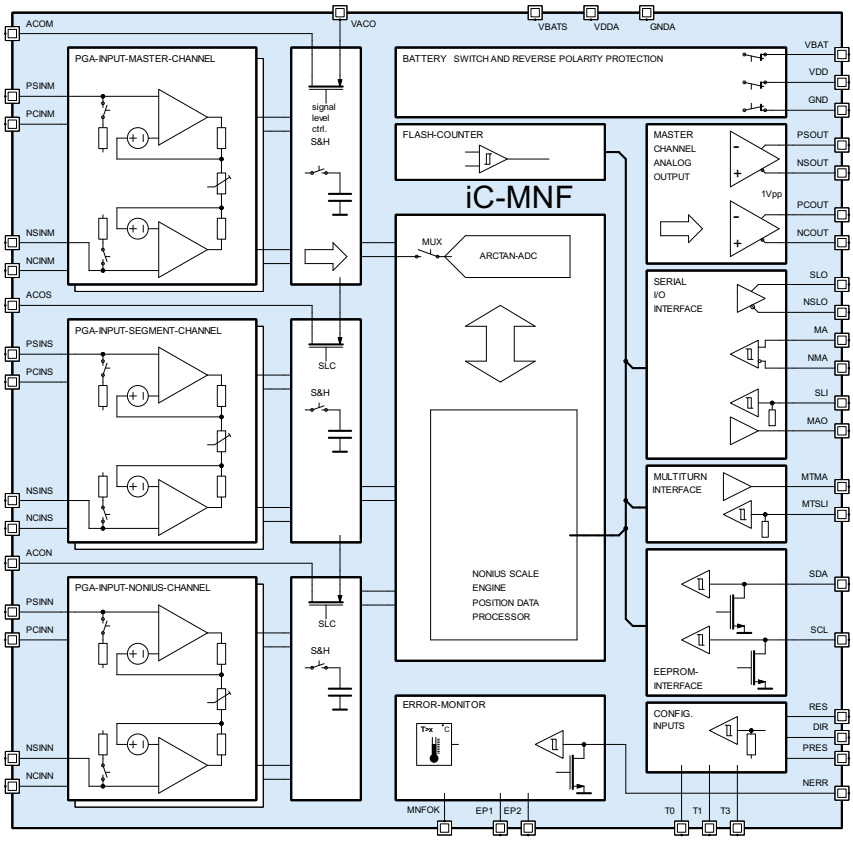
- Optical and magnetic position sensors
- Multi-channel sine-to-digital converter
- Singleturn and multiturn absolute encoders
- Linear scales for absolute position

PACKAGES



QFN48-7x7
7 mm x 7 mm x 0.9 mm
RoHS compliant

BLOCK DIAGRAM



DESCRIPTION

Encoder device iC-MNF is a 3-channel, simultaneous sampling sine-to-digital converter which interpolates sine/cosine sensor signals using a high precision SAR converter with a selectable resolution of up to 14 bits. Each input has a separate sample-and-hold stage which holds the track signal for the subsequent sequential A/D conversion. Various 2- and 3-track Vernier scale computations (after Nonius) and multiturn gear box synchronization modes can be configured for the calculation of high resolution angle positions; these computations permit angle resolutions of up to 26 bits.

The absolute angle position is output via the serial I/O interface with clock rates of up to 4 Mbit/s (SSI compatible), up to to 10 Mbit/s (BiSS C protocol) or up to to 8 Mbit/s (SPI protocol). For BiSS C and SSI point-to-point communication the required RS422 transceiver is integrated on the chip and has both a differential clock input and a differential line driver for data output.

Programmable instrumentation amplifiers with a selectable gain and offset and phase correction can be adjusted separately for each channel; these allow differential or single-ended input signals. At the same time the inputs can either be set to high impedance for voltage signals from magneto-resistive sensor bridges, for example, or to low impedance for adaptation and use with photosensors which provide current signals, for instance. This enables the device to be directly connected up to a number of different optical and magnetic sensors.

For the purpose of input signal stabilization the conditioned signals are fed into signal level controllers featuring current source outputs of up to 50 mA (master channel) and of up to 10 mA (for the nonius and segment channels each). These ACOx source pins either power the LEDs of an optical encoder or the magneto-resistive bridges of a magnetic encoder. If the control thresholds are reached this event can be released for alarm messaging using the serial I/O interface or the NERR output.

Both major chip functions and sensor errors are also monitored and can be enabled for alarm indication. In this manner typical sensor errors, such as signal loss due to wire breakage, short circuiting, dirt or aging, for example, can be signaled by alarms. Furthermore there are 3 error pins that can be configured to the error bit (SSI) or the error and warning bit (BiSS, SPI or ext. SSI) to report additional status-information to the Programmable Logic Controller (PLC).

The device features further digital encoder functions covering the correction of phase errors between the tracks, for example, or the zeroing or presetting of a specific position offset for data output. Using the BiSS/SSI master also integrated on the chip, position data from multiturn sensors, provided by a second iC-MNF, for example, can be read in and synchronized.

An internal digital 8 bit temperature sensor with adjustable error/alarm thresholds for excessive and low temperature is included in the device. The temperature data can be output reading a register or by enabling a second BiSS data channel.

To simplify implementation for battery buffered multiturn encoder designs, iC-MNF integrates switches and control logic to supply the external multiturn with an external battery or via pin VDD.

iC-MNF is protected against a reversed power supply voltage; the integrated supply switch for loads of up to 60 mA extends this protection to cover the overall system. The device is configured via an external EEPROM.

The device offered here is a multifunctional iC that contains integrated BiSS C interface components. The BiSS C process is protected by patent DE 10310622 B4 owned by iC-Haus GmbH. Users benefit from the open BiSS C protocol with a free license which is necessary when using the BiSS C protocol in conjunction with this iC.
Download the license at
www.biss-interface.com/bua

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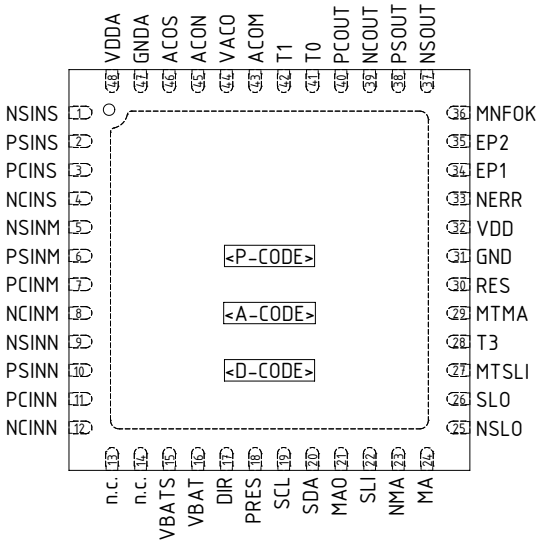
PACKAGING INFORMATION

PIN CONFIGURATION QFN48-7x7



PIN FUNCTIONS

No.	Name	Function
1	NSINS	Signal Input Sine - (Segment)
2	PSINS	Signal Input Sine + (Segment)
3	PCINS	Signal Input Cosine + (Segment)
4	NCINS	Signal Input Cosine - (Segment)
5	NSINM	Signal Input Sine - (Master)
6	PSINM	Signal Input Sine + (Master)
7	PCINM	Signal Input Cosine + (Master)
8	NCINM	Signal Input Cosine - (Master)
9	NSINN	Signal Input Sine - (Nonius)
10	PSINN	Signal Input Sine + (Nonius)
11	PCINN	Signal Input Cosine + (Nonius)
12	NCINN	Signal Input Cosine - (Nonius)
13	n.c. [2]	
14	n.c.	
15	VBATS	Battery Supply Voltage Sensor Output
16	VBAT [1, 4]	Battery Supply Voltage Input
17	DIR [4]	Code Direction Input
18	PRES [4]	Configurable Command Input

PIN FUNCTIONS

No.	Name	Function
19	SCL	EEPROM Interface, clock line
20	SDA	EEPROM Interface, data line
21	MAO [4]	I/O Interface, clock output (SPI Chip Select: NCS)
22	SLI [4]	I/O Interface, data input (SPI Data Input: MOSI)
23	NMA [1]	I/O Interface, clock input -
24	MA [1]	I/O Interface, clock input + (SPI Clock Input: SCLK)
25	NSLO [1]	I/O Interface, data output - (SPI Data Output: MISO)
26	SLO [1]	I/O Interface, data output +
27	MTSLI	Multiturn Interface, data input
28	T3 [4]	External Trigger Input
29	MTMA	Multiturn Interface, clock output
30	RES [4]	Reset Input
31	GND [1]	Ground
32	VDD [1, 6]	+4.5 to 5.5 V Supply Voltage Input
33	NERR [1]	Error Message Output, System Error Message Input
34	EP1 [4]	General Purpose I/O pin 1
35	EP2 [4]	General Purpose I/O pin 2
36	MNFOK	MNF OK Output
37	NSOUT [1]	Analog Output Sine - (Master)
38	PSOUT [1]	Analog Output Sine + (Master)
39	NCOUT [1]	Analog Output Cosine - (Master)
40	PCOUT [1]	Analog Output Cosine + (Master)
41	T0	Calibration Signal Output
42	T1 [5]	Calibration Signal Output
43	ACOM [1]	Signal Level Controller Outp. (Master)
44	VACO [1, 3, 6]	+4.5 to 5.5 V Signal Level Controller Supply Input
45	ACON [1]	Signal Level Ctrl. Output (Nonius)
46	ACOS [1]	Signal Level Ctrl. Output (Segment), Reference Voltage In/Out VREFin
47	GNDA	Sub-System Ground Output
48	VDDA [6]	Sub-System Supply Output and Internal Analog Supply Voltage
	BP [7]	Backside Paddle

IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes), <D-CODE> = date code (subject to changes)

[1] Pin is immune against faulty output or supply connection.

[2] Pin numbers marked n.c. are not connected.

[3] Connecting pin VACO to VDD is mandatory.

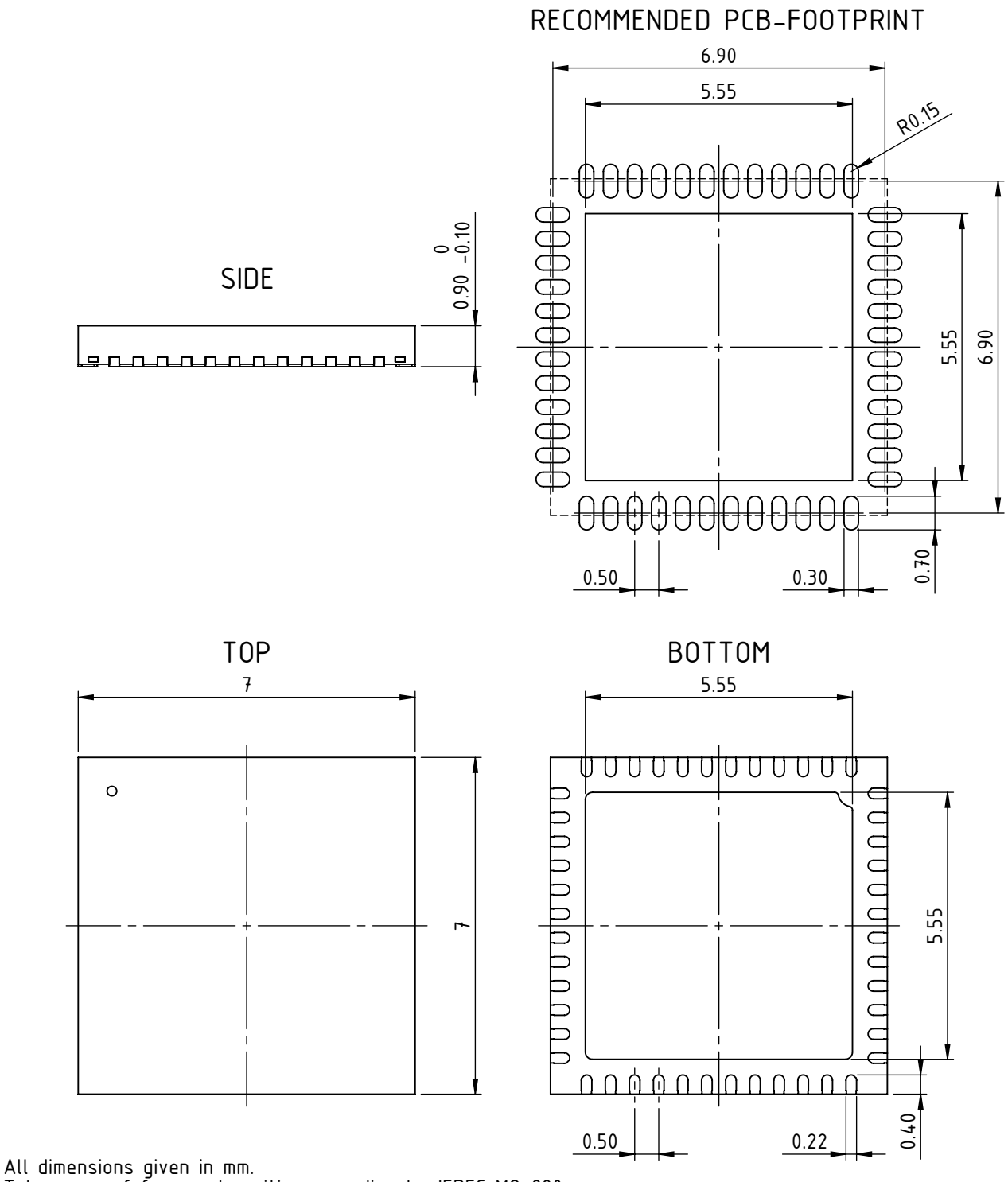
[4] It is generally recommended to connect unused inputs to GNDA via a resistor (e.g. 10 kΩ), with the exception of pin VBAT (connect GNDA directly).

[5] Pin T1 is used to calibrate the chip's bias current. Connect a pull-down resistor of 5 kΩ ±1 % from T1 to GNDA for the measurement (see Figure 14).

[6] Connect bypass capacitor(s) of about 100 nF with up to 1 µF in parallel close to the chip's supply terminals.

[7] To improve the heat dissipation connect the backside paddle to an extended copper area connected to GNDA. Avoid any current flow across the paddle. The heat distribution can be supported by connecting further PCB layers using *thermal vias*. If those need to be placed below the paddle, prefer blind vias.

PACKAGE DIMENSIONS QFN48-7x7



All dimensions given in mm.
Tolerances of form and position according to JEDEC MO-220.

drb_qfn48-7x7-3_pack_1, 8:1

ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these ratings device damage may occur.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	V()	Voltage at VDD, GND, NSLO, SLO, NERR, PSOUT, NSOUT, PCOUT, NCOUT, VACO, VBAT	referenced to GND	-6	6	V
G002	V()	Voltage at MA, NMA	referenced to GND	-9	14	V
G003	V()	Pin-to-Pin Voltage between VDD, GND, NSLO, SLO, NERR, PSOUT, NSOUT, PCOUT, NCOUT, VACO, VBAT			6	V
G004	V()	Voltage at NSINS, PSINS, PCINS, NCINS, NSINM, PSINM, PCINM, NCINM, NSINN, PSINN, PCINN, NCINN, DIR, PRES, SCL, SDA, MAO, SLI, MTSLI, RES, MTMA, EP1, EP2, MNFOK, T3, T0, T1, ACOM, ACON, ACOS, GNDA, VDDA, VBATS	V() < V(VDD) + 0.3 V	-0.3	6	V
G005	I(VDD)	Current in VDD		-100	400	mA
G006	I()	Current in VDDA, GNDA, PSOUT, NSOUT, PCOUT, NCOUT		-70	70	mA
G007	I()	Current in PSINM, NSINM, PCINM, NCINM, PSINS, NSINS, PCINS, NCINS, PSINN, NSINN, PCINN, NCINN, DIR, PRES, SCL, SDA, MAO, SLI, T3, RES, NERR, T0, T1, EP1, EP2, MNFOK, VBAT, VBATS		-20	20	mA
G008	I()	Current in SLO, NSLO, VACO		-120	120	mA
G009	I()	Current in MA, NMA		-0.6	1	mA
G010	I(ACOM)	Current in ACOM		-100	20	mA
G011	I()	Current in ACOS, ACON		-50	20	mA
G012	Vd()	ESD Susceptibility at all pins	HBM 100 pF discharged through 1.5 kΩ		2	kV
G013	Tj	Junction Temperature		-40	150	°C
G014	Ts	Storage Temperature Range		-40	150	°C

THERMAL DATA

Operating conditions: VDD = 5 V ±10 %

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range	package QFN48-7x7	-40		125	°C
T02	Rthja	Thermal Resistance Chip to Ambient	QFN48-7x7 surface mounted to PCB according to JEDEC 51		30		K/W

All voltages are referenced to analog ground GNDA unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = VACO = 5 V ±10 %, Tj = -40...140 °C,
IBP calibrated to 200 µA, reference point analog ground GNDA (GND for digital I/O pins, VDD and VACO) unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VDD, VACO	Permissible Supply Voltage		4.5		5.5	V
002	VBAT	Permissible Battery Supply		2		4	V
003	I(VDD)	Supply Current in VDD	Tj = 27 °C, no load		60	70	mA
004	I(VDDA)	Permissible Load Current at VDDA	V(VDDA) > 4 V	-60		0	mA
005	Vc()hi	Clamp Voltage hi (all pins with the exception of MA, NMA)	Vc()hi = V() − VDD, I() = 1 mA	0.4		1.5	V
006	Vc()hi	Clamp Voltage hi MA, NMA	Vc()hi = V() − VDD, I() = 10 mA	12.5		16	V
007	Vc()lo	Clamp Voltage lo (all pins with the exception of MA, NMA)	I() = -1 mA	-1.5		-0.2	V
008	Vc()lo	Clamp Voltage lo at MA, NMA	I() = -10 mA	-17		-10	V
Signal Conditioning and Inputs: PSINx, NSINx, PCINx, NCINx (x = M, S, N)							
101	Vin()sig	Permissible V-Mode Input Voltage	ISM_x = 0x4 ISM_x = 0xC, DCPOS = 0x1	0.75 -0.1		VDDA − 1.5 VDDA + 0.1	V V
102	Iin()	V-Mode Input Current	ISM_x = 0x4	-100		100	nA
103	Rin()	V-Mode Input Resistance	vs. VREFin, Tj = 27 °C, ISM_x = 0xC	16.4	20	23.6	kΩ
104	R2()	Effective V-Mode Resistor	vs. VREFin, Tj = 27 °C, ISM_x = 0xC		5		kΩ
105	Iin()sig	Permissible I-Mode Input Current	ISM_x = 0x0..0x3; DCPOS = 0x0 DCPOS = 0x1	 -10 10		 -300 300	 µA µA
106	SCR()	Permissible Signal Contrast Ratio	ratio of Iin()pk vs. Iin()dc	0.125		1	
107	Rin()	I-Mode Input Resistance	Tj = 27 °C, vs. VREFin; ISM_x = 0x0 ISM_x = 0x1 ISM_x = 0x2 ISM_x = 0x3	 1.2 1.8 2.5 3.5	 1.7 2.5 3.5 4.9	 2.2 3.2 4.5 6.3	 kΩ kΩ kΩ kΩ
108	R2()	Effective I-Mode Resistor	Tj = 27 °C, vs. VREFin; ISM_x = 0x0 ISM_x = 0x1 ISM_x = 0x2 ISM_x = 0x3		 1.6 2.3 3.2 4.6		 kΩ kΩ kΩ kΩ
109	TCRin	Temperature Coefficient Rin			0.15		%/K
110	VREFI	Internal Reference Voltage	DCPOS = 0x1 DCPOS = 0x0	1.35 2.25	1.5 2.5	1.65 2.75	V V
112	Vin()diff	Recommended Differential Input Voltage	Vin()diff = V(PSINx) − V(NSINx), Vin()diff = V(PCINx) − V(NCINx); ISM_x = 0x4 ISM_x = 0xC	 20 80	 	 1000 4000	 mVpp mVpp
113	Vcore()	Recommended Internal Signal Level	GF * GC * Vin()diff		6		Vpp
114	GF, GC	Selectable Gain Factors	ISM_x = 0x0..0x4 ISM_x = 0xC	6 1.5		300 75	
115	ΔGFdiff	Differential Fine Gain Error		-0.5		1.5 (evtl. 1)	LSB
116	ΔGFSabs	Absolute Fine Gain Accuracy		-20		20	LSB
117	ΔGCabs	Absolute Coarse Gain Accuracy	referenced to coarse gain range	-8		8	%

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = VACO = 5 V ±10 %, Tj = -40...140 °C,
IBP calibrated to 200 µA, reference point analog ground GNDA (GND for digital I/O pins, VDD and VACO) unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
118	VOScal	Offset Calibration Range	measured at output, source V(ACOx) = 3 V, REFVOS_x = 0x0; ORS_x/ORC_x = 0x0 ORS_x/ORC_x = 0x1 ORS_x/ORC_x = 0x2 ORS_x/ORC_x = 0x3		 ±450 ±900 ±2700 ±5400		 mV mV mV mV
119	VOScal2	Offset Calibration Range	measured at output, source VDC_{hi} = 125 mV, REFVOS_x = 0x1; ORS_x/ORC_x = 0x0 ORS_x/ORC_x = 0x1 ORS_x/ORC_x = 0x2 ORS_x/ORC_x = 0x3		 ±375 ±750 ±2250 ±4500		 mV mV mV mV
120	VOScal3	Offset Calibration Range	measured at output, source V025, REFVOS_x = 0x2; ORS_x/ORC_x = 0x0 ORS_x/ORC_x = 0x1 ORS_x/ORC_x = 0x2 ORS_x/ORC_x = 0x3		 ±750 ±1500 ±4500 ±9000		 mV mV mV mV
121	VOScal4	Offset Calibration Range	measured at output, source VDC_{lo} = 125 mV, REFVOS_x = 0x3; ORS_x/ORC_x = 0x0 ORS_x/ORC_x = 0x1 ORS_x/ORC_x = 0x2 ORS_x/ORC_x = 0x3		 ±375 ±750 ±2250 ±4500		 mV mV mV mV
122	ΔVOSdiff	Differential Linearity Error of Offset Correction		-0.5		0.5	LSB
123	ΔVOSint	Integral Linearity Error of Offset Correction		-100		100	LSB
124	PHIcal	Phase Correction Range	sine vs. cosine signal		±10.4		°
125	ΔPHIdiff	Differential Linearity Error of Phase Correction		-0.25		0.25	LSB
126	ΔPHIint	Integral Linearity Error of Phase Correction		-20		20	LSB
127	fin()max	Permissible Input Frequency	angle accuracy better 8 bit	200			kHz
128	fhc()	Input Amplifier Cut-off Frequency (-3 dB)	COMP_x = inv[GF_x(10:7)]	250			kHz
Signal Level Controller: ACOM							
401	Vs()hi	Saturation Voltage hi	Vs()hi = V(VACO) - V(); ACOR_M(1:0) = 0x0, I() = -5 mA ACOR_M(1:0) = 0x1, I() = -10 mA ACOR_M(1:0) = 0x2, I() = -25 mA ACOR_M(1:0) = 0x3, I() = -50 mA			 1 1 1 1	 V V V V
402	Isc()hi	Short-circuit Current hi	V() = 0...V(VACO) – 1 V; ACOR_M(1:0) = 0x0 ACOR_M(1:0) = 0x1 ACOR_M(1:0) = 0x2 ACOR_M(1:0) = 0x3	 -9.5 -19 -46 -85	 -7 -14.5 -36 -73	 -5 -10 -25 -50	 mA mA mA mA
403	Ilk()	Residual Current	With Reversed Supply VACO = GND = 0 V, V(VBAT) > 2 V, * V(ACOM) < 4 V * V(ACOM) < 2 V			50 2 0.05	µA µA µA
404	Tctrl	Control Time Constant	control to sine square		1.6		ms
405	Vpk()avg	Controlled Differential S/C Signal Amplitude (averaged)	square control: ACOT_M(1:0) = 0x1, ACOCTR_M calibrated, Op.mode ANA_M	2.925	3	3.075	V
406	Vt()min	Signal Monitoring AM_Min	referred to Vscq() = SQRT of $[V(PSOUT) - V(NSOUT)]^2$ + $[V(PCOUT) - V(NCOUT)]^2$		40		%

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = VACO = 5 V ±10 %, Tj = -40...140 °C,
IBP calibrated to 200 µA, reference point analog ground GNDA (GND for digital I/O pins, VDD and VACO) unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
407	Vt()max	Signal Monitoring AM_Max	referred to Vscq(), see 406		135		%
408	It()min	Control Monitoring ACM_Min	referenced to range ACOR_M()		3		%Isc
409	It()max	Control Monitoring ACM_Max	referenced to range ACOR_M()		90		%Isc
410	t()set	Settling time	t()set after tbusy()cfg (D07)		3		ms
Signal Level Controller: ACOx (x = S, N)							
501	Vs()hi	Saturation Voltage hi	Vs()hi = V(VACO) – V(); ACOR_x = 0x0, I() = -5 mA ACOR_x = 0x1, I() = -10 mA			 1 1	 V V
502	Isc()hi	Short-circuit Current hi	V() = 0...V(VACO) – 1 V; ACOR_x = 0x0 ACOR_x = 0x1	 -9.5 -19	 -7 -14.5	 -5 -10	 mA mA
503	Ilk()	Residual Current with Reverse Polarity				50	µA
504	Tctrl	Control Time Constant	control to sine square		1.6		ms
505	Vpk()avg	Controlled Differential S/C Signal Amplitude (averaged)	square control: ACOT_x(1:0) = 0x1, ACOCTR_x calibrated, operating mode ANA_x	2.925	3	3.075	V
506	Vt()min	Signal Monitoring AN_Min, AS_Min	referred to Vscq() = SQRT of $[V(PSOUT) - V(NSOUT)]^2 + [V(PCOUT) - V(NCOUT)]^2$		40		%
507	Vt()max	Signal Monitoring AN_Max, AS_Max	referred to Vscq(), see 506		135		%
508	It()min	Control Monitoring ACN_Min, ACS_Min	referenced to range ACOR_x()		3		%Isc
509	It()max	Control Monitoring ACN_Max, ACS_Max	referenced to range ACOR_x()		90		%Isc
510	Vin(ACOS)	Permissible Ref. Input Voltage at ACOS	CVREF = 0x3	0.5		VDDA – 2	V
511	t()set	Settling time	t()set after tbusy()cfg (D07)		3		ms
512	Vout(ACOS)	Output Voltage at ACOS	CVREF = 0x02 (output of internal reference voltage VREFI), relative to VREFI; I(ACOS) = –150...+150 µA	95	100	105	%
513	Rin(ACOS)	Input Resistance at ACOS	CVREF = 0x03 (input for external refernce voltage), REFVOS_M = REFVOS_S = REFVOS_N = 0x1 or 0x3	6.6	9	11.7	kΩ
Sample-&-Hold Stage, Signal Filter and Sine-To-Digital Conversion (x = M, S, N)							
601	fc1()	Cut-off Frequency of M/S/N Channel Signal Filter (-3 dB lowpass filter)	ENF(1) = 0x1; fin (master channel) < 20 Hz fin (master channel) > 1300 Hz		 4 300		 kHz kHz
602	amax	Permissible Angle Acceleration for 3(2) track nonius calculation	ENF(1) = 0x1		1000		$Mrad/s^2$
603	AAabs	Absolute Angular Accuracy	Used bit length UBL_x = 0x0C: 13 bit		±2		LSB
604	AAR	Repeatability			±1		LSB
605	tcnv	Conversion Time (1 Channel)	CNVSPD = 0x1: Used bit length UBL_M, or UBL_x with SYNC_x = 0x0 (with x = S, N): ≤ 14 bit ≤ 11 bit ≤ 8 bit ≤ 5 bit UBL_x with SYNC_x = 0x1 (with x = S, N) CNVSPD = 0x2: Used bit length UBL_M, or UBL_x with SYNC_x = 0x0 (with x = S, N): ≤ 14 bit ≤ 11 bit ≤ 8 bit ≤ 5 bit UBL_x with SYNC_x = 0x1 (with x = S, N)		 1.8 1.35 1.05 0.85 1.35 2.4 1.8 1.4 1.0 1.8		 µs µs µs µs µs µs µs µs µs µs

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = VACO = 5 V ±10 %, Tj = -40...140 °C,
IBP calibrated to 200 µA, reference point analog ground GNDA (GND for digital I/O pins, VDD and VACO) unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
606	trec()	Recovery Time Sampling-to-Sampling	termination of calculation and synchronization (Nonius or MT modes) to follow-up S&H trigger			1.65	µs
Analog Line Driver Outputs: PSOUT, NSOUT, PCOUT, NCOUT							
701	Vout()	Output Amplitude	RLdiff = 100 Ω, VDD = 4.5 V, DC level = VDD/2			300	mV
702	Vpk()	Differential Output Amplitude with Signal Level Control by ACOM	square control: ACOT_M(1:0) = 01, ACOCTR_M calibrated, Op.mode normal	475	500	525	mV
703	fc2()	Cut-off Frequency of Line Driver Signal Filter (-3 dB low-pass filter)	ENF(0) = 0x1; fin (master channel) < 20 Hz fin (master channel) > 1300 Hz		 4 300		 kHz kHz
704	fc3()	Cut-off Frequency of Line Driver (-3 dB)	CL = 500 pF, Vpp = 0.5 V, ENF(0) = 0x0	500			kHz
705	Voffs()	Offset Voltage		-8		8	mV
706	Isc()hi	Short-circuit Current hi	V() = GND	-40	-20	-15	mA
707	Isc()lo	Short-circuit Current lo	V() = VDD	15	20	40	mA
708	SR()	Slew Rate	RLdiff = 100 Ω, CL = 25 pF		5		V/µs
709	Ilk()	Tristate Leakage Current	tristate or reversed supply	-50		50	µA
711	Rout()	Output Impedance	Op.Mode ANA_M, ANA_N, ANA_S	1	2	5	kΩ
712	fout()cal	Permissible Output Frequency During Calibration	Op.Mode ANA_M, ANA_N, ANA_S; CL = 200 pF			2	kHz
Bias Current Source and Reference Voltages							
801	IBP	Bias Current Source	IBP calibrated to 200 µA	92.5	100	107.5	%
802	VPAH	Reference Voltage VPAH	referenced to GNDA	48	50	52	%VDD
803	V05	Reference Voltage V05	referenced to GNDA	460	512	570	mV
805	VBG	Bandgap Voltage	referenced to GNDA		1.24		V
Power-Down-Reset							
901	VDDon	Turn-on Threshold VDD (power on release)	increasing voltage VDD	3.9	4.1	4.4	V
902	VDDoff	Turn-off Threshold VDD (power down reset)	decreasing voltage VDD	3.4	3.8	4.0	V
903	VDDhys	Hysteresis	VDDhys = VDDon – VDDoff	200			mV
904	tready()cfg	Operation Startup Time	includes tbusy()cfg (D07, FAST_I2C = 0x1); MODE_MT = 0x0 MODE_MT ≠ 0x0		 15.1 25		 ms ms
Clock Oscillator							
A01	fosc	Clock Frequency		17.8	20.6	23.7	MHz
Battery Switch and Reverse Polarity Protection: VDDA, GNDA, VBAT, VBATS, VDD							
B01	Vs()	VDDA Supply-Switch Drop-Off Voltage	Vs() = V(VDD) - V(VDDA); unloaded			140	mV
B02	Ron()	VDDA Supply-Switch On-Resistance	VDD to VDDA			5	Ω
B03	Vs()	GNDA Ground-Switch Drop-Off Voltage	Vs() = V(GNDA) - V(GND); unloaded			110	mV
B04	Ron()	GNDA Ground-Switch On-Resistance	GND to GNDA			5	Ω
B05	Vt()act1	Battery Switch Activation Threshold to VDD	Vt()act1 = V(VDD) - V(VBAT), increasing voltage at VDD vs. VBAT, (note V(VDD) > 2 V is relevant) no reverse polarity	0		300	mV
B06	Vt()act2	Battery Switch Activation Threshold to VBAT	Vt()act2 = V(VDD) - V(VBAT), decreasing voltage at VDD vs. VBAT (note V(VBAT) > 2 V is relevant) no reverse polarity	-300		0	mV
B07	Vhys()act	Battery Switch Hysteresis	Vhys()act = Vt()act1 - Vt()act2	200		450	mV

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = VACO = 5 V ±10 %, Tj = -40...140 °C,
IBP calibrated to 200 µA, reference point analog ground GNDA (GND for digital I/O pins, VDD and VACO) unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
B08	Rs()	Battery Switch On-Resistance to VDD	Vt()act1 exceeded			100	Ω
B09	Rs()	Battery Switch On-Resistance to VBAT	Vt()act2 exceeded			200	Ω
B10	Ilk()	Leakage Current at VBAT	battery switch to VDD activated battery switch to VBAT activated, I(VBATS) = 0		 0.25	0.1 1.0	µA µA
B11	I(VBATS)	Permissible Load Current at VBATS	battery switch to VDD activated battery switch to VBAT activated			6.5 1	mA mA
B12	I()	Permissible Load Current at VDDA		-60			mA
B13	I()	Permissible Load Current into GNDA				60	mA
B14	Ilk(VDD)	Residual Current with Reverse Polarity		-0.5		0.5	mA
8 bit Digital Temperature Monitoring							
C01	TEMP	Digital Temperature Representation	Tj = -40 °C Tj = 20 °C Tj = 100 °C		0x18 0x54 0xA4		
C02	ΔT	Measurement Resolution			1		°C/LSB
C03	T_{os}	Measurement Offset Error	Tj = -40...140 °C OFF_TEM = 0x00	 -15		 15	°C
C04	INL	Integral Linearity Error	Tj = -40...140 °C	-3		3	LSB
C05	DNL	Differential Linearity Error	Tj = -40...140 °C	-1		1	LSB
C06	Tr	Refresh Rate			66		µs
EEPROM Interface: SCL, SDA							
D01	Vs()lo	Saturation Voltage lo	I() = 4 mA			450	mV
D02	Isc()lo	Short-circuit Current lo		4		70	mA
D03	Vt()hi	Input Threshold Voltage hi				2	V
D04	Vt(lo)	Input Threshold Voltage lo		0.8			V
D05	Vt()hys	Input Hysteresis	Vt(hys) = Vt()hi − Vt()lo	100	250		mV
D06	fclk(SCL)	Clock Frequency	during startup FAST_I2C = 0x0 FAST_I2C = 0x1 in normal operating mode FAST_I2C = 0x0 FAST_I2C = 0x1	 34 140	 46 185 62.5 250		 kHz kHz kHz kHz
D07	tbusy()cfg	Duration of EEPROM Read Out of Configuration Data During Startup	error free EEPROM access FAST_I2C = 0x0 FAST_I2C = 0x1		 24.4 7.1	 33 10	 ms ms
I/O Interface: RS422 Line Driver Outputs SLO, NSLO							
E01	Vs()hi	Saturation Voltage hi	Vs() = VDD − V(); SLO_SC = 0x0, I() = -20 mA SLO_SC = 0x1, I() = -4 mA			 1100 500	 mV mV
E02	Vs()lo	Saturation Voltage lo	SLO_SC = 0x0, I() = 20 mA SLO_SC = 0x1, I() = 4 mA			900 500	mV mV
E03	Isc()hi	Short-circuit Current hi	V() = 0 V; SLO_SC = 0x0 SLO_SC = 0x1	 -45 -12		 -20 -4	 mA mA
E04	Isc()lo	Short-circuit Current lo	V() = VDD SLO_SC = 0x0 SLO_SC = 0x1	 30 6		 65 18	 mA mA
E05	Ilk()tri	Tristate Leakage Current				100	µA
E06	tr()	Rise Time hi	RL = 100 Ω in-between SLO and NSLO; SLO_SC = 0x0; tr() = t(10 %→90 %)			20	ns

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = VACO = 5 V ±10 %, Tj = -40...140 °C,
IBP calibrated to 200 µA, reference point analog ground GNDA (GND for digital I/O pins, VDD and VACO) unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
E07	tf()	Fall Time lo	RL = 100 Ω in-between SLO and NSLO; SLO_SC = 0x0; tr() = t(10 %→90 %)			20	ns
E08	Ilk()	Residual Current with Reverse Polarity		-100		100	µA
I/O Interface: RS422 Line Receiver MA, NMA							
F01	Vin()	Permissible Input Voltage		-7		12	V
F02	Rin()	Input Resistance	Rin()= (V() - Voc()) / I(), inverse pin = GND	15	23	32	kΩ
F03	Vhys()	Differential Input Hysteresis	Vhys() = (V(MA) - V(NMA)) / 2	50		200	mV
F04	Vt()hi	Input Threshold Voltage hi at MA	pin NMA open, Voc() must be held at NMA			2	V
F05	Vt()lo	Input Threshold Voltage lo at MA	pin NMA open, Voc() must be held at NMA	0.8			V
F06	Voc()	Open Circuit Voltage	pins MA, NMA open	0.85	1.4	1.95	V
F07	Vt()Hys	Input Hysteresis	pin NMA open, Voc() must be held at NMA, Vt()hys = Vt()hi - Vt()lo	90	150		mV
F08	fclk()	Permissible Clock Frequency: SSI protocol	MODE_SER = 0x2 to 0x7, 0x9 to 0xE MODE_ST = 0x0A to 0x17, 0x1A to 0x1F			4	MHz
F09	fclk()	Permissible Clock Frequency: BiSS protocol	MODE_SER = 0x0 to 0x1			10	MHz
F10	fclk()	Permissible Clock Frequency: SPI protocol	MODE_SER = 0x8			8	MHz
F11	tp(MA-SLO)	Propagation Delay: MA edge vs. SLO output	RL(SLO/NSLO) = 120 Ω	10		50	ns
F12	tbusy_s	Delay of BiSS start bit (Single Cycle Data) for counted modes	MODE_SER = 0x0 to 0x1; Counted modes: MODE_ST = 0x00 to 0x05 MODE_ST = 0x06 to 0x09; 1 track MODE_ST = 0x06 to 0x09; 2 track MODE_ST = 0x06 to 0x09; 3 track MODE_ST = 0x0A to 0x17	 0.70µs + 1*tcnv + $\frac{2}{fclk}$ 0.70µs + 1*tcnv + $\frac{2}{fclk}$ 0.75µs + 2*tcnv + $\frac{2}{fclk}$ 0.80µs + 3*tcnv + $\frac{2}{fclk}$ $\frac{2}{fclk}$			µs
F13	tbusy_s	Delay of BiSS start bit (Single Cycle Data) for calculated modes	MODE_SER = 0x0 to 0x1; Calculated modes: MODE_ST = 0x18 to 0x19, 1 track MODE_ST = 0x18 to 0x19, 2 track MODE_ST = 0x18 to 0x19, 3 track MODE_ST = 0x1A to 0x1F	 0.70µs + 1*tcnv + $\frac{2}{fclk}$ 0.75µs + 2*tcnv + $\frac{2}{fclk}$ 0.80µs + 3*tcnv + $\frac{2}{fclk}$ $\frac{2}{fclk}$			µs
F14	tbusy_r	Delay of BiSS start bit (Register Access)	with read access to EEPROM			2	ms
F15	tidle	Interface Blocking Time	powering up without EEPROM			8	ms
I/O Interface: Clock Line Input/Output MAO							
G01	Vs()hi	Saturation Voltage hi	MAO as output, Vs()hi = VDD − V(), I() = -4 mA			450	mV
G02	Vs()lo	Saturation Voltage lo	MAO as output, I() = 4 mA			450	mV
G03	Isc()hi	Short-circuit Current hi	MAO as output	-85		-30	mA
G04	Isc()lo	Short-circuit Current lo	MAO as output	20		70	mA
G05	Vt()hi	Threshold Voltage hi	MAO as input			2	V
G06	Vt()lo	Threshold Voltage lo	MAO as input	0.8			V
G07	Vt()Hys	Hysteresis	MAO as input, Vt()hys = Vt()hi - Vt()lo	150	250		mV
G08	Ipd()	Pull-down Current	MAO as input, V() = 0.8 V...VDD	4	30	75	µA
External Trigger Pin: T3							
H01	Vt()hi	Input Threshold Voltage hi				2	V

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = VACO = 5 V ±10 %, Tj = -40...140 °C,
IBP calibrated to 200 µA, reference point analog ground GNDA (GND for digital I/O pins, VDD and VACO) unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
H02	Vt()lo	Input Threshold Voltage lo		0.8			V
H03	Vt()hys	Input Hysteresis		150	250		mV
H04	Ipd()	Input-Pull-Down-Current	V() = 0.8 V...VDD	4	30	75	µA
I/O Interface: Input SLI							
J01	Vt()hi	Input Threshold Voltage hi				2	V
J02	Vt()lo	Input Threshold Voltage lo		0.8			V
J03	Vt()hys	Input Hysteresis		150	250		mV
J04	Ipd()	Input Pull-down Current	V() = 0.8 V...VDD	4	30	75	µA
Digital Inputs: DIR, PRES, RES							
K01	Vt()hi	Input Threshold Voltage hi				2	V
K02	Vt()lo	Input Threshold Voltage lo		0.8			V
K03	Vt()hys	Input Hysteresis		150	250		mV
K04	Ipd()	Input Pull-down Current	V() = 0.8 V...VDD	4	30	75	µA
K05	tblank()	Filter Time		16		20	µs
Error Message Input/Output: NERR, MNFOK							
L01	Vs()lo	Saturation Voltage lo	I() = 4 mA			450	mV
L02	Isc()lo	Short-circuit Current lo		4		70	mA
L03	Vt()hi	Input Threshold Voltage hi				2	V
L04	Vt()lo	Input Threshold Voltage lo		0.8			V
L05	Vt()hys	Input Hysteresis	Vt(hys) = Vt()hi - Vt()lo	100	250		mV
L06	Ipu()	Input Pull-up Current at NERR	V() = 0... VDD - 1 V DLS = 0x0	-750	-300	-60	µA
L07	Ilk()	Residual Current with Reverse Polarity		-100		100	µA
L08	R()pd	Pull-Down Resistor at MNFOK	referenced to GNDA	200	500	800	kΩ
L10	Vs()hi	Saturation Voltage hi at MNFOK	Vs()hi = VDD - V(), I() = 0 µA		100		mV
L11	Ron	MNFOK On-Resistance hi at MNFOK	from chip release MNF_Y1 on: I() = 100 µA	2.5		6	kΩ
Multiturn Interface: MTMA, MTSLI							
M01	Vt()hi	Input Threshold Voltage hi	Input func. of MTMA (MODE_MT = 0x8)			2	V
M02	Vt()lo	Input Threshold Voltage lo	Input func. of MTMA (MODE_MT = 0x8)	0.8			V
M03	Vt()hys	Input Hysteresis	Input func. of MTMA (MODE_MT = 0x8)	150	250		mV
M04	Ipd()	Input Pull-down Current	V() = 0.8 V...VDD	4	30	75	µA
M05	Vs()hi	Saturation Voltage hi at MTMA	Vs()hi = VDD - V(), I() = 4 mA			450	mV
M06	Vs()lo	Saturation Voltage lo at MTMA	I() = 4 mA			450	mV
M07	Isc()hi	Short-circuit Current hi at MTMA		-85		-30	mA
M08	Isc()lo	Short-circuit Current lo at MTMA		20		70	mA
M09	fclk()	SSI Clock Frequency at MTMA	MODE_MT = 0x2 to 0x7 SLOW_MT = 0x0 SLOW_MT = 0x1		125 31.25		kHz kHz
M10	fclk()	BiSS Clock Frequency at MTMA	MODE_MT = 0x1 SLOW_MT = 0x0 SLOW_MT = 0x1		1 0.125		MHz MHz
M11	t_{frame}	Max. BiSS Data Frame Duration	MODE_MT = 0x1			1	ms
M12	t_{wait}	MT Data Check Interval	MODE_MT = 0x1 to 0x8, CHK_MT = 0x1		8		ms
M13	t_{wait}	MT Retry Wait Time on Startup	MODE_MT = 0x1 to 0x7, MT_ERR = 0x1 during Startup		1		ms
General Purpose Digital I/O: EP1, EP2							
N01	Vt()hi	Threshold Voltage hi	EP1, EP2 as input			2	V
N02	Vt()lo	Threshold Voltage lo	EP1, EP2 as input	0.8			V
N03	Vt()hys	Input Hysteresis	EP1, EP2 as input, Vt()hys = Vt()hi - Vt()lo	150	250		mV

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = VACO = 5 V ±10 %, Tj = -40...140 °C,
IBP calibrated to 200 µA, reference point analog ground GNDA (GND for digital I/O pins, VDD and VACO) unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N04	Ipd()	Pull-down Current at EP1, EP2	V() = 0.8 V...VDD	4	30	75	µA
N05	Vs()hi	Saturation Voltage hi at EP1, EP2 as Outputs	Vs()hi = VDD - V(), I() = -4 mA			450	mV
N06	Vs()lo	Saturation Voltage lo at EP1, EP2 as Outputs	I() = 4 mA			450	mV
N07	Isc()hi	Short-circuit Current hi	EP1, EP2 as Outputs	-85		-30	mA
N08	Isc()lo	Short-circuit Current lo	EP1, EP2 as Outputs	20		70	mA
N09	tblank()	Filter Time		16		20	µs

OPERATING REQUIREMENTS: Multiturn Interface

Operating conditions: VDD = 5 V ±10 %, Ta = -40...125 °C,
IBP calibrated for fosc = 20 MHz, reference point GNDA (GND for digital I/O pins), unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
Multiturn SSI Interface (Figure 1, MODE_MT = 0x2-0x7)						
I001	T_{MTMA}	Clock Period	SLOW_MT = 0x0	8		µs
			SLOW_MT = 0x1	32		µs
I002	t_sMD	Setup Time: Data valid before MTMA lo→hi		50		ns
I003	t_hMD	Hold Time: Data stable after MTMA lo→hi		0		ns
I004	t_{out}	Timeout		> T_{MTMA}		
I005	t_{wait}	MT Data Check Interval	CHK_MT = 0x1	see Elec. Char. M12		
		MT Retry Wait Time on Startup	MT_ERR = 0x1 during Startup	see Elec. Char. M13		
Multiturn BiSS Interface (Figure 2, MODE_MT = 0x1)						
I006	T_{MTMA}	Clock Period	SLOW_MT = 0x0	1		µs
			SLOW_MT = 0x1	8		µs
I007	t_sMD	Setup Time: Data valid before MTMA lo→hi		50		ns
I008	t_hMD	Hold Time: Data stable after MTMA lo→hi		0		ns
I009	t_{out}	Timeout		20		µs
I010	t_{frame}	Max. BiSS Data Frame Duration		see Elec. Char. M11		
I011	t_{wait}	MT Data Check Interval	CHK_MT = 0x1	see Elec. Char. M12		
		MT Retry Wait Time on Startup	MT_ERR = 0x1 during Startup	see Elec. Char. M13		

Multiturn: Timing SSI

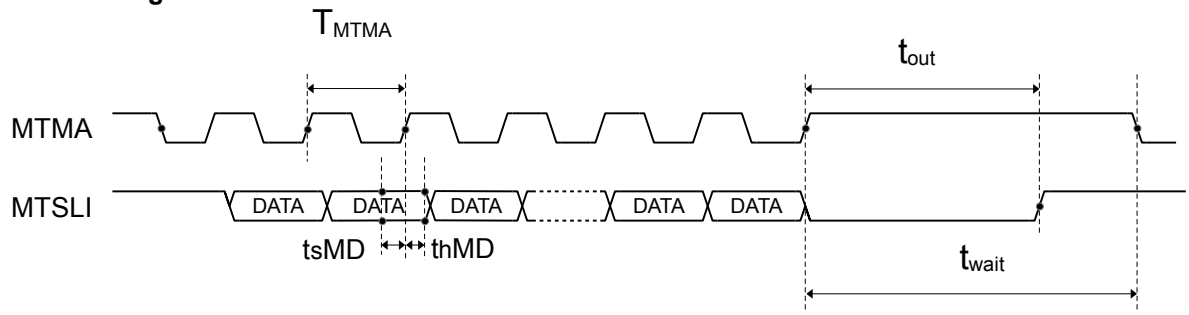


Figure 1: Timing multiturn interface (MODE_MT = 0x2-0x7)

Multiturn: Timing BiSS

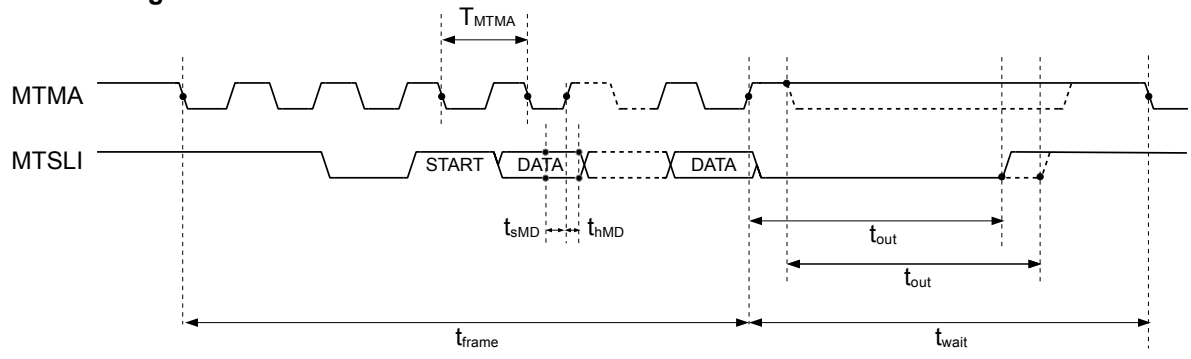


Figure 2: Timing multiturn interface (MODE_MT = 0x1)

OPERATING REQUIREMENTS: I/O Interface

Operating conditions: VDD = 5 V ±10 %, Ta = -40...125 °C,
IBP calibrated for fosc = 20 MHz, reference point GNDA (GND for digital I/O pins), unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
SSI Protocol (Figure 3, 4; MODE_SER = 0x2-0x7, 0x9-0xE)						
I101	T_{MAS}	Permissible Clock Period at pin MA		250	2 x t_{out}	ns
I102	t_{out}	SSI Timeout	NTOA = 1, fixed NTOA = 0, adaptive, (not recommended)	16000 80	24000 24000	ns ns
I103	t_{MASh}	Clock Signal Hi Level Duration		25	t_{out}	ns
I104	t_{MASl}	Clock Signal Lo Level Duration		25	t_{out}	ns
I105	t_{cycle}	Permissible Frame Repetition		*)	indefinite	
BiSS C Protocol (Figure 5, 6; MODE_SER = 0x0-0x1)						
I106	T_{MAS}	Permissible Clock Period at pin MA		100	20000	ns
I107	T_{CLK}	sampling frequency: 1/TCLK of pin MA		89	122	ns
I108	t_{out}	Slave Timeout	NTOA = 0, adaptive, typ. t_{init} NTOA = 1, fixed	1.5*T_{MAS} 16000	1.5*T_{MAS} +4*T_{CLK} 24000	ns ns
I109	t_{MASh}	Clock Signal Hi Level Duration		25	20000	ns
I110	t_{MASl}	Clock Signal Lo Level Duration		25		ns
I111	t_{busy}	Minimum Data Output Delay	MODE_ST = 0x0A-0x0F, 0x1A-0x1F MA lo→hi until SLO lo→hi	2x T_{MAS}		µs
I112	t_{busy}	Maximum Data Output Delay: Example for 19-bit ST data from 3-track nonius or multiturn calculation	MODE_ST = 0x00...0x05, fclk(MA) = 10 MHz, UBL_M = 13 bit, UBL_x = 3 bit, SYNC_x = 0x1 (x = S,N), see Figure 5	2.4		µs
I113	t_{busy}	Maximum Data Output Delay: Example for 19-bit ST data from 3-track nonius or multiturn calculation	MODE_ST = 0x06...0x09, fclk(MA) = 10 MHz, UBL_M = 13 bit, UBL_x = 3 bit, SYNC_x = 0x1 (x = S,N), see Figure 5	5.5		µs
I114	t_{busy}	Maximum Data Output Delay: Example for 39-bit ST data from 3-track interpolation without synchronization	MODE_ST = 0x18, fclk(MA) = 10 MHz, UBL_M 13 bit, UBL_x 13 bit, SYNC_x = 0x0 (x = S,N), see Figure 5	6.2		µs
I115	t_{cycle}	Permissible Frame Repetition		*)	indefinite	
SPI Protocol (Figure 7; MODE_SER = 0x8)						
I116	t_{C1}	Permissible Clock Period	see Elec. Char. No.:F10	1/fclk()		ns
I117	t_{W1}	Wait Time: between NCS lo → hi and NCS hi → lo		500		ns
I118	t_{S1}	Setup Time: NCS lo before SCLK lo → hi		50		ns
I119	t_{P1}	Propagation Delay: MISO stable after NCS hi → lo			50	ns
I120	t_{P2}	Propagation Delay: MISO high impedance after NCS lo → hi			50	ns
I121	t_{H1}	Hold Time: NCS lo after SCLK lo → hi	valid for SPI mode 3	30		ns
I122	t_{S2}	Setup Time: MOSI stable before SCLK lo → hi		30		ns
I123	t_{H2}	Hold Time: MOSI stable after SCLK lo → hi		20		ns
I124	t_{P3}	Propagation Delay: MISO stable after MOSI change	mode: repeating MOSI on MISO		50	ns
I125	t_{P4}	Propagation Delay: MISO stable after SCLK hi → lo	mode: sending data MISO		60	ns
I126	t_{H3}	Hold Time: NCS lo after SCLK hi → lo	valid for SPI mode 0	50		ns
I127	t_{W2}	Wait Time: SCLK stable after NCS lo → hi		500		ns

OPERATING REQUIREMENTS: I/O Interface

Operating conditions: VDD = 5 V ±10 %, Ta = -40...125 °C,
IBP calibrated for fosc = 20 MHz, reference point GNDA (GND for digital I/O pins), unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
I128	t_{L1}	Clock Signal lo Level Duration		25		ns
I129	t_{L2}	Clock Signal hi Level Duration		25		ns

Note: *) Allow t_{out} to elapse.

Timing SSI

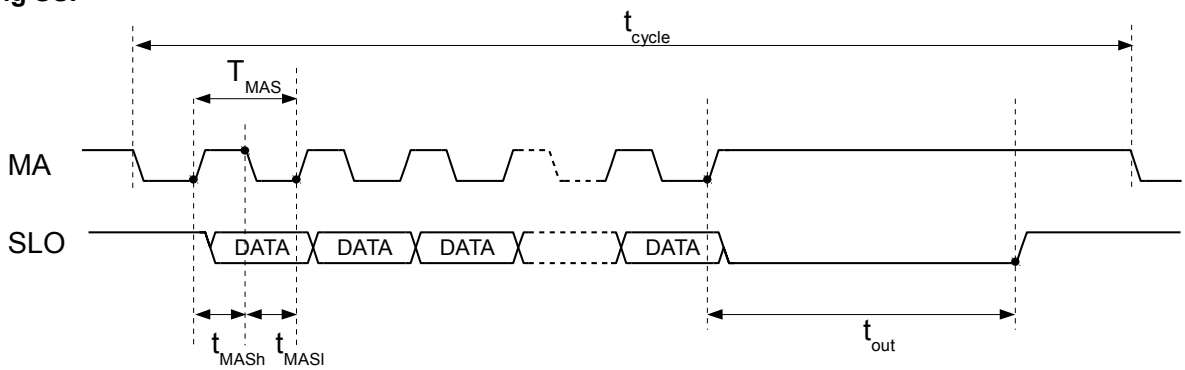


Figure 3: I/O Interface timing with SSI protocol (MODE_SER = 0x2-0x7, 0x9-0xE)

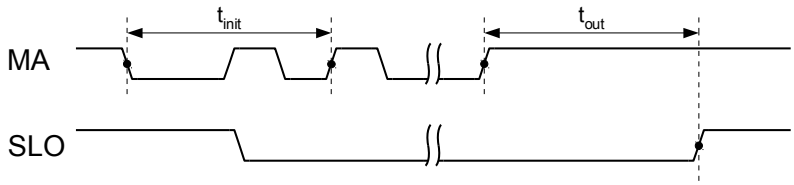


Figure 4: Timeout SSI interface adaptive (NTOA = 0)

Timing BiSS

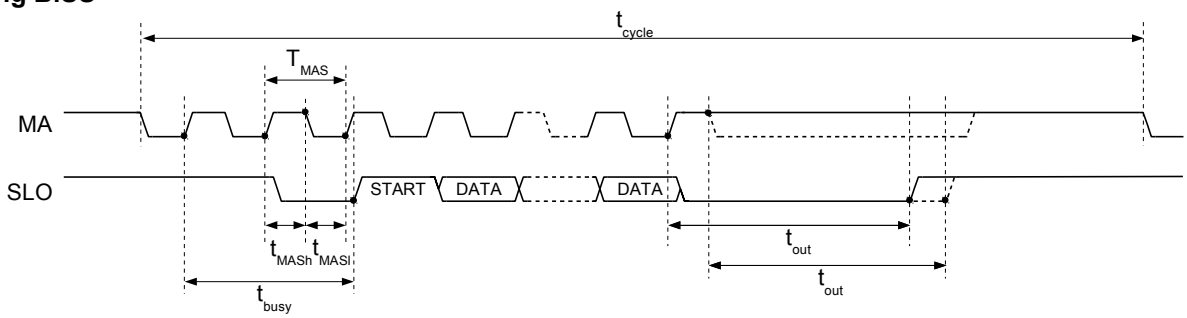


Figure 5: I/O Interface timing with BiSS C protocol (MODE_SER = 0x0-0x1)

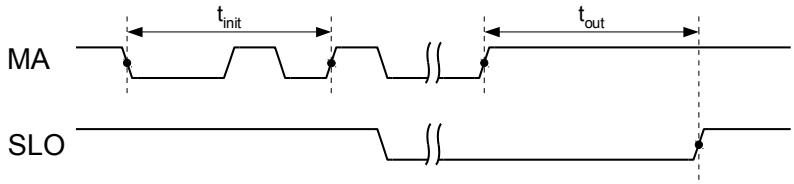


Figure 6: Timeout BiSS interface adaptive (NTOA = 0)

Timing SPI

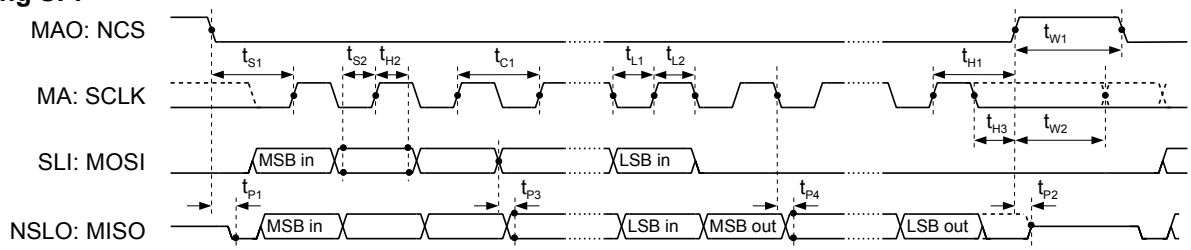


Figure 7: I/O Interface timing with SPI protocol (MODE_SER = 0x8)

CONFIGURATION PARAMETERS

Analog Parameters (valid for all channels)

CFGIBP: Bias Trimming (p. 36)
DCPOS: Input Current Polarity (p. 30)
ENF: Noise Filter Enable (p. 36)
NDBF: Noise Filter Frequency Adaption Mode (p. 36)
CVREF: VREF Source Selection (p. 30)
FGHI: Test Setting Noise Filter (p. 36)
LGSH: Test Setting Sample and Hold Gain (p. 104)
DISCURLIM: Test Setting Noise Filter (p. 36)

Signal Conditioning
x = M, S, N (for master, segment, nonius channel)

ACOCON_x: Signal Level Control: Current (p. 35)
ACOCTR_x: Signal Level Control: Current (p. 35)
ACOR_x: Signal Level Control: Range (p. 34)
ACOT_x: Signal Level Control: Op. Mode (p. 34)
ACO_HYS_x: Signal Level Control: Hysteresis (p. 34)
GR_x: Gain Range (p. 30)
GFS_x: Gain Factor Sine (p. 31)
GFC_x: Gain Factor Cosine (p. 31)
COMP_x: S/C Frequency Response (p. 31)
MPS_x: Center Potential Sine (p. 32)
MPC_x: Center Potential Cosine (p. 32)
OFC_x: Offset Factor Cosine (p. 33)
ORC_x: Offset Range Cosine (p. 32)
OFS_x: Offset Factor Sine (p. 33)
ORS_x: Offset Range Sine (p. 32)
PH_x: S/C Phase Correction (p. 33)
REFVOS_x: Offset Reference Source (p. 32)
ISM_x: Input Signal Mode (p. 29)

Operating Modes
x = M, S, N (for master, segment, nonius channel)

TRACMODE: Op. Mode Parameter (p. 28)
TEST: Op. Mode Parameter (p. 28)
BYP_x: Bypass Switch (p. 28)

Sine-To-Digital Conversion

MODE_ST: S/D Conversion Mode (p. 67)
EUS: Enable Upscale (p. 69)
UBL_M: Bit Length Master (p. 65)
UBL_N: Bit Length Nonius (p. 65)
SYNC_N: Synchronization of Nonius Track (p. 65)
UBL_S: Bit Length Segment (p. 65)
SYNC_S: Synchronization of Segment Track (p. 65)
FRQ_TH: Signal Frequency Monitoring (p. 71)
SPO_N: Offset Nonius Track (p. 72)
SPO_S: Offset Segment Track (p. 72)
CNVSPD: Conversion Speed (p. 65)

I/O Interface

MODE_SER: Interface Protocol (p. 44)
NTOA: Adaptive Timeout (p. 46)
DL_ST: ST Data Length (p. 44)
DL_MT: MT Data Length (p. 44)
CDL_MT: Change MT Data Length (p. 45)
ECDL_MT: Enable CDL_MT Changes (p. 45)
DL_ZERO: Additional Zero-Bits after ST Data (p. 45)
ROT: Inversion of Code Direction (p. 45)
PAR_SSI: Parity Bit SSI (p. 49)
CID_SCD: CRC Start Value (p. 46)
ELC: Sign-of-Life Counter (p. 48)
ETS: Additional Data Channel For Temperature Data (p. 85)
CHIP_REL: Chip Release (p. 60)

Analog and Digital Driver Settings

DRVDIS: Sin/Cos output driver disable (p. 37)
DRVMASK: Sin/Cos output driver disable masking (p. 37)
SLO_SC: SLO/NSLO Driver Short-Circuit Current (p. 37)
SLO_LS: SLO/NSLO Driver Output Mode (p. 37)
DLS: Driver Output Mode MTMA, EP1, EP2 (p. 37)

Temperature Sensor Settings

OFF_TEM: Temperature Offset Correction (p. 84)
ETH_TEM: Temperature High Warning and Error Thresholds (p. 84)
ETL_TEM: Temperature Low Error Thresholds (p. 84)

Command And Status Register

STATUS: Status Register (p. 86)
MNF_CMD: Implemented Commands (p. 93)
PROT_CMD: Disable Command Register (p. 94)
AUTORES: Automatic Reset Function (p. 96)

Error And Warning Bit

CFGEW0: Error And Warning Bit Config. (p. 90)
CFGEW1: Error And Warning Bit Config. (p. 91)
CFGEW2: Error And Warning Bit Config. (p. 91)
EWM: Error And Warning Bit Output mode (p. 91)
E2EPR: Diagnosis Memory Enable (p. 88)
C2EPR: Save Counter Check Errors to EEPROM (p. 87)
RR_STAT: Readout Resets Status (p. 86)

MT Interface

MODE_MT: MT Interface Operation Mode (p. 73)
DL_EXT_MT: MT Data Length (p. 74)
SBL_MT: MT Synch. Bit Length (p. 74)
CHK_MT: Period Counter Verification (p. 75)
ROT_MT: Inversion of Code Direction External Multiturn (p. 73)
SPO_MT: Offset External Multiturn (p. 74)
SLOW_MT: Reduction of I/O Clock Frequency External Multiturn (p. 73)
WI2C_MT: Delay Start of External MT Check In Case Of Ongoing I2C Communication (p. 76)

Preset Function

OFFS_ST: Position Offset for ST Data Output (p. 63)
PRES_ST: Preset Value for ST Data Output (p. 63)
OFFS_MT: Position Offset for MT Data Output (p. 64)
PRES_MT: Preset Value for MT Data Output (p. 64)
PRES_MODE: Preset Mode (p. 95)
FPRES_MT: Force MT Preset (p. 95)

Configurable I/O Pins

RES_MODE: Configurable Modes for RES Pin (p. 97)
NENDIR_P: Disable DIR Pin (p. 45)
PRES_CONF: Configurable Commands to Input Pin PRES (p. 98)
EP1_IO: Pin EP1: Input/Output (p. 91)
EP1_HL: Pin EP1: Polarity (p. 92)
EP2_IO: Pin EP2: Input/Output (p. 91)
EP2_HL: Pin EP2: Polarity (p. 92)

EEPROM Interface

FAST_I2C: I2C Fast Mode (p. 39)
CRC_CFG: Configuration Data Check Sum Config (p. 40)
CRC_OFF: Offset Data Check Sum Offset (p. 40)
CRC_PRES: Preset Data Check Sum Preset (p. 40)
PROT_E2P: Register Access Control (p. 61)

BiSS/Profile-ID

DEV_ID: BiSS Device ID (p. 27)
MFG_ID: BiSS Manufacturer ID (p. 27)
EDS: EDSBANK configuration (p. 27)
EDSBANK: BiSS EDSBANK (p. 27)
PRO_ID0: BiSS Profile ID Position Data Channel (p. 27)
PRO_ID1: BiSS Profile ID Temperature Data Channel (p. 27)
SER_NO: BiSS Serial Number (p. 27)
PROT_INS: Disable BiSS commands 0 and 1 (p. 47)

REGISTER ASSIGNMENTS (EEPROM)

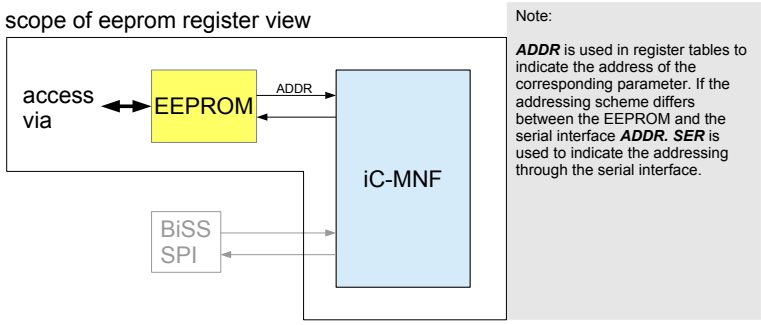


Figure 8: Scope of register mapping EEPROM

The abbreviation *Addr.* is used in the register tables of this specification to indicate the address of the corresponding parameter. If the addressing scheme differs between the EEPROM and the serial I/O interface *Addr. SER* is used to indicate the addressing when using the serial I/O interface.

OVERVIEW								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Signal conditioning master channel								
0x00	GFS_M(7:0)							
0x01	OFS_M(3:0)				FAST_I2C	GFS_M(10:8)		
0x02		OFS_M(10)	OFS_M(9:4)					
0x03	GFC_M(7:0)							
0x04	OFC_M(3:0)					GFC_M(10:8)		
0x05		OFC_M(10)	OFC_M(9:4)					
0x06	PH_M(7:0)							
0x07	COMP_M(3:0)						PH_M(9)	PH_M(8)
0x08	MPS_M(7:0)							
0x09	MPC_M(3:0)						MPS_M(9:8)	
0x0A			MPC_M(9:4)					
0x0B	BYP_M		REFVOS_M(1:0)		ORC_M(1:0)		ORS_M(1:0)	
0x0C		GR_M(2:0)			ISM_M(3:0)			
0x0D	ACO_HYS_M(1:0)		ACOT_M(1:0)		ACOR_M(1:0)		FGHI	DISCURLIM
0x0E			ACOCON_M(5:0)					
0x0F				ACOCTR_M(4:0)				

Table 1: Register map master channel (EEPROM)

OVERVIEW								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Signal conditioning segment channel								
0x10	GFS_S(7:0)							
0x11	OFS_S(3:0)					GFS_S(10:8)		
0x12		OFS_S(10)	OFS_S(9:4)					
0x13	GFC_S(7:0)							
0x14	OFC_S(3:0)					GFC_S(10:8)		
0x15		OFC_S(10)	OFC_S(9:4)					
0x16	PH_S(7:0)							
0x17	COMP_S(3:0)						PH_S(9)	PH_S(8)
0x18	MPS_S(7:0)							
0x19	MPC_S(3:0)						MPS_S(9:8)	
0x1A			MPC_S(9:4)					
0x1B	BYP_S	DCPOS	REFVOS_S(1:0)		ORC_S(1:0)		ORS_S(1:0)	
0x1C		GR_S(2:0)			ISM_S(3:0)			
0x1D	ACO_HYS_S(1:0)		ACOT_S(1:0)		NHYS	ACOR_S	CVREF(1:0)	
0x1E			ACOCON_S(5:0)					
0x1F				ACOCTR_S(4:0)				

Table 2: Register map segment channel (EEPROM)

OVERVIEW								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Signal conditioning nonius channel								
0x20	GFS_N(7:0)							
0x21	OFS_N(3:0)					GFS_N(10:8)		
0x22		OFS_N(10)	OFS_N(9:4)					
0x23	GFC_N(7:0)							
0x24	OFC_N(3:0)					GFC_N(10:8)		
0x25		OFC_N(10)	OFC_N(9:4)					
0x26	PH_N(7:0)							
0x27	COMP_N(3:0)						PH_N(9)	PH_N(8)
0x28	MPS_N(7:0)							
0x29	MPC_N(3:0)						MPS_N(9:8)	
0x2A			MPC_N(9:4)					
0x2B	BYP_N		REFVOS_N(1:0)		ORC_N(1:0)		ORS_N(1:0)	
0x2C		GR_N(2:0)			ISM_N(3:0)			
0x2D	ACO_HYS_N(1:0)		ACOT_N(1:0)		LGSH	ACOR_N		
0x2E			ACOCON_N(5:0)					
0x2F				ACOCTR_N(4:0)				

Table 3: Register map nonius channel (EEPROM)

OVERVIEW								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Digital Parameters								
0x30	TRACMODE(2:0)			NDBF	ENF(1:0)		AUTORES(1:0)	
0x31	OPTEST(1:0)		TEST(5:0)					
0x32	NENDIR_P	DLS	SLO_SC	SLO_LS	CNVSPD(1:0)		EP2_IO	EP1_IO
0x33	DRVMASK(1:0)		DRVDIS(1:0)		EUS	EDS	PAR_SSI	NTOA
0x34	SPO_S(5:0)						0	0
0x35	SPO_S(13:6)							
0x36	SPO_N(5:0)						0	0
0x37	SPO_N(13:6)							
0x38	UBL_S(3:0)				UBL_M(3:0)			
0x39	FRQ_TH(1:0)		SYNC_N	SYNC_S	UBL_N(3:0)			
0x3A	DL_ZERO(2:0)			MODE_ST(4:0)				
0x3B	ELC	ROT	DL_ST(5:0)					
0x3C	ETS	CDL_MT(1:0)		DL_MT(4:0)				
0x3D	CID_SCD(3:0)				MODE_SER(3:0)			
0x3E	CFGEW0(7:0)							
0x3F	CFGEW1(7:0)							
0x40	C2EPR	E2EPR	PROT_E2P(1:0)		EWM(1:0)		CFGEW2(1:0)	
0x41	MODE_MT(3:0)				CFGIBP(3:0)			
0x42	SBL_MT(1:0)		CHK_MT(1:0)		SPO_MT(3:0)			
0x43	WI2C_MT	SLOW_MT	ROT_MT	DL_EXT_MT(4:0)				
0x44	RR_STAT	RES_MODE	PROT_INS	PROT_CMD	PRES_MODE	PRES_CONF(2:0)		
0x45			OFF_TEM(5:0)					
0x46		ETH_TEM(2:0)				ETL_TEM(2:0)		
0x47	CRC_CFG(15:8)							
0x48	CRC_CFG(7:0)							
0x49	OFFS_ST(7:0)							
0x4A	OFFS_ST(15:8)							
0x4B	OFFS_ST(23:16)							
0x4C	OFFS_ST(31:24)							
0x4D	OFFS_MT(7:0)							
0x4E	OFFS_MT(15:8)							
0x4F	OFFS_MT(23:16)							
0x50	CRC_OFF(7:0)							
0x51	PRES_ST(7:0)							
0x52	PRES_ST(15:8)							
0x53	PRES_ST(23:16)							
0x54	PRES_ST(31:24)							
0x55	PRES_MT(7:0)							
0x56	PRES_MT(15:8)							
0x57	PRES_MT(23:16)							
0x58					FPRES_MT	ECDL_MT	EP2_HL	EP1_HL
0x59	CRC_PRES(7:0)							
0x5A ... 0x71	Reserved							

OVERVIEW								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x72	STATUS0_E2P(7:0)							
0x73	STATUS1_E2P(7:0)							
0x74	STATUS2_E2P(7:0)							
0x75	STATUS3_E2P(7:0)							
0x76	Reserved							
0x77	Reserved							
0x78	DEV_ID(47:40)							
0x79	DEV_ID(39:32)							
0x7A	DEV_ID(31:24)							
0x7B	DEV_ID(23:16)							
0x7C	DEV_ID(15:8)							
0x7D	DEV_ID(7:0)							
0x7E	MFG_ID(15:8)							
0x7F	MFG_ID(7:0)							
0x80	PRO_ID1(15:8)							
0x81	PRO_ID1(7:0)							
0x82	PRO_ID0(15:8)							
0x83	PRO_ID0(7:0)							
0x84	SER_NO(31:24)							
0x85	SER_NO(23:16)							
0x86	SER_NO(15:8)							
0x87	SER_NO(7:0)							
0x88 ... 0xBF	Reserved							

Table 4: Register map digital parameters (EEPROM)

BiSS Specific Registers

For further information on the following BiSS parameters, see BiSS Interface Protocol Description (C Mode) www.ichaus.de/BiSS Interface.

DEV_ID(47:40)	Addr. 0x78; bit 7:0
DEV_ID(39:32)	Addr. 0x79; bit 7:0
DEV_ID(31:24)	Addr. 0x7A; bit 7:0
DEV_ID(23:16)	Addr. 0x7B; bit 7:0
DEV_ID(15:8)	Addr. 0x7C; bit 7:0
DEV_ID(7:0)	Addr. 0x7D; bit 7:0
Code	Description
0x000000000000 ... 0xFFFFFFFFFFFF	Device ID

Table 5: BiSS Device ID

MFG_ID(15:8)	Addr. 0x7E; bit 7:0
MFG_ID(7:0)	Addr. 0x7F; bit 7:0
Code	Description
0x0000 ... 0xFFFF	Manufacturer ID

Table 6: BiSS Manufacturer ID

Parameter EDS selects whether EDSBANK returns 0x0 (i.e. no EDS specified) or 0x3.

EDS	Addr. 0x33; bit 2	
Code	Description	
0x0 0x1	EDSBANK = 0x0 (no EDS specified) EDSBANK = 0x3	
EDSBANK(7:0)	Addr. SER:0x41; bit 7:0	R
Code	Condition	
0x0/0x3	start of EDS data according to parameter EDS	

Table 7: BiSS EDS bank number: start of EDS data

PRO_ID0(15:8)	Addr. 0x82; bit 7:0
PRO_ID0(7:0)	Addr. 0x83; bit 7:0
PRO_ID0(15:8)	Addr. SER:0x42 *); bit 7:0
PRO_ID0(7:0)	Addr. SER:0x43 *); bit 7:0
Code	Description
0x0000 ... 0xFFFF	Profile ID Position Data Channel (MT+ST)
Note	*) when addressing the position data channel (MT+ST)

Table 8: BiSS Profile ID Position Data Channel

PRO_ID1(15:8)	Addr. 0x80; bit 7:0
PRO_ID1(7:0)	Addr. 0x81; bit 7:0
PRO_ID1(15:8)	Addr. SER:0x42 *); bit 7:0
PRO_ID1(7:0)	Addr. SER:0x43 *); bit 7:0
Code	Description
0x0000 ... 0xFFFF	Profile ID Temperature Data Channel
Note	*) when addressing the temperature data channel; for activation of the temperature data channel refer to p. 85

Table 9: BiSS Profile ID Temperature Data Channel

SER_NO(31:24)	Addr. 0x84; bit 7:0
SER_NO(23:16)	Addr. 0x85; bit 7:0
SER_NO(15:8)	Addr. 0x86; bit 7:0
SER_NO(7:0)	Addr. 0x87; bit 7:0
SER_NO(31:24)	Addr. SER:0x44; bit 7:0
SER_NO(23:16)	Addr. SER:0x45; bit 7:0
SER_NO(15:8)	Addr. SER:0x46; bit 7:0
SER_NO(7:0)	Addr. SER:0x47; bit 7:0
Code	Description
0x00000000 ... 0xFFFFFFFF	Serial number

Table 10: BiSS Serial number

OPERATING and CALIBRATION MODES

iC-MNF supports a number of different calibration strategies, providing analog test signals to this end. The following tables show the relevant parameters and resulting operating modes.

For the adjustment of the signal conditioning unit analog test signals are output in analog **calibration modes ANA_x**. The order of the calibration procedure is described in the following chapter.

In **calibration mode BYP_x** the calibration unit is bypassed and the selected track is output at pins PSOUT, NSOUT, PCOUT, NCOUT.

In **calibration mode TIBP** the bias reference source IBP can be adjusted (see p. 36)

In **calibration mode TMS** the signals of the master (SIN/COS) and segment (NSIN/NCOS) track are output for mechanical track adjustment.

In **calibration mode TMN** the signals of the master (SIN/COS) and nonius (NSIN/NCOS) track are output for mechanical track adjustment.

In **calibration mode TSN** the signals of the segment (SIN/COS) and nonius (NSIN/NCOS) track are output for mechanical track adjustment.

TRACMODE	Addr. 0x30; bit 7:5
TEST	Addr. 0x31; bit 5:0
BYP_M	Addr. 0x0B; bit 7
BYP_S	Addr. 0x1B; bit 7
BYP_N	Addr. 0x2B; bit 7

Table 11: Tracking mode, Test mode, Bypass mode

Note:
iC-MNF provides an automatic analog signal calibration feature that can be started using commands. See Chapter **AUTOMATIC CALIBRATION FEATURE** p. 99 for details.

Operating Modes						
	Parameter			Output Signals		
Op. Mode	TRACMODE	TEST	BYP_(M,S,N)*	Pins PSOUT, NSOUT, PCOUT, NCOUT	Pin T0	Pin T1
Normal operating mode						
Normal	0x0	0x0	0x0	Output of master track via line driver	0	0
Analog signal calibration						
Bypass of internal signal conditioning unit						
BYP_M	0x0	0x0	BYP_M = 0x1	PSINM, NSINM, PCINM, NCINM	0	0
BYP_S	0x0	0x0	BYP_S = 0x1	PSINS, NSINS, PCINS, NCINS	0	0
BYP_N	0x0	0x0	BYP_N = 0x1	PSINN, NSINN, PCINN, NCINN	0	0
Signal calibration modes with VDCx intermediate voltages						
ANA_M	0x1	0x0	0x0	PSINM_C, NSINM_C, PCINM_C, NCINM_C**	SVDCM	CVDCM
ANA_S	0x2	0x0	0x0	PSINS_C, NSINS_C, PCINS_C, NCINS_C**	SVDCS	CVDCS
ANA_N	0x3	0x0	0x0	PSINN_C, NSINN_C, PCINN_C, NCINN_C**	SVDCN	CVDCN
Bias Calibration						
TIBP	0x4	0x0	0x0	Output of master track via line driver	-	IBP
Mechanical track adjustment						
TMS	0x5	0x0	0x0	PSINM_C, NSINS_C, PCINM_C, NCINS_C**	REFVPAH	-
TMN	0x6	0x0	0x0	PSINM_C, NSINN_C, PCINM_C, NCINN_C**	REFVPAH	-
TSN	0x7	0x0	0x0	PSINS_C, NSINN_C, PCINS_C, NCINN_C**	REFVPAH	-
Notes	S/D conversion modes with a cyclic conversion (see Table 110 and 111) are not permitted during signal calibration. Cyclic BiSS data requests must also be avoided due to its trigger for sample-and-hold. Analog calibration signals are output via 5 kΩ source impedance. The maximum permissible signal frequency is 2 kHz for a load of 200 pF (see Elec. Char. 711, 712) * Bypass function: inputs (without voltage divider) to outputs, approx. 7 kΩ source impedance, if not stated otherwise BYP_(M,S,N) = 0x0 ** calibration signals of the regarding tracks						

Table 12: Operating modes

SIGNAL CONDITIONING for MASTER-, SEGMENT- and NONIUS-Channel

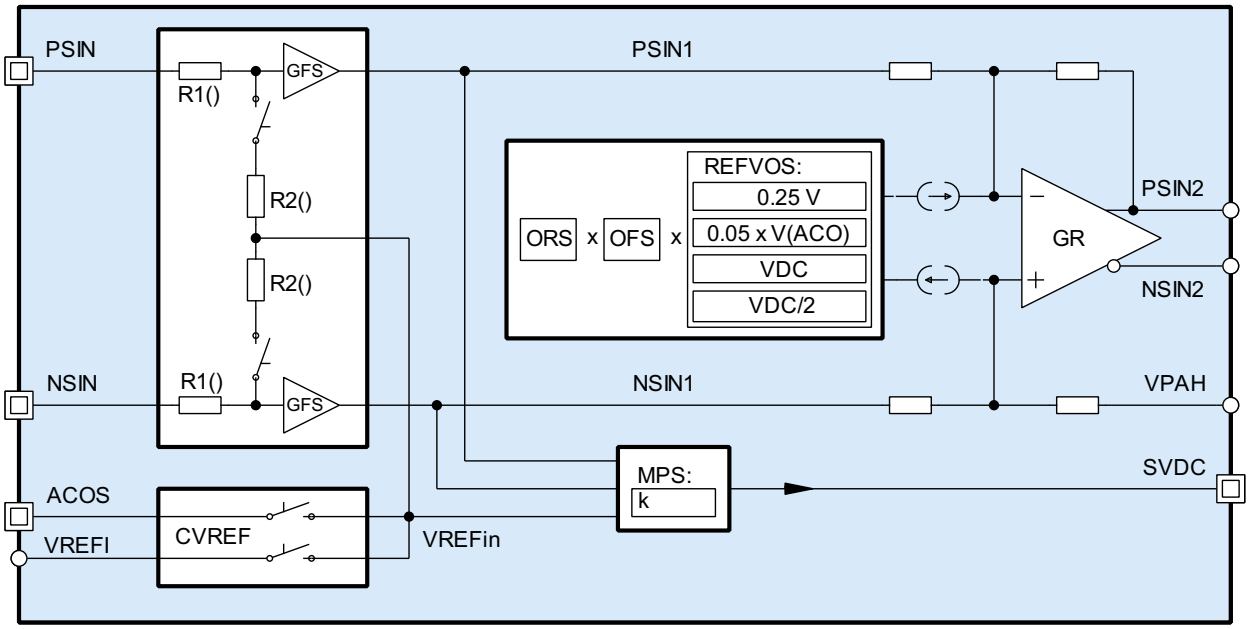


Figure 9: Signal-conditioning unit (sine channel)

All settings are to be carried out for each individual channel separately. A small x in the parameter name stands for (M)aster, (S)egment and (N)onius.

Calibration Hint
Signal adjustment should be made in the order:

1. gain
2. offset
3. phase

The order of description of the analog parameters is in line with this recommendation and can be taken as a guide to signal conditioning.

ISM_M	Addr. 0x0C; bit 3:0		
ISM_S	Addr. 0x1C; bit 3:0		
ISM_N	Addr. 0x2C; bit 3:0		
Code	Function		
Code	Additional R1()	Internal R2()	Mode
0x0	0.1 kΩ	1.6 kΩ	Current input
0x1	0.2 kΩ	2.3 kΩ	Current input
0x2	0.3 kΩ	3.2 kΩ	Current input
0x3	0.3 kΩ	4.6 kΩ	Current input
0x4	3.5 kΩ	High impedance	Voltage input
0xC	15 kΩ	5 kΩ	Voltage input
Others	Reserved		
Note	Refer to Elec.Char. Nos.103,107: Rin() = R1() + R2()		

Table 13: Signal mode

Input Configuration

All input stages are configured as instrumentation amplifiers and thus directly suitable for differential input signals. Referenced input signals can be processed by applying the input signals' reference voltage to the negative inputs. Signal adjustment is possible only in operating modes *ANA_x* (see p. 28). Figure 9 shows a sine channel's conditioning unit; the cosine channel's set-up is equivalent to that of the sine channel.

Both voltage and current signals can be accepted as input signals. For selection, use parameter ISM_x.

Current Mode

In current mode, an input resistor Rin() becomes active at each input pin, converting the current signal into a voltage signal. The input resistance Rin() consists of a pin resistor R1() and the resistor R2() which is connected to the adjustable bias source VREFin. Table 13 shows the selection options. Indicated values are typical, refer to the Electrical Characteristics for tolerances. The input resistance should be set so that center potentials SVDC and CVDC are between 125 mV and 250 mV.

Note: The input circuit is not suitable for back-to-back photodiodes.

Voltage Mode

In voltage mode, a voltage divider can be selected for high input amplitudes. This voltage divider reduces the input signal's amplitude to 25% of the original. The internal circuit corresponds to the circuit in current mode, just the resistor connecting the pin is altered.

Input Reference Voltage

The parameter DCPOS determines the internal input reference voltage VREFI. In the generation of center potentials SVDC and CVDC, it also determines whether the reference voltage VREFin is subtracted from the sum of the particular input signals or the sum is subtracted from VREFin().

DCPOS	Addr. 0x1B; bit 6		
Code	VREFI	Sensor output:	
		Current	Voltage*
0	2.5 V	Low-side current sink	V(PSIN) + V(NSIN) < 2 * VREFin
1	1.5 V	High-side current source	V(PSIN) + V(NSIN) > 2 * VREFin (e.g. LSHC, PN, PNH)
Note	*) Only relevant if using a self-tracked source VDC as offset reference (see Table 20) or if using the voltage divider (refer to Elec.Char. No.101)		

Table 14: Reference voltage and current polarity

Parameter CVREF configures the reference voltage multiplexer.

CVREF	Addr. 0x1D; bit 1:0	
Code	VREFin	Pin function ACOS
0x0	internal	Normal operation
0x2	internal	Output*: output of VREFI
0x3	external	Input**: external reference replaces VREFI (e.g. LSHC, PN, PNH)
0x1	Reserved	
Notes	*) Do not load, buffer recommended. ACOCON_S = 0x0 and ACOT_S = 0x2 is mandatory. **) Refer to Elec.Char. No.510 for permissible input voltage. ACOCON_S = 0x0 is mandatory.	

Table 15: Reference source

Sine/Cosine Gain Settings

The gain is set in four steps:

1. The sensor signal level controller is shut down and the constant current source for the ACO_x output set to a suitable output current (parameter ACOCON_x; current value close to the later operating point).

2. The coarse gain factor is selected so that differential signal amplitudes of about 6 Vpp are produced at the core of the converter (signal PSINx_C to NSINx_C and PCINx_C to NCINx_C).

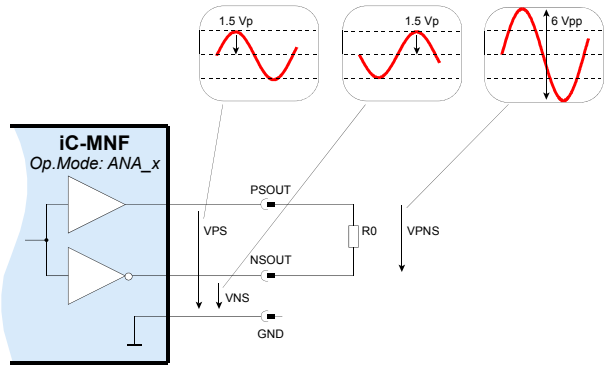


Figure 10: Output signals at pins PSOUT/NSOUT resp. PCOUT/NCOUT in *ANA_x* mode

Note: In *Normal* mode, the master channel converter core signals are output via line drivers with 1/6 of the amplitude of the *ANA_M* mode (see p. 28).

3. Using fine gain factor GFS_x the sine signal amplitude is then adjusted to 6 Vpp.

4. Finally,the cosine signal amplitude needs to be adjusted exactly to the sine signal amplitude using the fine gain factor GFC_x. If this is not possible go back to step 2. and select a different coarse gain factor.

GR_M	Addr. 0x0C; bit 6:4
GR_S	Addr. 0x1C; bit 6:4
GR_N	Addr. 0x2C; bit 6:4
Code	Factor
0x0	6.0
0x1	12.4
0x2	16.2
0x3	20.2
0x4	26.0
0x5	31.6
0x6	39.5
0x7	48.0
Notes	The effective total gain calculates as: G_{eff} = GF(S/C)_x * GR_x, or G_{eff} = 1/4 * GF(S/C)_x * GR_x when using the input voltage divider (ISM_x = 0xC).

Table 16: Coarse gain

GFS_M(10:8)	Addr. 0x01; bit 2:0
GFS_M(7:0)	Addr. 0x00; bit 7:0
GFS_S(10:8)	Addr. 0x11; bit 2:0
GFS_S(7:0)	Addr. 0x10; bit 7:0
GFS_N(10:8)	Addr. 0x21; bit 2:0
GFS_N(7:0)	Addr. 0x20; bit 7:0
Code	Factor
0x000	1
0x001	1.0009
0x002	1.0018
...	$6.25^{(GFS_x/1984)}$
0x7FF	6.6245

Table 17: Sine fine gain

GFC_M(10:8)	Addr. 0x04; bit 2:0
GFC_M(7:0)	Addr. 0x03; bit 7:0
GFC_S(10:8)	Addr. 0x14; bit 2:0
GFC_S(7:0)	Addr. 0x13; bit 7:0
GFC_N(10:8)	Addr. 0x24; bit 2:0
GFC_N(7:0)	Addr. 0x23; bit 7:0
Code	Factor
0x000	1
0x001	1.0009
0x002	1.0018
...	$6.25^{(GFC_x/1984)}$
0x7FF	6.6245

Table 18: Cosine fine gain

Frequency Compensation
iC-MNF allows to configure the frequency compensation of the fine gain stage.

COMP_M(3:0)	Addr. 0x07; bit 7:4
COMP_S(3:0)	Addr. 0x17; bit 7:4
COMP_N(3:0)	Addr. 0x27; bit 7:4
Code	Function
0x0	Low compensation, high cut-off frequency
...	...
0xF	High compensation, low cut-off frequency
Note	Oscillation may occur if the compensation is set too low.

Table 19: Frequency compensation fine gain stage

The best suitable value depends on the selected fine gain factor, i.e. on GFS_x and GFC_x. For each track COMP_x should be set to the inverted bits 10:7 of GFS_x or GFC_x, whichever is smaller. For a nonius system, the compensation should be set equally for all channels, and the lowest fine gain factor setting should determine the compensation COMP_x of all tracks.

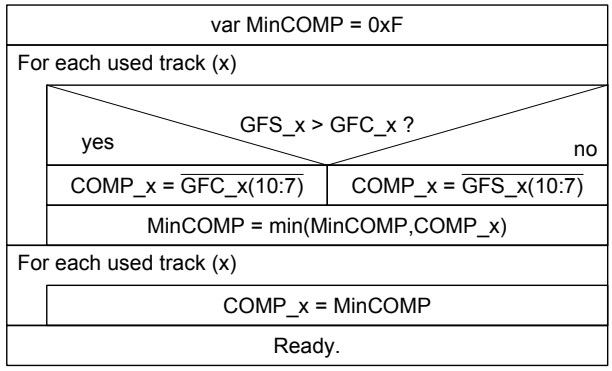


Figure 11: Structogram of the COMP_x setting process for nonius applications (MODE_ST: Nonius, see Table 110)

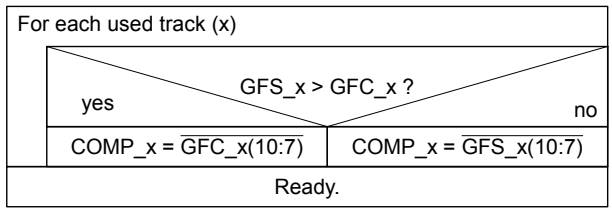


Figure 12: Structogram of the COMP_x setting process for all applications except nonius (MODE_ST: Multiturn, see Table 111)

Sine/Cosine Offset Calibration
In order to calibrate the offset, the reference source must first be selected using parameter REFVOS_x. One fixed voltage and three dependent sources are available for this purpose. The fixed voltage source should be selected for external sensors which provide stable, self-regulated signals.

The VDC references enable the offset calibration to be automatically tracked dependent on the DC level of the input signal. In order to use this function, center potentials SVDC and CVDC have to be adjusted to a minimal AC ripple using parameters MPS_x and MPC_x (refer to the k factor of Table 21).

If V(ACOx) is chosen as the offset reference, 1/20 of the voltage at pin ACOx, acts as the reference. This enables the offset to be calibrated dependent on the supply voltage of the sensor. In this case adjusting the center potentials MPS_x and MPC_x is unnecessary.

REFVOS_M	Addr. 0x0B; bit 5:4
REFVOS_S	Addr. 0x1B; bit 5:4
REFVOS_N	Addr. 0x2B; bit 5:4
Code	Source type
0x0	Feedback of pin voltage V(ACOx): V(REFOS) = $V(ACOx)/20$ for sensor supply-dependent diff. voltage signals for Wheatstone measuring bridges to measure VDDA
0x2	Fixed reference V025: V(REFOS) = 0.25 V for single-ended current or voltage signals for single-ended or differential stabilized signals (regulated sensors, frequency generator)
0x1	Self-tracking sources SVDC and CVDC: VDC_{lo}: V(REFOS) = $^{SVDCx}/_{2}$, $^{CVDCx}/_{2}$ * for differential current signals for differential voltage signals** (e.g. LSHC, PN, PNH)
0x3	Self-tracking sources SVDC and CVDC: VDC_{hi}: V(REFOS) = SVDCx, CVDCx for differential current signals for differential voltage signals**
Note	*) SVDCx, CVDCx divided internally **) Requires CVREF_x = 0x3 and the supply of pin ACOS with the sensor's reference potential (refer to Elec. Char. No. 510 for acceptable input voltages).

Table 20: Offset reference source

MPS_M(9:8)	Addr. 0x09; bit 1:0
MPS_M(7:0)	Addr. 0x08; bit 7:0
MPS_S(9:8)	Addr. 0x19; bit 1:0
MPS_S(7:0)	Addr. 0x18; bit 7:0
MPS_N(9:8)	Addr. 0x29; bit 1:0
MPS_N(7:0)	Addr. 0x28; bit 7:0
Code	$SVDC = k * V(PSIN1) + (1 - k) * V(NSIN1)$
0x000	$k = 0.33$
0x001	$k = 0.33032$
...	... $k = 0.33 + Code \cdot 0.00032$
0x200	$k = 0.50$ (center setting)
...	...
0x3FF	$k = 0.66$
Note	Adjustment required only if REFVOS_x = 0x1 or 0x3

Table 21: Sine center potential

MPC_M(9:4)	Addr. 0x0A; bit 5:0
MPC_M(3:0)	Addr. 0x09; bit 7:4
MPC_S(9:4)	Addr. 0x1A; bit 5:0
MPC_N(3:0)	Addr. 0x19; bit 7:4
MPC_N(9:4)	Addr. 0x2A; bit 5:0
MPC_N(3:0)	Addr. 0x29; bit 7:4
Code	$CVDC = k * V(PCIN1) + (1 - k) * V(NCIN1)$
0x000	$k = 0.33$
0x001	$k = 0.33032$
...	... $k = 0.33 + Code \cdot 0.00032$
0x200	$k = 0.50$ (center setting)
...	...
0x3FF	$k = 0.66$
Note	Adjustment required only if REFVOS_x = 0x1 or 0x3

Table 22: Cosine center potential

The offset calibration range is dependent on the selected REFVOS_x source and is adjusted using the coarse offset factors ORS_x and ORC_x. The actual offset calibration happens through adjusting the factors OFS_x and OFC_x after having selected the calibration range. The calibration target is reached when the DC rate of the differential signals V(PSOUT)-V(NSOUT) and V(PCOUT)-V(NCOUT) is zero.

ORS_M(1:0)	Addr. 0x0B; bit 1:0
ORS_S(1:0)	Addr. 0x1B; bit 1:0
ORS_N(1:0)	Addr. 0x2B; bit 1:0
Code	Factor
0x0	maxVOSS_x = 3 * V(REFVOS)
0x1	maxVOSS_x = 6 * V(REFVOS)
0x2	maxVOSS_x = 18 * V(REFVOS)
0x3	maxVOSS_x = 36 * V(REFVOS)
Note	The offset calibration range refers to the internal calibrated signals (calibration mode ANA_x, see page 28)

Table 23: Sine coarse offset factor

ORC_M(1:0)	Addr. 0x0B; bit 3:2
ORC_S(1:0)	Addr. 0x1B; bit 3:2
ORC_N(1:0)	Addr. 0x2B; bit 3:2
Code	Factor
0x0	maxVOSC_x = 3 * V(REFVOS)
0x1	maxVOSC_x = 6 * V(REFVOS)
0x2	maxVOSC_x = 18 * V(REFVOS)
0x3	maxVOSC_x = 36 * V(REFVOS)
Note	The offset calibration range refers to the internal calibrated signals (calibration mode ANA_x, see page 28)

Table 24: Cosine coarse offset factor

The larger the maxVOS(S/C)_x value the larger is also the offset calibration step size (LSB), what can rise

residual offset errors. Depending on the signal's amplitude, the residual offset errors can limit the possible interpolation accuracy. Table 25 shows the dependencies for full-scale and half-scale signals (referred to calibration mode ANA_x).

Range x Source	maxVOSC_x maxVOSS_x	Cal. Step Size (LSB)	Limitation Of Angle Accuracy
3 x 0.25 V	750 mV	733 µV	none, >14 bit [a] 0.03° ≈ 13.7 bit [b]
6 x 0.25 V	1.5 V	1466 µV	0.03° ≈ 13.7 bit [a] 0.06° ≈ 12.6 bit [b]
6 x 0.5 V	3 V	2933 µV	0.06° ≈ 12.6 bit [a] 0.11° ≈ 11.7 bit [b]
18 x 0.5 V	9 V	8798 µV	0.17° ≈ 11 bit [a] 0.34° ≈ 10 bit [b]
a) Full scale signal ≈ 6 Vpp b) 50 % FS signal ≈ 3 Vpp			

Table 25: Offset calibration Range and impact on the angle accuracy

The sine and cosine offsets are calibrated by a linear voltage divider using OFS_x (10:0) and OFC_x (10:0).

OFS_M(10:4)	Addr. 0x02; bit 6:0		
OFS_M(3:0)	Addr. 0x01; bit 7:4		
OFS_S(10:4)	Addr. 0x12; bit 6:0		
OFS_S(3:0)	Addr. 0x11; bit 7:4		
OFS_N(10:4)	Addr. 0x22; bit 6:0		
OFS_N(3:0)	Addr. 0x21; bit 7:4		
Code	Factor OFS_x	Code	Factor OFS_x
0x000	0	0x400	0
0x001	0.00098	0x401	−0.00098
...	0.00098 ∗ *OFS_x*	...	−0.00098 ∗ *OFS_x*
0x3FF	1	0x7FF	−1

Table 26: Sine fine offset factor

OFC_M(10:4)	Addr. 0x05; bit 6:0		
OFC_M(3:0)	Addr. 0x04; bit 7:4		
OFC_S(10:4)	Addr. 0x15; bit 6:0		
OFC_S(3:0)	Addr. 0x14; bit 7:4		
OFC_N(10:4)	Addr. 0x25; bit 6:0		
OFC_N(3:0)	Addr. 0x24; bit 7:4		
Code	Factor OFC_x	Code	Factor OFC_x
0x000	0	0x400	0
0x001	0.00098	0x401	−0.00098
...	0.00098 ∗ *OFC_x*	...	−0.00098 ∗ *OFC_x*
0x3FF	1	0x7FF	−1

Table 27: Cosine fine offset factor

The calibrated offset is generated through
$VOS() = maxVOS(S/C) * OF(S/C)\_x$

Sine to Cosine Phase Correction
The phase shift between sine and cosine can be adjusted using the parameter value PH_x.

Note: If the corrected phase error exceeds 2.25°, the gain and offset correction need to be readjusted in order to ensure a 13 bit track resolution accuracy.

PH_M(9:8)	Addr. 0x07; bit 1:0		
PH_M(7:0)	Addr. 0x06; bit 7:0		
PH_S(9:8)	Addr. 0x17; bit 1:0		
PH_S(7:0)	Addr. 0x16; bit 7:0		
PH_N(9:8)	Addr. 0x27; bit 1:0		
PH_N(7:0)	Addr. 0x26; bit 7:0		
Code	Correction angle	Code	Correction angle
0x000	+0	0x200	−0
0x001	+0.0204	0x201	−0.0204
...	+0.0204 ∗ *PH_x*	...	−0.0204 ∗ *PH_x*
0x1FF	+10.42	0x3FF	−10.42

Table 28: Sine to cosine phase correction

AMPLITUDE CONTROL

The iC-MNF allows the amplitude of the output signals at pins PSOUT, NSOUT, PCOUT, and NCOUT to be kept constant - regardless of temperature and ageing effects - by tracking the sensor supply. For this purpose, the iC-MNF has a controlled high-side current source at pins ACOM, ACOS and ACON which can power the external sensors (e.g. AMR sensor bridges). The driver capability of these current sources is selected by ACOR_x and the control mode by ACOT_x (the small x in the parameter name stands for (M)aster, (S)egment and (N)onius).

So that the output signals can be calibrated without control interference, the relevant signal level controller output ACOx has to be set to a constant current (see Table 31). The constant current is adjusted using ACOCON_x and ACOR_x. This current must be so low as to leave enough reserve for temperature and aging effects and ensure that no unnecessary power dissipation is generated. However, the source current may not be too low so as to permit a better signal contrast and improved signal to noise ratio. Using this current the signal calibration can then be performed so that the sine/cosine signals at the sine-to-digital converter have a (differential) value of 6 Vpp in their calibrated state. Once calibration has proved successful the signal level controller can be activated.

There are three integrated signal level control units which are powered by VACO. It is thus possible to regulate each track individually or, in optical systems with a LED, for example, all three tracks using the master signal level controller. If the control unit's working range is exceeded, an error message is generated (ACx_MIN/MAX; refer to Elec. Char. nos. 408, 409, 508 and 509). Note that error messaging is disabled during constant current mode.

Note: The control output ACOx is activated with power-on, using reset values (0x00) initially, until the relevant configuration registers have been read from the EEPROM.

ACOR_M(1:0) Addr. 0x0D; bit 3:2	
Code	Maximum current I_{max}(ACOM)
0x0	5 mA
0x1	10 mA
0x2	25 mA
0x3	50 mA

Table 29: Maximum output current (for ACOM output)

ACOR_S Addr. 0x1D; bit 2 **ACOR_N** Addr. 0x2D; bit 2	
Code	Maximum current I_{max}(ACOS), I_{max}(ACON)
0x0	5 mA
0x1	10 mA

Table 30: Maximum output current (for ACOS and ACON output)

ACOT_M(1:0) Addr. 0x0D; bit 5:4 **ACOT_S(1:0)** Addr. 0x1D; bit 5:4 **ACOT_N(1:0)** Addr. 0x2D; bit 5:4	
Code	Operation mode
0x0	Deadband square control, **
0x1	Continuous square control, *
0x2	Constant current source
0x3	Not permitted
*) Square control of V()scq = $\sqrt{(V(PSOUT - V(NSOUT))^2 + (V(PCOUT - V(NCOUT))^2}$ **) deadband range is set by ACO_HYS_x (x = M,S,N)	

Table 31: Controller op. mode (all ACOM, ACOS, ACON output)

Note: Excessive input signals or internal signal clipping can interfere control operation, so that the preset operating point may not be reached (upon power up) or maintained (upon disturbances). Use Control Error ACM_MAX and Signal Error AM_MIN for monitoring and warning messaging; configure CFGEW0 accordingly.

With active Deadband square control the signal deviation is only balanced if the set deadband range is exceeded. In Continuous square control mode any signal deviation is balanced over the ACOx output.

ACO_HYS_M(1:0) Addr. 0x0D; bit 7:6 **ACO_HYS_S(1:0)** Addr. 0x1D; bit 7:6 **ACO_HYS_N(1:0)** Addr. 0x2D; bit 7:6	
Code	Deadband Range
0x0	2.5%
0x1	5%
0x2	7.5%
0x3	10%

Table 32: Controller deadband range (ACOT_x = 0x0, all ACOM, ACOS, ACON output)

ACOCON_M(5:0) Addr. 0x0E; bit 5:0 **ACOCON_S(5:0)** Addr. 0x1E; bit 5:0 **ACOCON_N(5:0)** Addr. 0x2E; bit 5:0	
Code	Factor
0x00	0% * I_{max}(ACOM, ACOS, ACON)
0x01	1.6% * I_{max}(ACOM, ACOS, ACON)
...	...
0x3F	100% * I_{max}(ACOM, ACOS, ACON)

Table 33: Fine constant current factor (ACOT_x = 0x2, all ACOM, ACOS, ACON output)

Square control mode keeps the sum of the sine/cosine amplitude squares at a constant value. The parameter ACOCTR_x provides fine adjustment capabilities to the setpoint for the analog output signals.

ACOCTR_M(4:0) Addr. 0x0F; bit 4:0 **ACOCTR_S(4:0)** Addr. 0x1F; bit 4:0 **ACOCTR_N(4:0)** Addr. 0x2F; bit 4:0	
Code	Setpoint Correction $ACOCTR = \frac{Code}{31} * 20 - 10$
0x00	-10%
...	...
0x0F	-0.32%
0X10	0.32%
...	...
0x1F	+10%

Table 34: Setpoint Correction Square Control (ACOT_x = 0x0, 0x1, all ACOM, ACOS, ACON output)

Besides the control unit's working range also the signal's amplitude is monitored. If one of the implemented limits is exceeded, the corresponding signal error bit is set (Ax_MIN/MAX; see Elec. Char. nos. 406, 407, 506 and 507).

Note: Signal amplitude monitoring is operational in constant current mode, but with limits depending on the square control setpoint (ACOCTR_x).

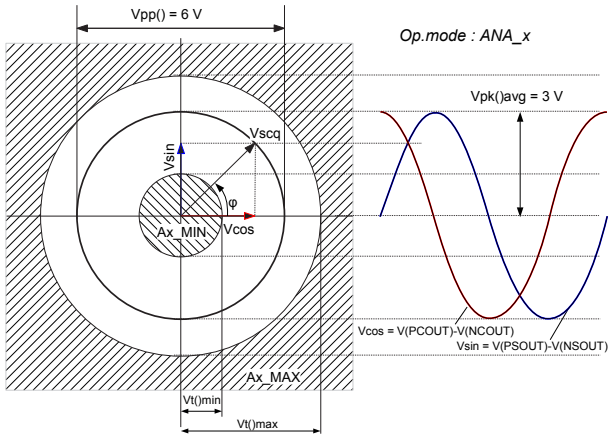


Figure 13: Signal monitoring according to setpoint of square control (numerical example; for limits see Elec. Char. nos. 406, 407, 506 and 507).

ANALOG PARAMETERS

Bias Current Source

The calibration of the bias current source in operation mode *TIBP* (see p. 28) is prerequisite for adherence to the given electrical characteristics and also instrumental in the determination of the chip timing (e.g., SCL clock frequency). For the calibration of source IBP to its target value of 200 µA the voltage across the 5 kΩ measurement resistor has to be adjusted to 1 V.

CFGIBP Addr. 0x41; bit 3:0 **CFGIBP** Addr. SER:0x01; bit 3:0 Bank 1			
Code k	$IBP \sim \frac{31}{31-k}$	Code k	$IBP \sim \frac{31}{31-k}$
0x0	100.0 %	0x8	134.8 %
0x1	103.3 %	0x9	140.9 %
0x2	106.9 %	0xA	147.6 %
0x3	110.7 %	0xB	155.0 %
0x4	114.8 %	0xC	163.2 %
0x5	119.2 %	0xD	172.2 %
0x6	124.0 %	0xE	182.4 %
0x7	129.2 %	0xF	193.8 %

Table 35: Bias current source calibration

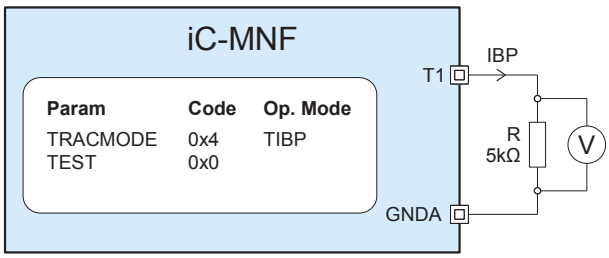


Figure 14: Measurement circuit

Signal Noise Filters

iC-MNF has noise filters for both the analog output drivers and the sine-to-digital converter. These filters can be activated by ENF.

ENF(0) Addr. 0x30; bit 2	
Code	Function
0x0	Disabled
0x1	Sin/Cos Output driver noise filter activated

Table 36: Noise filter for the output drivers

ENF(1) Addr. 0x30; bit 3	
Code	Function
0x0	Disabled
0x1	S/D Conversion noise filter activated

Table 37: Noise filter for the sine-to-digital converter

The noise filter's adaption mode can be changed using NDBF. Using deadband adaption is favorable regarding signal distortion. However, assuming a fixed input frequency, note that the lowpass cutoff frequency can vary due to the deadband behavior.

NDBF Addr. 0x30; bit 4	
Code	Function
0x0	Deadband
0x1	Standard

Table 38: Frequency adaption mode for both signal noise filters

DISCURLIM Addr. 0x0D; bit 0	
Code	Function
0x0	Default (test0)
0x1	Reserved for iC-Haus test (test1)

Table 39: DISCURLIM

FGHI Addr. 0x0D; bit 1	
Code	Function
0x0	Default (test0)
0x1	Reserved for iC-Haus test (test1)

Table 40: FGHI

ANALOG AND DIGITAL DRIVERS

Sin/Cos Output Drivers

The analog signal path of iC-MNF operates independently from the interpolation engine, and features embedded line drivers to output differential 1 Vpp signals to lines with 100 Ω termination.

The parameter DRVDIS defines if the output drivers are enabled after startup, and whether error events can switch the drivers to high impedance (tristate). For the latter, DRVMASK selects the type of errors: **Standard Errors**, **Data Control**, **Analog Signal/Control** and **Communication Errors**.

DRVDIS	Addr. 0x33; bit 5:4
Code	Function
0x0	Never disable the drivers on error (the drivers are disabled during startup only)
0x1	Disable the drivers during error(s) (as long as an error persists)
0x2	Disable the drivers on error(s) until clearing action (MNF_CMD: CLEAR_STAT, SOFT_RES, HARD_RES, or read of status register (RR_STAT = 0x1))
0x3	Drivers permanently disabled.

Table 41: Sin/Cos output driver disable

DRVMASK	Addr. 0x33; bit 7:6
Code	Function
0x0	Driver disabled on **Standard Errors**: 1. iC-MNF in startup procedure 2. EPR_ERR[1]: I2C communication/CRC Error 3. TH_ERR/TL_ERR[1]: Temperature Error 4. EP1_STAT/EP2_STAT[1]: EP1/EP2 is set
0x1	Driver disabled as defined with DRVMASK = 0x0 + **Data Control Errors**: 1. ST_CTR 2. MT_CTR
0x2	Driver disabled as defined with DRVMASK = 0x1 + **Analog Signal/Control Errors**: 1. Ax_MAX/Ax_MIN[1] 2. ACx_MAX/ACx_MIN[1]
0x3	Driver disabled as defined with DRVMASK = 0x2 + **Communication Errors**: 1. RF_ERR 2. CT_ERR 3. MT_ERR
Notes	Explanation of status bits see p. 86 ff. [1] if configured to error bit with CFGEW0..2 (see p. 90 ff.)

Table 42: Sin/Cos output driver disable masking: active with DRVDIS = 0x1, 0x2

Digital Driver Outputs

The digital outputs SLO and NSLO can be used as either a push-pull or low-side driver. The mode of operation is determined by SLO_LS. The driving capability is set with SLO_SC.

SLO_LS	Addr. 0x32; bit 4
Code	Operating mode
0x0	Push-pull operation
0x1	Low-side driver mode (N channel open drain)

Table 43: RS422 Driver output mode

In order to meet RS422 specifications a short-circuit current of 30 mA should be selected. The driving capability can be reduced for instance when external line drivers are used or the master device such as an MCU is on the same PCB.

SLO_SC	Addr. 0x32; bit 5
Code	Short-circuit current
0x0	30 mA
0x1	4 mA

Table 44: RS422 Driver short-circuit current

In order to be able to connect the digital output pins MTMA, MAO, EP1, EP2 and NERR directly to an external IC which uses e.g., 3.3V supply voltage these drivers can be configured as low-side driver. The mode of operation is determined by DLS.

DLS	Addr. 0x32; bit 6	
Code	Pin	Operating mode
0x0	MTMA, MAO, EP1, EP2	Push-pull operation
0x1		Low-side driver mode (N channel open drain)
0x0	NERR	Internal pull-up enabled
0x1		Internal pull-up disabled

Table 45: Driver output mode MTMA, MAO, EP1/2, NERR

Note:
If configured in **Low-side driver mode** external Pull-Up resistors to the appropriate voltage have to be connected to the relevant pins.

BATTERY MANAGEMENT AND MNFOK OUTPUT

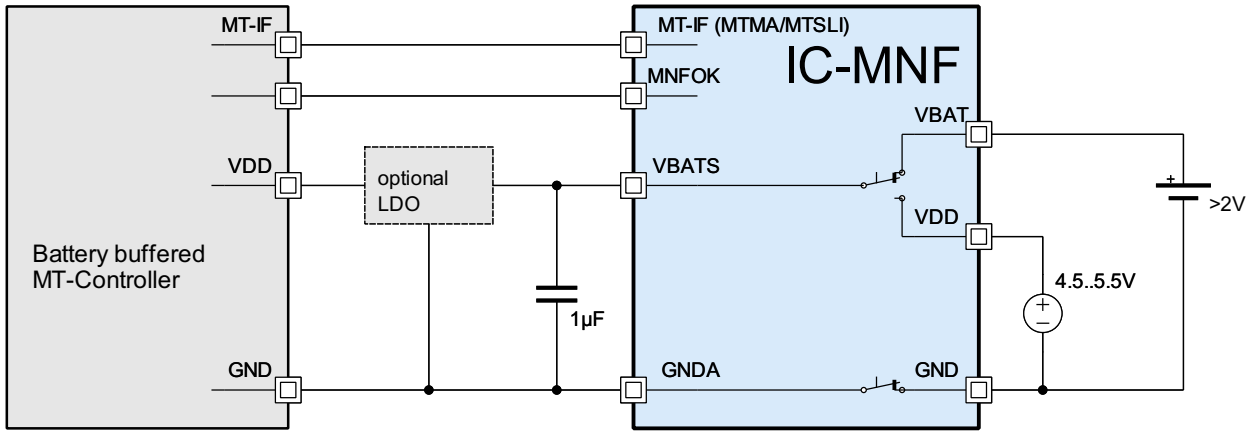


Figure 15: Battery management circuit overview

To simplify implementation for battery buffered multiturn encoder designs, iC-MNF integrates switches, control logic and extended reverse polarity protection in order to supply the external multiturn with an external battery or via pin VDD.

Application Hint
If not needed for application, pin MNFOK can be left open.
Pin VBAT may not be left open. It is recommended to connect it to GNDA.

Battery and supply are connected to the reverse polarity protected pins VBAT and VDD. iC-MNF tracks both voltages and routes the higher of both voltages to pin VBATS. In order to stabilize this voltage output when switching between the two input voltages, an additional capacitor of 1µF is needed (shown in Fig. 15; other standard additional devices are omitted here for sake of convenience). GNDA and VBATS can be used as supply for a battery stabilized multiturn counter, which is then reverse polarity protected through iC-MNF. At the same time the battery current draw at VBAT by iC-MNF is very low (see Elec. Char. no. B10).

Additionally, the control signal MNFOK is provided. It signals to the battery buffered MT-controller whether iC-MNF is supplying the sensor (logic level high) or if the MT-controller is alone responsible for counting and supplying the sensor (logic level low). Logic level low is indicated with 0 V and logic level high is indicated with VDD.

The MNFOK signal is set if the following conditions are met:

1. EEPROM present and CRC_CFG and CRC_OFF are correct
2. EEPROM readout completed and 1 ms timeout expired
3. AM_MIN error is not set

If condition 1. is not fulfilled, MNFOK is not set until a valid configuration has been written to iC-MNF and the command SOFT_RES has been executed.

Voltage Level at pin MNFOK	Responsible for sensor supply
0 V	MT-controller
VDD	iC-MNF

Table 46: MNFOK signal

EEPROM AND I2C INTERFACE

I2C Interface

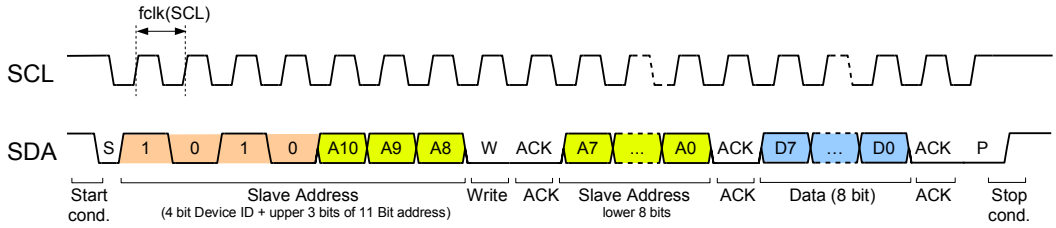


Figure 16: Example of line signals for I2C protocol: write single byte to EEPROM

The I2C interface enables read and write access to a serial EEPROM which uses an addressing scheme equal to an 24C02 EEPROM.

Application Hints
iC-MNF is not multi-master capable; do not connect another I2C master.
In case of interconnection with iC-PVL, please contact support@ichaus.de.

Application Hints
To protect the EEPROM against a reversed power supply voltage it can be connected to the integrated supply switch (pins VDDA and GNDA).
The EEPROM specifications and absolute maximum ratings should comply to the pin voltages of VDDA, SCL and SDA during startup and operation. A protective circuit may be advisable depending on the EEPROM model.
For EEPROM selection the following minimal requirements must be fulfilled:

- Operation from 3.3 V to 5 V
- I2C-Interface
- Address space max. 11 bit
- Min. 2048 bit, 256x8, i.e., type 24C02
  Min. with EDS 4096 bit, 512x8, i.e., type 24C04
  Max. 16384 bit, 2048x8, i.e., type 24C16

If addressing one EEPROM of <16384 bit (type 24C16), the block selections bits of the EEPROM device normally named A0..2 must be set to zero and thus the I 2 C device ID is 0xA (first byte of communication addressing EEPROM address 0x00 is b'1010 0000 with the R/W bit on zero).

Number of I2C communication retries	
Operation	max. number of retries
I2C write access	256 per byte
I2C single read access	8 per byte
EEPROM read on startup	3 per CRC protected configuration area (CRC_CFG, CRC_OFF, CRC_PRES)

Table 47: Number of I2C communication retries in case of an error

The I2C clock frequency at pin SCL can be selected using the parameter FAST_I2C. During the startup procedure the I2C clock frequency changes immediately after reading EEPROM address 0x01. Please refer to Elec. Char. No. D06 for the I2C clock frequency during startup.

FAST_I2C	Addr. 0x01; bit 3
Code	Function
0x0	Regular clock frequency , f(SCL) approx. 62.5 kHz[1]
0x1	High clock frequency , f(SCL) approx. 250 kHz[1]
Note	[1] I2C clock frequency after successful system start up, i.e. with CFGIBP calibrated

Table 48: I2C Fast Mode

CRC: Configuration, Offset and Preset Data

For the cyclic redundancy checks the parameters of iC-MNF are grouped into three areas: configuration, offset and preset with the corresponding checksums CRC_CFG, CRC_OFF and CRC_PRES.

CRC_CFG, CRC_OFF and CRC_PRES are checked on startup. A check during operation can be explicitly requested with command CRC_CHECK (see Table 67 and 165). This command can also be configured to the input pin PRES and if so be started with a rising edge on PRES (see Table 172). A CRC error is reported on status bit EPR_ERR.

iC-MNF calculates CRC_CFG, CRC_OFF and CRC_PRES automatically when writing the configuration to the EEPROM. However, an example of a CRC calculation routine is given in Table 49.

```
unsigned char ucDataStream = 0;
int iCRC_CFGPoly = 0x1021;
unsigned int uiCRC_CFG;
int i = 0;

uiCRC_CFG = 1; // start value !!!
for (iReg = 0; iReg<71; iReg ++)
{
  ucDataStream = ucGetValue(iReg);
  for (i=0; i<=7; i++) {
    if ((uiCRC_CFG & 0x80) != (ucDataStream & 0x80))
      uiCRC_CFG = (uiCRC_CFG << 1) ^ iCRC_CFGPoly;
    else
      uiCRC_CFG = (uiCRC_CFG << 1);
    ucDataStream = ucDataStream << 1;
  }
}
```

Table 49: C++ example of CRC_CFG checksum calculation

The configuration data is located in address range 0x00 to 0x46. It is protected with a 16 bit checksum (CRC_CFG) build with a 17 bit CRC polynomial. The start value for the CRC_CFG calculation is 1.

CRC_CFG(7:0)	Addr. 0x48; bit 7:0	
CRC_CFG(15:8)	Addr. 0x47; bit 7:0	
CRC_CFG(7:0)	Addr. SER:0x08; bit 7:0	Bank 1
CRC_CFG(15:8)	Addr. SER:0x07; bit 7:0	Bank 1
Code	Meaning	
...	CRC formed with CRC polynomial 0x11021*)	
Note	*) $x^{16} + x^{12} + x^5 + 1$, start value 0x1 This is equivalent to CRC-CCITT/CRC-16	

Table 50: Configuration data checksum

The offset data is located in address range 0x49 to 0x4F of the EEPROM and is protected with an 8-bit checksum (CRC_OFF) build with a 9 bit CRC polynomial. The start value for the CRC_OFF calculation is 1.

CRC_OFF	Addr. 0x50; bit 7:0	
CRC_OFF	Addr. SER:0x10; bit 7:0	Bank 1
Code	Meaning	
...	CRC formed with CRC polynomial 0x107*)	
Note	*) $x^8 + x^2 + x^1 + 1$, start value 0x1	

Table 51: Offset data checksum

The preset data and the parameters FPRES_MT, ECDL_MT and EPx_HL (x = 1,2) are located in address range 0x51 to 0x58 of the EEPROM and are protected with an 8-bit checksum (CRC_PRES) build with a 9 bit CRC polynomial. The start value for the CRC_PRES calculation is 1.

CRC_PRES	Addr. 0x59; bit 7:0	
CRC_PRES	Addr. SER:0x19; bit 7:0	Bank 1
Code	Meaning	
...	CRC formed with CRC polynomial 0x107*)	
Note	*) $x^8 + x^2 + x^1 + 1$, start value 0x1	

Table 52: Preset data checksum

STARTUP BEHAVIOR

Startup
Figure 17 shows the startup behavior of iC-MNF. After turning on the power supply (power-on reset) iC-MNF reads the configuration, offset and preset data from the EEPROM. If the data can be read without error, a timeout of 8 ms is allowed to elapse.

If the multiturn interface has been configured for an external sensor, the device waits for a longer timeout of 16 ms to elapse. The multiturn data is then read in and the first conversion performed in order to determine the absolute position. iC-MNF then goes into normal operation.

Note: During startup, the NERR pin is held low, the CMD_EXE status bit is set, and command execution is denied. If a multiturn is connected, it must return a disabled error bit to exit the startup loop. See also Figure 56 for details.

If an error occurs while the EEPROM data is being read (a CRC error or communication error with the EEPROM), the current read in process is canceled and restarted. Following a third failed attempt the read in procedure is terminated.
If no EEPROM is connected the parameters of the configuration area are initialized as shown in Table 53, the offset and preset area is initialized with zero. If there was a CRC error in a parameter area (configuration, offset or preset) only the corresponding parameter area is initialized to its default values.

In case of an EEPROM or CRC_CFG error the logic level at pin MAO selects the interface protocol.

Note: In case of an EEPROM or CRC_CFG error at startup, the I/O interface protocol is set depending on the logic level at the MAO pin:
MAO = 0 → BiSS
MAO = 1 → SPI
Do not permanently clamp MAO to logic "0". An internal pull-down selects the BiSS interface as default.

If the BiSS protocol is selected, pin SLO is set high to indicate an error and the interface must be unlocked prior to system configuration (see **BiSS: Initial Configuration After Startup Error**, p. 43). The system configuration can be started directly if the SPI protocol is selected. After successful configuration of iC-MNF via the I/O interface the command SOFT_RES must be executed in order to switch iC-MNF to normal operation (see p. 93) and to enable the registers CFGIBP, DLS and MODE_SER.

Default values			
Bank	Addr. (serial access)	value	Meaning/ parameters affected
Master/Segment/Nonius channel			
0	0x*7	0xF0	COMP_x*)
0	0x*9	0x02	MPS_x
0	0x*A	0x20	MPC_x
0	0x*C	0x04	ISM_x
0	0x*D	0x60	ACO_HYS_x, ACOT_x
0	0x*F	0x10	ACOCTR_x
Notes	* = 0,1,2 parameter area Master, Segment, Nonius *) x = M, S, N		
Digital Parameters			
0	0x31	0xC0	ensure default
0	0x32	0x04	CNVSPD = Fast
0	0x3B	0x08	DL_ST = 8 bit
0	0x3E	0xFF	CFGEW0: messages to error and warning enabled
0	0x3F	0x80	CFGEW1(7): EPR_ERR enabled to error
1	0x06	0x70	temperature threshold warning:125°C, error:140°C
Notes	all other registers are preset with 0 Register assignment for register access via serial I/O interface see p. 58		
MFG_ID and DEV_ID: no EEPROM on startup present			
-	0x78	0x4D	≃ M
-	0x79	0x4E	≃ N
-	0x7A	0x46	≃ F
-	0x7B	CHIP_REL	see Table 93
-	0x7E	0x69	≃ i
-	0x7F	0x43	≃ C
Notes	in case of CRC errors addressing 0x78 - 0x7F will access the external EEPROM Register assignment for register access via serial I/O interface see p. 58		

Table 53: Default configuration without EEPROM, after EEPROM error or CRC_CFG error on startup

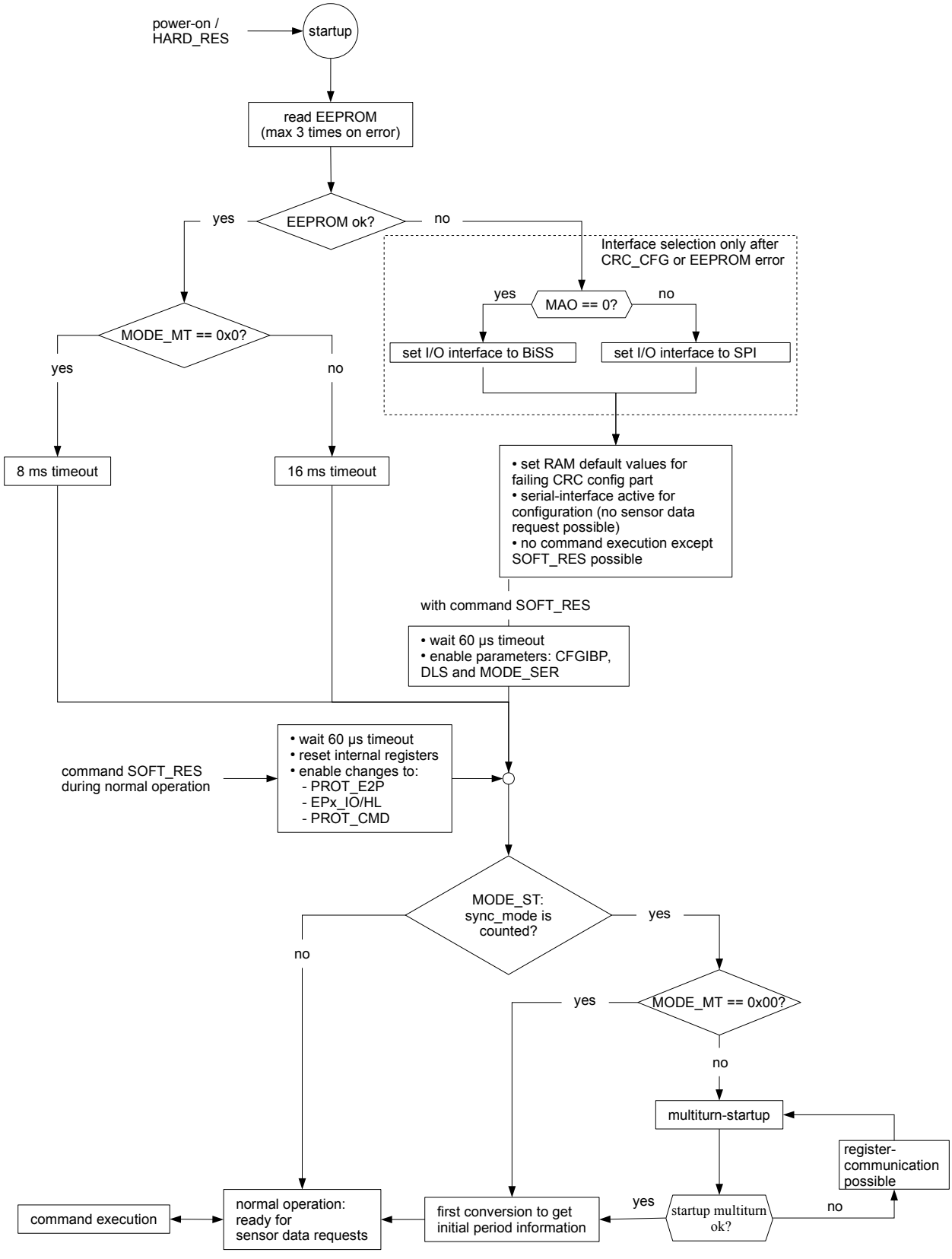


Figure 17: Startup behavior

BiSS: Initial Configuration After Startup Error
Pin SLO is set to permanent '1' (NSLO = '0') if the BiSS protocol is selected via pin MAO after a configuration error at startup. The configuration parameters are initialized according to Table 53.

At first BiSS bidirectional communication is not possible because pin SLO is driven high and pin SLI is ignored. The initial configuration must be written "blind" as no data is sent back from iC-MNF. For the initial configuration using BiSS mode communication, iC-MNF uses always slave ID 0.

To release pin SLO and to restore full BiSS bidirectional communication, MODE_SER must be set to BiSS and command SOFT_RES must be executed (MODE_SER see Tab. 54, MNF_CMD see Tab. 165).

Since each BiSS cycle transmits only a single CDM bit (BiSS register communication), it can be reduced to four clock periods plus timeout.

Note:
A detailed explanation of the BiSS register communication can be found in the BiSS Interface Protocol Description (C-Mode) at www.biss-interface.com.

The following figure shows a single BiSS cycle with CDM = 0, CDM = 1, and a four BiSS cycle extract for a CDM sequence of 0b0010.

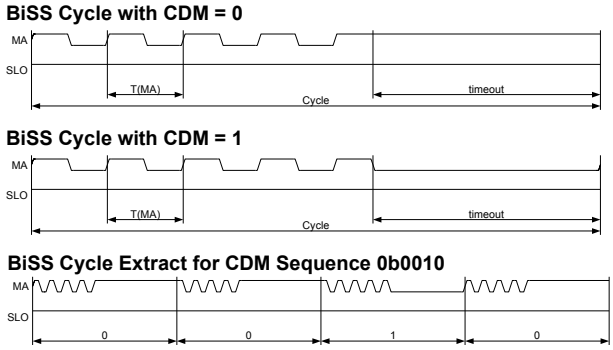


Figure 18: Example of reduced BiSS frames for configuration

A single BiSS register write requires 14 BiSS cycles with CDM = 0 followed by 32 cycles of BiSS C register communication data. Following is an example BiSS sequence to write MODE_SER and then reset iC-MNF using the SOFT_RES command.

```
1) Address 0x3D, Data 0x00

CDM 00000000000000
    S CTS ID  ADR     CRC  R W S DATA     CRC  P
CDM 1 1   000 0111101 1101 0 1 1 00000000 1111 0

2) Address 0x77, Data 0x00

CDM 00000000000000
    S CTS ID  ADR     CRC  R W S DATA     CRC  P
CDM 1 1   000 1110111 0111 0 1 1 00000000 1111 0
```

Note:
The first CRC covers CTS, ID and ADR. The second CRC covers DATA.
CRC is sent inverted. The CRC polynomial is 0x13.

Figure 19: BiSS CDM sequence to unlock SLO

I/O INTERFACE

Serial Interface: Overview

iC-MNF can transmit position data according to the BiSS C, SSI and SPI protocol.

MODE_SER	Addr. 0x3D; bit 3:0
Code	Protocol
0x0	BiSS C
0x1	BiSS C Extended CRC
0x2	SSI binary
0x3	SSI binary +ERRL
0x4	SSI binary +ERRH
0x5	SSI gray
0x6	SSI gray +ERRL
0x7	SSI gray +ERRH
0x8	SPI + EW
0x9	RSSI binary
0xA	RSSI binary +ERRL
0xB	RSSI binary +ERRH
0xC	RSSI gray
0xD	RSSI gray +ERRL
0xE	RSSI gray +ERRH
0xF	ExtSSI

Table 54: Interface protocol

The polarity of the error (SSI/RSSI + ERRL/ERRH) and error and warning (BiSS) bits are summarized in Table 55. For a summary of the status information which can be displayed on error and warning please refer to p. 86.

MODE_SER				
Function	Error		Warning	
	low active	high active	low active	high active
BiSS	✓	-	✓	-
(R)SSI(gray)	-	-	-	-
(R)SSI(gray) +ERRL	✓	-	-	-
(R)SSI(gray) +ERRH	-	✓	-	-
SPI + EW	✓	-	✓	-

Table 55: MODE_SER: error/warning-bit within serial protocols

Serial Interface: Configuring Data Length And Code Direction

The number of output bits is determined in general by parameters DL_ST, DL_MT, DL_ZERO. Depending on the specified protocol the number of output bits can be augmented by error/warning bits and a 6 bit sign-of-life counter. A detailed explanation can be found in the chapter of the regarding protocol: BiSS: p. 47, SSI: p. 50, SPI: p. 51.

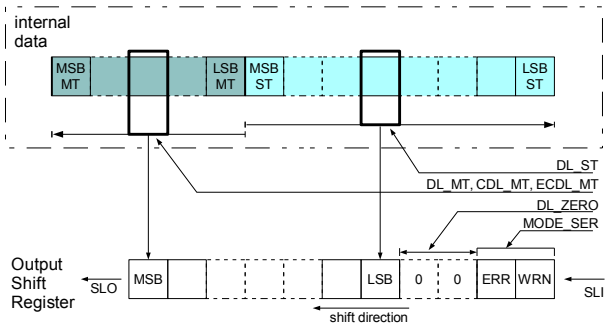


Figure 20: Overview of parameters influencing the output data length

The output data bit length for singleturn data can be set independently of the internal converter resolution. For bit lengths which exceed the internal word length the data following the LSB is filled with zeros.

Optional multiturn data is always transmitted before singleturn data. If an external MT sensor is configured, the output data bit length for multiturn data can be set independently of the multiturn data length read-in via the external multiturn interface. If the output data bit length exceeds the data length available from the external MT sensor, the additional data will correspond to the internally counted MT value.

Additional zeros to be inserted after the user data can be configured with DL_ZERO .

DL_MT	Addr. 0x3C; bit 4:0
Code	Bit count
0x00	0 bit
0x01	1 bit
...	...
0x18	24 bit

Table 56: MT data length

DL_ST	Addr. 0x3B; bit 5:0
Code	Bit count
0x00	0 bit
...	...
0x30	48 bit
Note	Default is 0x8: 8 bit

Table 57: ST Data length

DL_ZERO	Addr. 0x3A; bit 7:5
Code	Bit count
0x0	no additional '0' Bit
0x1	1 additional '0' Bit
...	...
0x7	7 additional '0'-Bits

Table 58: Selection of additional ZEROs

For encoder designs which temporarily need to restrict or disable the output of multiturn data, iC-MNF offers the possibility to restrict the multiturn output data length according to CDL_MT even if register protection is activated with PROT_E2P (see Table 94). Parameter CDL_MT is located in the protectable configuration data area. The changes are enabled with ECDL_MT.

CDL_MT	Addr. 0x3C; bit 6:5
Code	Function
0x0	DL_MT as configured/ECDL_MT has no effect
0x1	Set DL_MT to 0 bit/external MT deactivated
0x2	Set DL_MT to 1 Bit
0x3	Set DL_MT to 2 Bit

Table 59: Possible changes to MT data length which can be activated with ECDL_MT

Parameter ECDL_MT enables the change to the multiturn output data length configured with parameter CDL_MT. It is located in the PRESET configuration area which is accessible even if PROT_E2P = RP1.

ECDL_MT	Addr. 0x58; bit 2	
ECDL_MT	Addr. SER: 0x18; bit 2	Bank 1
Code	DL_MT restriction configured with CDL_MT	
0x0	disabled	
0x1	enabled	

Table 60: Enable changes to MT data length configured with CDL_MT

Note:
If the changes to DL_MT activated by ECDL_MT should be permanent the command WRITE_CONF must be executed.

The code direction of the output data word can be changed using pin DIR or parameter ROT. Both signals are EXOR-gated and together comprise the internal code direction signal.

ROT	Addr. 0x3B; bit 6
Code	Function
0x0	no inversion of code direction
0x1	inversion of code direction

Table 61: Inversion of code direction

The DIR-Pin can be disabled, so that a change of the code direction via pin is no longer possible.

NENDIR_P	Addr. 0x32; bit 7
Code	change of code direction via pin
0x0	enabled
0x1	disabled

Table 62: DIR pin enable

BiSS Protocol

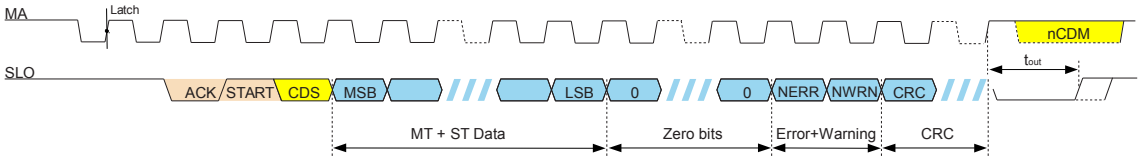


Figure 21: Example of line signals for BiSS C protocol

MODE_SER	
Code	Protocol
0x0 0x1	BiSS C BiSS C with extended CRC *)
Note	*) see Table 65

Table 63: Interface protocol BiSS

The BiSS C interface serial bit stream is binary coded. The error and warning bit is low active. Transmission of sensor and register data is implemented. For further information regarding the BiSS-C-protocol visit www.ichaus.de/BiSS Interface.

For BiSS C point-to-point communication the required RS422 transceiver is integrated on the chip and has both a differential clock input and a differential line driver for data output. If iC-MNF is to be used in a BiSS daisy chain, it is recommended to use external RS422 line drivers. By using external transceivers the delay time can be evenly spread. More detailed information can be found in corresponding application notes.

A communication frame ends when the MA pin clock cycles stop. After the last edge on MA the communication timeout begins. With NTOA set to 0 the timeout is adaptive. The timeout period t_{out} is calculated based on the first MA edges as shown in Figure 6. By setting NTOA to 1 a fixed timeout of 20 µs terminates the communication frame.

NTOA Addr. 0x33; bit 0		
Code	Description	Timeout *)
0 1	Adaptive Fixed	t_{init} 20 µs
Note	*) see l108, p. 17	

Table 64: Communication Timeout

In BiSS protocol iC-MNF uses fixed CRC polynomials, see Table 65. The single cycle data (SCD), i.e. the primary data which is newly generated and completely transmitted in each cycle, contains the position data (optional multiturn + singleturn) and the error and warning bit. With CID_SCD a CRC start value can be selected, thus enabling a PLC to clearly allocate data to the source (for safety applications). The CRC value is output inverted.

data-channel*)	type of CRC	CRC HEX Code	Polynomial
SCD (sensor)	normal (MODE_SER = 0x0) extended (MODE_SER = 0x1)	0x43 0x190D9	x^6+x^1+1 $x^{16}+x^{15}+x^{12}+x^7+x^6+x^4+x^3+1$
CDM, CDS (register)	-	0x13	x^4+x^1+1
Note	*) explanation s. BiSS-C specification		

Table 65: BiSS CRC polynomials

CID_SCD Addr. 0x3D; bit 7:4	
Code	CRC start value SCD
0x0 . . . 0xF	CID_SCD

Table 66: CRC start value for SCD

iC-MNF has a 15-bit busy shift register. If, for example, two identically configured iC-MNFs are connected up to the BiSS master as slaves in a chain, with the help of the busy shift register an internal clock jitter can be avoided which could lead to different data conversion times for the two slaves. Should the busy shift register not be sufficient, i.e. should iC-MNF need longer to convert data than the subsequent slave, iC-MNF generates the start bit and marks the data it has output as faulty. This ensures that the data of the subsequent slave is not lost.

BiSS: Protocol Commands

The following BiSS interface protocol commands are implemented.

CD Channel: BiSS Protocol Commands		
CMD	Availability	Function
Addressed		
00	Yes	Activate Single-Cycle Data channels
01	Yes*	Deactivate control communication
10	Yes	Execute SOFT_PRES_E2P[1]
11	Yes	Execute CRC_CHECK[1]
Broadcast (all slaves)		
00	Yes	Deactivate Single-Cycle Data channels
01	Yes	Activate control communication
10	—	Reserved
11	—	Reserved
Notes	* Command works only if ETS = 1. [1] Description of commands see p. 93	

Table 67: BiSS Protocol Commands

BiSS protocol commands 0 and 1 can be used for BiSS bus establishment if more than 8 Slaves are connected to the BiSS Master and can be disabled with PROT_INS = 0x1.

PROT_INS	Addr. 0x44; bit 5	
PROT_INS	Addr. SER:0x14; bit 5	Bank 1
Code	BiSS Commands 0 and 1	
0x0	enabled	
0x1	disabled	

Table 68: Disable BiSS commands 0 and 1

Note:
With PROT_CMD the execution of BiSS Protocol Commands 0x2 and 0x3 (see p. 94) can be disabled.

BiSS: Output Data Length

The total output bit count is derived from the parameters DL_ST, DL_MT, CDL_MT, ECDL_MT, DL_ZERO, ELC and MODE_SER. The BiSS protocol always transmits two additional bits for the error and warning messages. Additional zeros can be configured with DL_ZERO and are inserted between the user data and the error/warning.

$datalength_{BiSS}$ = *bits(DL_ST) + bits(DL_MT, CDL_MT, ECDL_MT) + bits(DL_ZERO) + error + warning + bits(ELC) +* $bits_{CRC}$*(MODE_SER)*

BiSS: Safety Application Settings

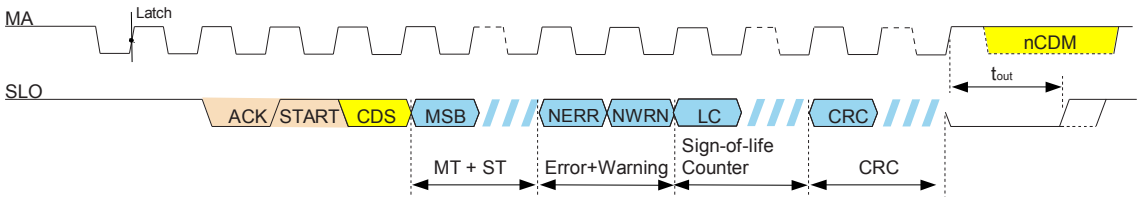


Figure 22: Example of line signals for BiSS C protocol with sign-of-life counter

For safety applications the iC-MNF offers:

- the transmission of a sign-of-life counter
- the usage of a 16 bit Extended-CRC
- the usage of CID_SCD as a start-value for the CRC calculation

It is possible to transmit a sign-of-life counter value in the sensor data for safety applications. When the sign-of-life counter is activated, a 6-bit counter value is transmitted in the sensor data which is incremented with each new sensor data readout. The sign-of-life counter has a range of 1 to 63.

ELC	Addr. 0x3B; bit 7
Code	Function
0x0	Sign-of-life counter not active
0x1	Sign-of-life counter (6 bit) enabled

Table 69: Sign-of-life counter

With MODE_SER = 0x1 it is possible to configure BiSS to use a 16 Bit CRC (see Table 63, 65).

The parameter CID_SCD (see Table 66) can be used to facilitate the allocation of the received data to a specific slave if more than one BiSS-Slave is connected to the PLC.

SSI Protocol[1]

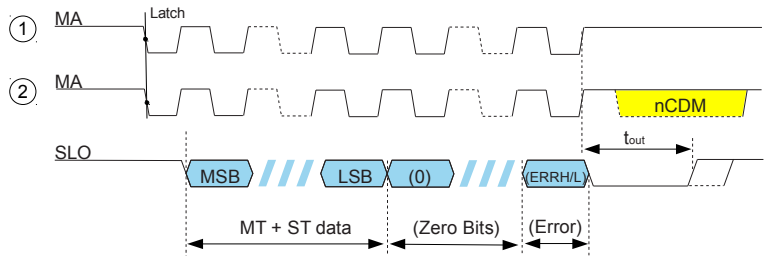


Figure 23: Example of SSI line signals:
(1) Standard SSI, (2) Advanced SSI protocol

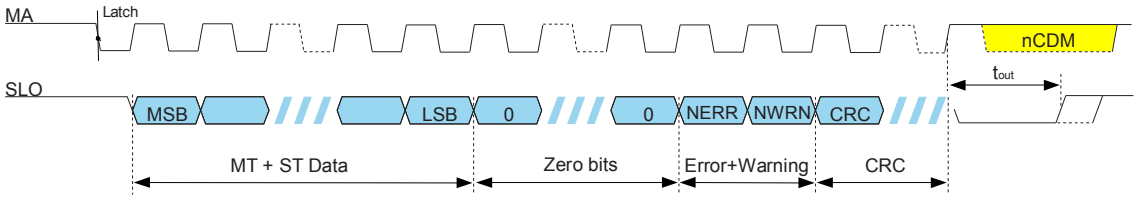


Figure 24: Example of extended SSI line signals (MODE_SER = 0xF, ExtSSI)

MODE_SER	
Code	Protocol
0x2	SSI binary
0x3	SSI binary +ERRL
0x4	SSI binary +ERRH
0x5	SSI gray
0x6	SSI gray +ERRL
0x7	SSI gray +ERRH
0x9	RSSI binary
0xA	RSSI binary +ERRL
0xB	RSSI binary +ERRH
0xC	RSSI gray
0xD	RSSI gray +ERRL
0xE	RSSI gray +ERRH
0xF	ExtSSI

Table 70: Interface protocol SSI

more unidirectional register communication (Advanced SSI protocol see Fig. 23) is supported.

The standard SSI protocol (MODE_SER = 0x2-0x7, 0x9-0xE) can be extended with a parity bit. If activated with PAR_SSI the parity bit comes last in the sensor data word. The polarity of the parity bit can be configured with CID_SCD, Bit 0 (see Table 66).

PAR_SSI	Addr. 0x33; bit 1		
Code	SSI data	CID_SCD(0) = 0	CID_SCD(0) = 1
0x0	no parity bit	-	-
0x1	with parity bit	Odd	Even
Note	Only for MODE_SER = 0x2-0xE		

Table 71: Parity Bit SSI: Even or Odd

iC-MNF can transmit position data according to the SSI protocol where both data length and error messaging are configurable. The error bit can be configured to be high active (ERRH) or low active (ERRL). The sensor data can be output in binary or Gray code. The format option Gray or binary code covers the MT and ST data word in its entirety; filled in zeros (DL_ZERO, see Table 58) and the error bit remain untouched. The data package containing sensor data optional zero bits and an optional error bit is terminated by a stop (0). Furthermore, the SSI ring mode (RSSI) can be used for the repeated output of position data in the SSI protocol. The repeated position data is separated by a zero-bit. The position is repeated until the SSI timeout t_{out} (see Fig. 3, p. 18) elapses. After t_{out} has elapsed a new request can be made for position data. By checking the repeated position data for equality, the SSI ring operation mode enables any possible transmission error to be detected. If the SSI ring operation (RSSI) is deactivated, zeros are subsequently output after the position data output.

[1] For iC-MNF X1: Please refer to the design review on p. 106.

In extended SSI mode (ExtSSI, see Fig. 24) the multiturn data (optional), singleturn data, error, warning, sign-of-life counter (optional) and CRC can be read out. All data is sent with the MSB first and is equivalent to the data package that is output when using the BiSS protocol.

Note:
The selected mode of operation MODE_ST for the sine-to-digital conversion can limit the permissible SSI clock frequency (see Operating Conditions on p. 17). The highest possible SSI clock frequency of 4 MHz is permissible for converter modes with an immediate data output (e.g., MODE_ST with cyclic background conversion see p. 67).

NTOA	Addr. 0x33; bit 0	
Code	Description	Timeout *)
0	Adaptive	t_{init}
1	Fixed	20 µs
Note	*) see I102, p. 17	

Table 72: Communication Timeout

It is possible to select the adaptive or the fixed timeout in SSI mode. However in order to meet the requirements of the standard SSI protocol the fixed timeout of 20 µs should be chosen by setting NTOA to 1.

SSI: Output Data Length
The total output bit count in the standard SSI mode (MODE_SER = 0x2-0x7, 0x9-0xE) is derived from the parameters DL_ST, DL_MT, CDL_MT, ECDL_MT, DL_ZERO, PAR_SSI and MODE_SER. The parameter DL_ZERO can be used to fill a SSI data word with zeros if DL_ST is less than 13 bits and 13/25-bit Standard SSI is desired. Additional zeros configured with DL_ZERO are inserted between the user data and the optional error bit.

$datalength_{SSI}$ = *bits(DL_ST) + bits(DL_MT, CDL_MT, ECDL_MT) + bits(DL_ZERO) + optional(error) + optional(PAR_SSI)*

For the output data length in the extended SSI mode (ExtSSI, MODE_SER = 0xF) please refer to chapter **BiSS: Output Data Length**, p. 47.

SPI Protocol

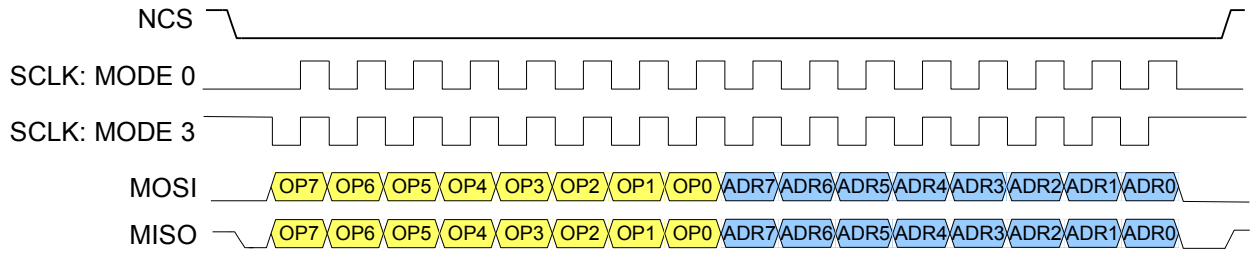


Figure 25: SPI transmission SPI-Mode 0 and 3, using opcode Read REGISTER(single) as an example

MODE_SER					
Code	MAO	MA	SLI	NSLO	Function
0x8	NCS	SCLK	MOSI	MISO *)	SPI
Note	*) tristate if NCS = 1; for further settings of pin NSLO see SLO_LS, SLO_SC: Table 43, 44; p. 37				

Table 73: Pins used for interface protocol SPI

In interface mode SPI the MISO pin is set to tristate if the slave is not selected by the master, i.e. NCS=1. This function is used for a parallel SPI bus configuration (Figure 26).

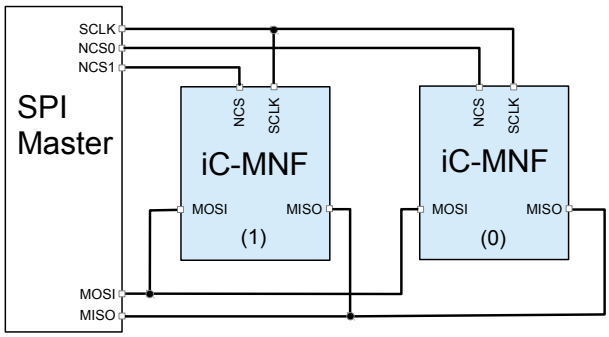


Figure 26: Example configuration SPI bus with 2 parallel Slaves

SPI modes 0 and 3 are supported, meaning that the idle state of SCLK is 0 or 1. Data is always accepted on the rising edge of SCLK and is sent in 8-bit packages with the MSB first (see Figure 25). Each data transmission starts with the master sending an opcode (Table 74) to the slave.

The following describes the typical sequence of an SPI data transmission, taking the command **Read REGISTER (single)** as an example (see Figure 25):

1. Master initiates a transaction with a falling edge on the chip select input (NCS).
2. iC-MNF feeds MOSI through to MISO.
3. Master sends opcode OP and address ADR on MOSI; iC-MNF feeds OP and ADR through to MISO.
4. Master ends the transaction with a rising edge on NCS.
5. iC-MNF switches its MISO output to tristate.

OPCODE	
Code	Description
0xB0	ACTIVATE
0xA6	SDAD-transmission (sensor data + EW + opt(LC))
0xF5	SDAD Status
0x97	Read REGISTER(single)
0xD2	Write REGISTER (single)
0x81	Read REGISTER (cont.) delayed
0xCF	Write REGISTER (cont.)
0x9C	Read STATUS (STATUS0..STATUS4)
0xD9	Write INSTRUCTION (MNF_CMD)
0xAD	REGISTER status/data

Table 74: SPI OPCODEs

SPI: Output Data Length
To be compatible with the SPI protocol, it must be ensured that the sensor data output length is a multiple of 8 bits when setting the sensor data length for the command **SDAD transmission**.

The bit count for the sensor data output with SPI command **SDAD transmission** is derived from the parameters DL_ST, DL_MT, CDL_MT, ECDL_MT and DL_ZERO. The parameter DL_ZERO can be used to achieve multiples of 8 bits for the data length, see chapter **Serial Interface: Configuring Data Length And Code Direction**, p. 44 for details.

$datalength_{SPI}$ = *bits(DL_ST) + bits(DL_MT, CDL_MT, ECDL_MT) + bits(DL_ZERO) + error + warning + (6 zero-bits or sign-of-life counter (ELC))*

SPI: Command ACTIVATE

OPCODE	
Code	Description
0xB0	ACTIVATE

Table 75: SPI Opcode: ACTIVATE

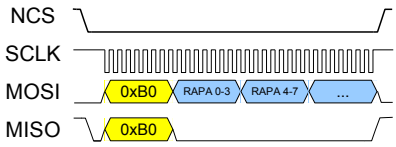


Figure 27: Set ACTIVATE: RACTIVE/PACTIVE (several slaves)

The **ACTIVATE** command turns the register and sensor data channels of the connected slaves on and off individually. Each iC-MNF has one RACTIVE register to activate or deactivate the register data channel and one PACTIVE register to activate or deactivate the sensor data channel.

The command causes all slaves to reset their RACTIVE and PACTIVE registers, turning both channels off, and resets the bits FAIL, VALID, BUSY, and DISMISS in the SPI-STATUS byte (see Table 88). The RACTIVE (RA) and PACTIVE (PA) bits in the data byte following the opcode then activate or deactivate one or both channels for subsequent transactions.

With only one iC-MNF slave connected (one register and one sensor data channel) the RA and PA bits are bits 1 and 0 respectively in the data byte following the opcode as shown in Fig. 28.

After startup RACTIVE and PACTIVE are set to 1, meaning register and sensor data channels are enabled by default.

RACTIVE	
Code	Description
0	Register communication deactivated
1	Register communication activated*)
PACTIVE	
Code	Description
0	Sensor data channel deactivated
1	Sensor data channel activated*)
Note	*) default after startup

Table 76: RACTIVE and PACTIVE bits

With RACTIVE = 0 the register data channel is deactivated and when using the commands **Read REGISTER (single), Write REGISTER (single), Read REGISTER (cont.) delayed, Write REGISTER (cont.), REGISTER status/data** the ERROR bit is set in the SPI-STATUS byte (see Table 88) to indicate that the command has not been executed. At MISO the slave immediately outputs the data transmitted by the master via MOSI.

With PACTIVE = 0 the sensor data channel is deactivated and when using the commands **SDAD status** or **SDAD transmission** the ERROR bit is set in the SPI-STATUS byte (see Table 88) to indicate that the command has not been executed. At MISO the slave immediately outputs the data transmitted by the master via MOSI.

Note: If two or more devices are connected to a chain (see Figure 29), the master can determine the number of the connected register and sensor data channels with the command **ACTIVATE**. To achieve this, the master can transmit a high level after the opcode, which is repeated at MISO after the number of register/sensor data channels (see Figure 28).

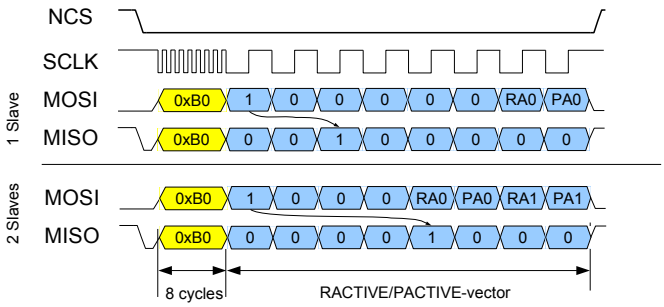


Figure 28: Set ACTIVATE: RACTIVE/PACTIVE (Example with one and two slaves (daisy chain), the shift of the single '1' after the opcode could be used to detect how many slaves are connected)

An example for a daisy chain wiring of 2 SPI slaves is given in Figure 29. In order to do register communication (**Read REGISTER (single), Write REGISTER (single), Read REGISTER (cont.) delayed, Write REGISTER (cont.), REGISTER status/data**) with e.g., slave (1) the register communication has to be enabled explicitly for this slave and disabled for slave (0) with command **ACTIVATE** and parameter **RACTIVE**.

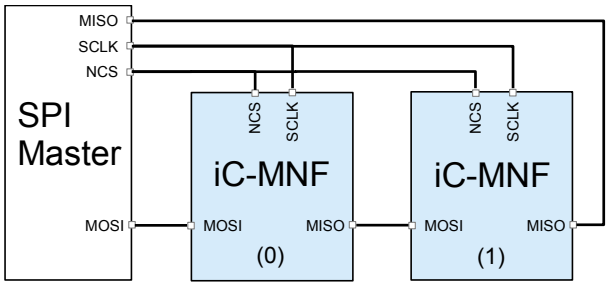


Figure 29: Example configuration with 2 Slaves (daisy chain)

SPI: Command SDAD transmission

OPCODE	
Code	Description
0xA6	SDAD-transmission (sensor data + EW + opt(LC))

Table 77: SPI Opcode: SDAD-transmission

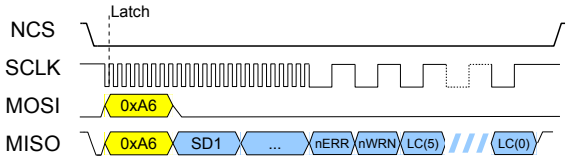


Figure 30: SDAD transmission: read SD

iC-MNF latches the absolute position on the first rising edge at SCLK, when NCS is at zero (Latch). In the case that iC-MNF is configured to output cyclically generated data, previously converted data or data triggered by pin T3 (see Table 110 and 111), the master can transmit the **SDAD transmission** command directly.

After the opcode the sensor data shift register is clocked out. The length of the sensor data shift register should match multiples of 8 (see chapter **SPI: Output Data Length**, p. 51).

The sensor data (SD) is transmitted binary with the MSB first and is terminated with an EW-byte including one error bit and one warning bit (both low active) and optionally six bits sign of life counter (LC). If no sign of life counter is configured (see Table 78) zeros are transmitted.

ELC	Addr. 0x3B; bit 7
Code	Function
0x0	Sign-of-life counter not active
0x1	Sign-of-life counter (6 bit) enabled

Table 78: Sign-of-life counter

In the case that iC-MNF needs processing time to generate output data command **SDAD status** must be used to request new sensor data and to cyclically check for the end of the sensor data generation.

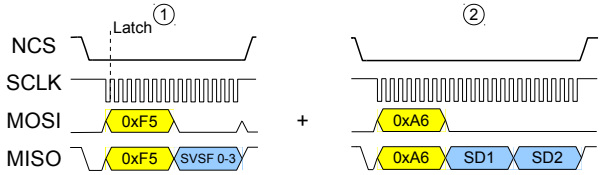


Figure 31: SDAD transmission: request SD with SDAD status followed by SD readout with SDAD transmission

If the internal data generation was not completed but data is sampled in the sensor data shift register, the ERROR bit is set in the SPI-STATUS byte (see Table 88) and the output data bytes are set to zero.

SPI: Command SDAD status

OPCODE	
Code	Description
0xF5	SDAD Status

Table 79: SPI Opcode: SDAD Status

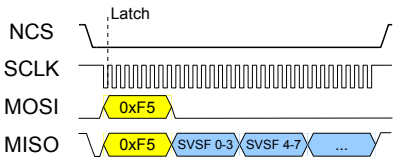


Figure 32: SDAD status

If the master does not know the processing time of the connected slaves, it can request sensor data using the command **SDAD status**. Each iC-MNF has one SVALID (SV) register to signal the end of conversion and one SFAIL (SF) register to signal a failing sensor data request.

The **SDAD status** command causes:

1. All slaves activated with PACTIVE = 1 (see Tab. 76) to output their SVALID and SFAIL registers in the data byte following the opcode.
2. The next request for sensor data started with the first rising edge at SCLK of the next SPI communication is ignored by the slave.

Using this command, the master can cyclically poll for the successful end of the sensor data generation sig-

naled with SVALID (SV). The sensor data is read out with the command **SDAD transmission**.

If SFAIL (SF) is set, requesting new sensor data on the first rising edge at SCLK of the next SPI communication is enabled again.

Note:
If both SVALID (SV) and SFAIL (SF) are set, the sensor data is invalid.

SVALID	
Code	Description
0	Sensor data generation in progress
1	Sensor data ready
SFAIL	
Code	Description
0	Sensor data request okay
1	Sensor data request failed

Table 80: SVALID and SFAIL bits

If only one slave is connected, the corresponding SVALID (SV0) and SFAIL (SF0) bits are placed at bit positions 7 and 6 in the SVALID byte as shown in Fig. 33.

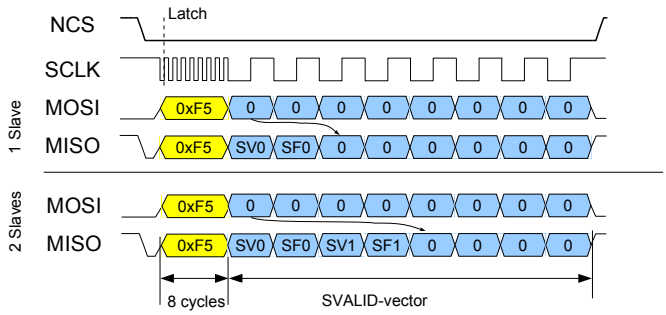


Figure 33: SDAD status (Example with one and two slaves (daisy chain, see Fig. 29))

Figure 34 shows the interaction of the two commands **SDAD Status** and **SDAD transmission**. The sensor data communication starts with the command **SDAD Status** (1). The first **SDAD Status** requests new data. Following **SDAD Status** commands are used to check for the data to be ready to output (no new sensor data requests are issued). If the sensor data is signaled to be ready with SVALID the command **SDAD-transmission** (2) is executed to read out the sensor data. At this point sensor data requests are enabled again. Finally the command **REGISTER status/data** should be executed to detect an unsuccessful SPI communication.

Note:
It is recommended to define a maximum wait time for SVALID/SFAIL. After this timeout has elapsed, the current sensor data request should be interrupted with, e.g. the REGISTER status/data command.

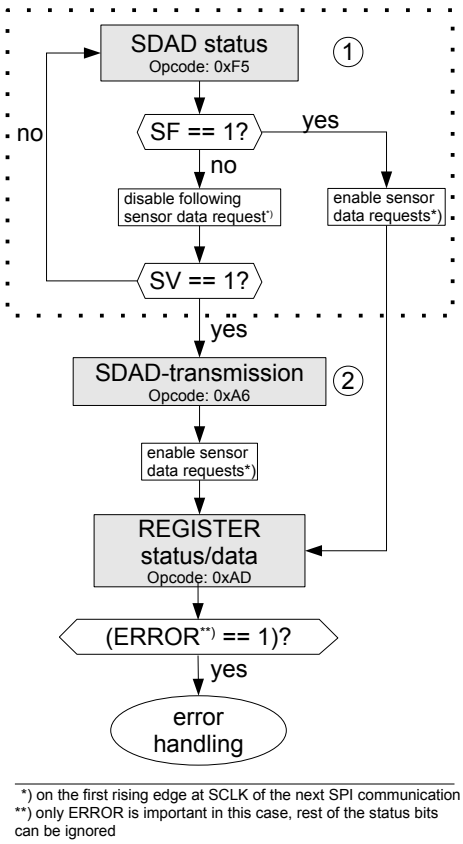


Figure 34: Example sequence of the commands SDAD Status/SDAD-transmission

SPI: Command Read REGISTER (single)

OPCODE	
Code	Description
0x97	Read REGISTER (single)

Table 81: SPI Opcode: Read REGISTER (single)

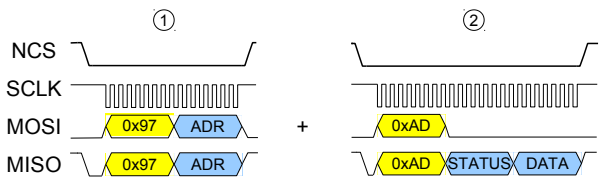


Figure 35: Read REGISTER (single): set the read address (1) + command REGISTER status/data to read-out data (2)

This command enables register data to be read out from the slave byte by byte.

The master first transmits the **Read REGISTER (single)** command followed by the address ADR. The slave immediately outputs the command and address at MISO.

Following this, using the **REGISTER status/data** command (see p. 57) the master can poll until the validity of the DATA following the SPI-STATUS byte is signaled via SPI-STATUS.

SPI: Command Write REGISTER (single)

OPCODE	
Code	Description
0xD2	Write REGISTER (single)

Table 82: SPI Opcode: Write REGISTER (single)

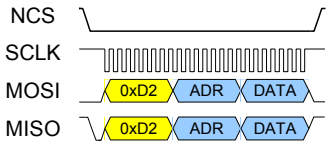


Figure 36: Write REGISTER (single); set write address and Data

This command enables data to be written to the slave byte by byte.

The master first transmits the **Write REGISTER (single)** command followed by the address ADR and the data (DATA). The slave immediately outputs the command, address, and data at MISO.

It is recommended to use the **REGISTER status/data** command after the command **Write REGISTER (single)** and all other REGISTER commands to check if the register communication was successful. In case iC-MNF needs processing time e.g. write register data to the EEPROM, the SPI master can use the **REGISTER status/data** command to poll the end of procedure.

SPI: Command Read REGISTER (cont.) delayed

OPCODE	
Code	Description
0x81	Read REGISTER (cont.) delayed

Table 83: SPI Opcode: Read REGISTER (cont.) delayed

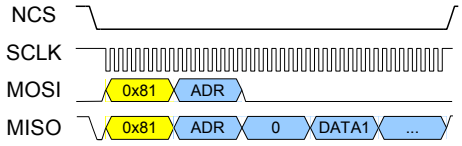


Figure 37: Read REGISTER (cont.)

The **Read REGISTER (cont.)** command can be used to read registers where iC-MNF does not need processing time to provide the corresponding data.

Each of the following register areas can be read using **Read REGISTER (cont.)**:

- Addr. 0x00 - 0x3F (64 bytes) with I2CDEV = 0x0 and BSEL = 0x0
- Addr. 0x00 - 0x29 (42 bytes) with I2CDEV = 0x0 and BSEL = 0x1
- Addr. 0x40 (only 1 byte)
- Addr. 0x41 (only 1 byte)
- Addr. 0x6B (only 1 byte)
- Addr. 0x6C - 0x6F (4 bytes)
- Addr. 0x72 - 0x76 (5 bytes)

The master transmits the **Read REGISTER (cont.) delayed** opcode. In the second byte the start address ADR is transmitted. The slave immediately outputs the opcode and the address followed by a ZERO-byte and then transmits the DATA1 data. The internal address counter is incremented following each data packet.

If an error occurs during register readout in continuous mode (e.g. the address is invalid or the requested data is not yet valid on data byte clock out), the internal address counter is no longer incremented and the error bit FAIL is set in the communication status register (see page 57).

Note:
The command **Read REGISTER (cont.) delayed** can not be used to continuously read data from an external EEPROM as iC-MNF needs processing time to obtain the data.

The status of the register communication should be checked using the **REGISTER status/data** command.

SPI: Command Write REGISTER (cont.)

OPCODE	
Code	Description
0xCF	Write REGISTER (cont.)

Table 84: SPI Opcode: Write REGISTER (cont.)

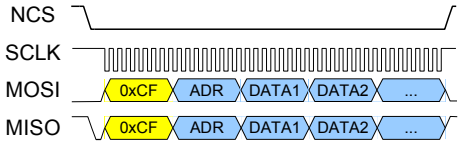


Figure 38: Write REGISTER (cont.)

The **Write REGISTER (cont.)** command can be used for internal registers where iC-MNF does not need processing time to write the corresponding data.

Data can be written to the following register areas using **Write REGISTER (cont.)**:

- Addr. 0x00 - 0x3F (64 bytes) with I2CDEV = 0x0 and BSEL = 0x0
- Addr. 0x00 - 0x29 (42 bytes) I2CDEV = 0x0 and BSEL = 0x1
- Addr. 0x40 (only 1 byte)
- Addr. 0x77 (only 1 byte)

The master transmits the **Write REGISTER (cont.)** opcode. In the second byte start address ADR is transmitted, followed by the DATA1-DATAn data packets to be written. The slave immediately outputs the opcode, address and data at MISO. The slave increments its internal address counter following each data packet.

If an error occurs during the write access to the registers in continuous mode (e.g. the address is invalid or the data write process of the last address was not finished), the internal address counter is no longer incremented and the error bit FAIL is set in the communication status register (see page 57).

Note:
The command **Write REGISTER (cont.)** can not be used to continuously write data to an external EEPROM as the communication between iC-MNF and the EEPROM needs processing time.

The status of the register communication should be checked using the **REGISTER status/data** command.

SPI: Command Read STATUS

OPCODE	
Code	Description
0x9C	Read STATUS (STATUS0..STATUS4)
Note	STATUS0..STATUS4 see p. 86 ff.

Table 85: SPI Opcode: Read STATUS

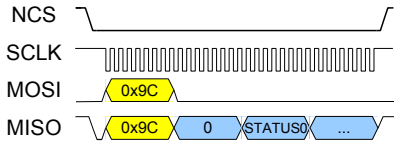


Figure 39: Read STATUS

The command **Read STATUS** is designed to enable a fast readout of the internal, iC-MNF status registers (STATUS0...STATUS4). With the opcode the address is set to the STATUS0 address (see Tab. 144). The opcode is followed by a ZERO-byte and the STATUS0 to STATUS4 bytes. The internal address counter is incremented following each STATUSx byte.

The status of the register communication should be checked using the **REGISTER status/data** command.

SPI: Command Write INSTRUCTION

OPCODE	
Code	Description
0xD9	Write INSTRUCTION (MNF_CMD)
Note	MNF_CMD see p. 93 ff.

Table 86: SPI Opcode: Write INSTRUCTION

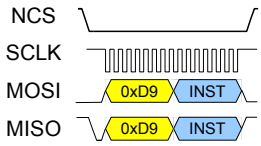


Figure 40: Write INSTRUCTION

The command **Write INSTRUCTION** is designed to enable a fast setting of the internal, slave-specific command registers. With the opcode the address is set to the MNF_CMD register address (see Tab. 165). The instruction data byte (INST) is send directly after the OPCODE byte.

The status of the register communication should be checked using the **REGISTER status/data** command.

ATTENTION:
After the execution of the HARD_RES command, the SPI interface must be reset. After sending the HARD_RES command, wait for a time of tready()cfg * 1.3 (see Elec. Char. 904). Then the REGISTER status/data opcode must be sent. The read-back value can be discarded.

SPI: Command REGISTER status/data

OPCODE	
Code	Description
0xAD	REGISTER status/data

Table 87: SPI Opcode: REGISTER status/data

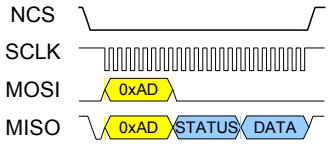


Figure 41: REGISTER status/data

The **REGISTER status/data** command returns the SPI-STATUS byte which indicates the status of the last register transaction or data transmission.

As shown in Figure 41, the SPI-STATUS byte is returned immediately following the **REGISTER status/-data** opcode and is followed by a DATA byte.

The SPI-STATUS bits are updated with every register access, except bit ERROR, which indicates the status of the last SPI-communication with the slave (see Tab. 88).

SPI-STATUS		
Bit	Name	Description of the status report
7	ERROR	Opcode not implemented, Sensor data was not ready for output
6..4	-	Reserved
Status Bits of the register communication		
3	DISMISS	Address rejected
2	FAIL	Data request has failed
1	BUSY	Slave is busy with a request
0	VALID	DATA is valid/register communication terminated successfully
Note	Display logic: 1 = true, 0 = false	

Table 88: Communication status byte

Following the **Read REGISTER (single)** command the requested data byte is returned via DATA . The validity of the DATA byte is signaled with the VALID status bit.

Following the **Write REGISTER (single)** command, the data to be written is repeated in the DATA byte. With all other opcodes, the DATA byte is not defined.

In general bits 0 to 3 of the SPI-STATUS byte reflect the status of the register communication.

Figure 42 shows the sequence of the commands **read-/write REGISTER (single/cont), read STATUS, write INSTRUCTION** and **REGISTER status/data**.

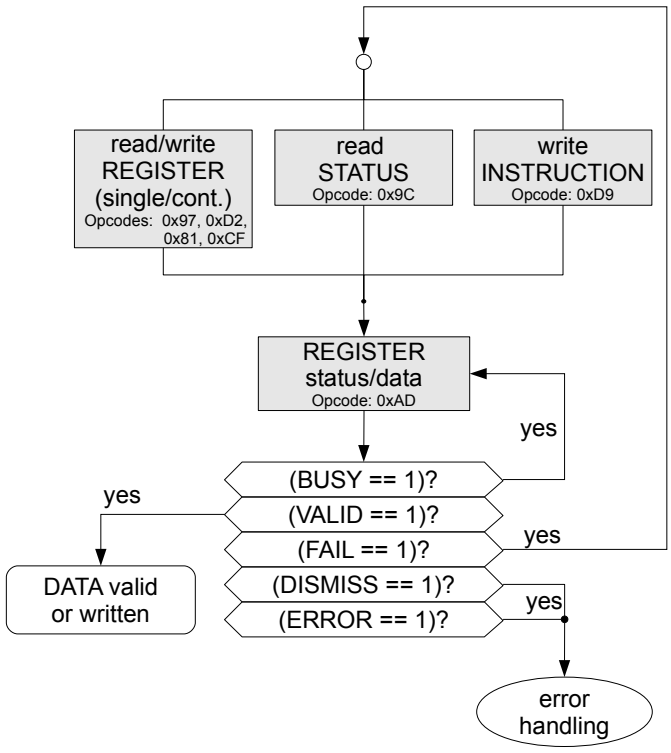


Figure 42: Example sequence of REGISTER SPI commands and REGISTER status/data

REGISTER ACCESS USING THE I/O INTERFACE

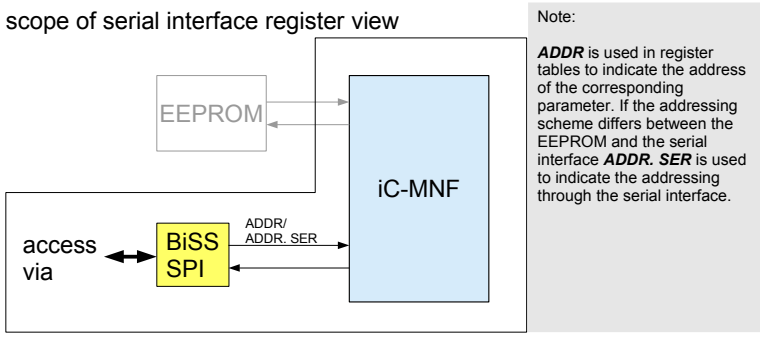


Figure 43: Scope of register mapping serial I/O interface

The abbreviation *Addr.* is used in the register tables of this specification to indicate the address of the corresponding parameter. If the addressing scheme differs between the EEPROM and the serial I/O interface *Addr. SER* is used to indicate the addressing when using the serial I/O interface.

Memory Map And Register Access

The distribution of the addresses in iC-MNF corresponds to the document BiSS C Protocol Description which can be downloaded at www.ichaus.de/BiSS Interface.

iC-MNF supports an addressing scheme using banks. Therefore the internal address space is divided into banks of 64 bytes each. The address sections visible via the I/O interface recognizes a ”dynamic” section (Addr SER: 0x00 to 0x3F, content selectable with BSEL) and a ”static” section which is permanently visible (Addr SER: 0x40 to 0x7F, content independent of BSEL). The content of the static part is shown in Table 91.

The different memory banks can be addressed with BSEL. I2CDEV changes the I2C Device ID. This enables access to I2C slaves others than the configuration EEPROM, which are connected to the same I2C bus using different I2C Device IDs, e.g., external multiturn devices.

BSEL	Addr. SER:0x40; bit 4:0	
Code	Bank	Resulting 11 bit address: BSEL(4:0) & Addr. SER(5:0)
0x0	Bank 0	0x000-0x03F
0x1	Bank 1	0x040-0x07F
...	...	
0x1F	Bank 31	0x7C0-0x7FF

Table 89: BSEL: Bank selection and resulting addresses with Addr. SER: 0x00...0x3F

I2CDEV	Addr. SER:0x40; bit 7:5
Code	I2C Device-ID*) (binary representation)
0x0	101 0 xxx **)
0x1	101 1 xxx
0x2	100 0 xxx
0x3	100 1 xxx
0x4	111 0 xxx
0x5	111 1 xxx
0x6	110 0 xxx
0x7	110 1 xxx
Note	*) first 7 bit of I2C addressing sequence (Fig. 16): 4 bit Dev. ID + upper 3 bit of 11 bit addr. (see Table 89) shown as don't care (x) **) standard EEPROM Device ID refer to Table 91 and Fig. 46 to see whether an I2C communication is started

Table 90: I2CDEV: I2C device ID

Figure 44 illustrates the principle of the bank-wise addressing scheme using BSEL. Figure 46 gives a detailed overview including memory mapping and register protection levels.

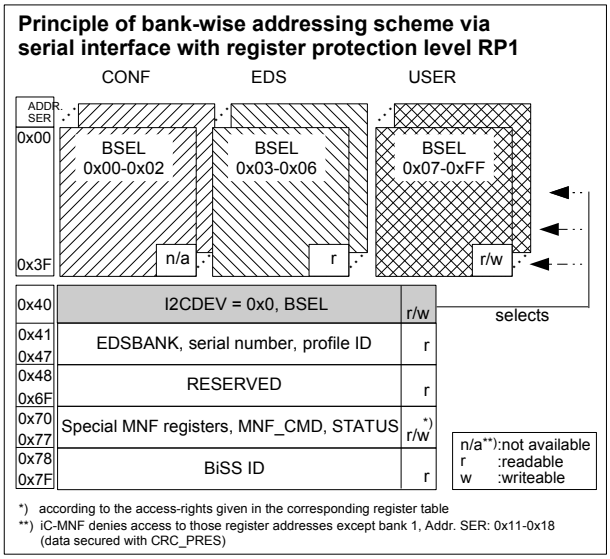


Figure 44: Principle of bank-wise memory addressing and access restrictions with register protection level RP1 (I2CDEV = 0x0)

The address translation to address an EEPROM device (I2C Device-ID = 0xA) via the bank register (BSEL = 0x0 . . . 0x1F) is shown in Table 91 and in Fig. 46.

Note:
To use the bank-wise addressing scheme shown in Figure 44 the parameter I2CDEV must be set to 0x0.

Code	Bank	Addr. SER	Memory location	Type of data
CONF	0	0x00-0x3F	internal register	config. data
	1	0x00-0x29	internal register	
	1	0x2A-0x3F	E2P: 0x06A-0x07F	
	2	0x00-0x3F	E2P: 0x080-0x0BF	
EDS	3	0x00-0x3F	E2P: 0x0C0-0x0FF	**E**lectronic-**D**ata-**S**heet
	. . .	. . .	. . .	
	6	0x00-0x3F	E2P: 0x180-0x1BF	
USER	7	0x00-0x3F	E2P: 0x1C0-0x1FF	OEM data, free user area
	. . .	. . .	. . .	
	31	0x00-0x3F	E2P: 0x7C0-0x7FF	
Note	refer also to Fig. 46			

Table 91: Address translation Addr Ser: 0x00-0x3F with I2CDEV = 0x0

Application Hint:
The minimum requirement for the external EEPROM is an 24C02 EEPROM with 256 Byte memory. However in order to cover the sections CONF, EDS and USER (with 1 USER Bank) at least an 24C04 EERPOM with 512 Byte memory should be used. For further EEPROM requirements see p. 39.

Static part: Addresses 0x40-0x7F								
Addr. SER	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x40	I2CDEV			BSEL				
0x41	R: EDSBANK(7:0)							
0x42	PRO_ID0(15:8)							
0x43	PRO_ID0(7:0)							
0x44	SER_NO(31:24)							
0x45	SER_NO(23:16)							
0x46	SER_NO(15:8)							
0x47	SER_NO(7:0)							
0x48 ... 0x6A	Reserved							
0x6B	STAT_CIF	0	0	1	0	STAT_CAL(2:0)		
0x6C	TEMP(7:0)							
0x6D (R)	DMAX_N(3:0)				DMIN_N(3:0)			
0x6E (R)	DMAX_S(3:0)				DMIN_S(3:0)			
0x6E (W)	PROT_E2P_RES(7:0)							
0x6F	CHIP_REL(7:0)							
0x70	STATEXT0(7:0)							
0x71	STATEXT1(7:0)							
0x72	STATUS0(7:0)							
0x73	STATUS1(7:0)							
0x74	STATUS2(7:0)							
0x75	STATUS3(7:0)							
0x76	STATUS4(7:0)							
0x77	MNF_CMD(7:0)							
0x78	DEV_ID(47:40)							
0x79	DEV_ID(39:32)							
0x7A	DEV_ID(31:24)							
0x7B	DEV_ID(23:16)							
0x7C	DEV_ID(15:8)							
0x7D	DEV_ID(7:0)							
0x7E	MFG_ID(15:8)							
0x7F	MFG_ID(7:0)							

Table 92: Register map addresses 0x40-0x7F (access via serial I/O interface; content independent of I2CDEV, BSEL)

The current iC-MNF chip release can be read out with parameter CHIP_REL.

CHIP_REL	Addr. SER:0x6F; bit 7:0
Code	Chip version
0x04	iC-MNF Y
0x05	iC-MNF Y1
0x07	iC-MNF X1
0x09	iC-MNF X3

Table 93: Chip release iC-MNF

Register Protection Levels

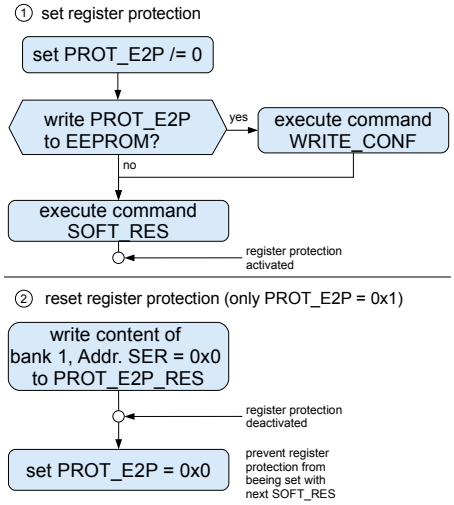


Figure 45: Setting/resetting register protection

PROT_E2P Addr. 0x40; bit 5:4 **PROT_E2P** Addr. SER:0x0; bit 5:4 Bank 1		
Code	Mode and restrictions	Register protection level (RPL)
0x0	Configuration mode -no restrictions	RP0
0x1 *)	Shipping mode -reset to RP0 possible -command **WRITE_CONF** writes only the PRES_ST/MT values	RP1
0x2 *)	Shipping mode -no reset to RP0 possible -command **WRITE_CONF** writes only the PRES_ST/MT values	RP1
Note	*) The command SOFT_RES should be executed for the register protection to take effect	

Table 94: Register access control

Register access can be restricted using PROT_E2P (see Table 94). PROT_E2P = 0x1 selects a shipping mode with limited access which can be set back to PROT_E2P = 0x0. To set back PROT_E2P the content of Bank: 1, Addr. SER: 0x0 (q.v. Addr. 0x40, register layout digital parameters p. 25) has to be written to PROT_E2P_RES.

Note:
After setting PROT_E2P to RP1 the command SOFT_RES should be executed for register protection to take effect.
If PROT_E2P with enabled register protection should be written to the external EEPROM the command WRITE_CONF should be executed before command SOFT_RES.

Note:
Once the shipping mode RP1 is activated, command **WRITE_CONF** only writes the configuration data secured with CRC_PRES to the EEPROM addresses 0x49...0x59.

PROT_E2P_RES Addr. SER:0x6E; bit 7:0 W	
Code	Description
0x00 . . . 0xFF	Set back value for PROT_E2P
Note	The set back value is equivalent to the content of Bank: 1, Addr. SER: 0x0 (q.v. EEPROM Addr. 0x40)

Table 95: Set back value for RPL

Sections CONF, EDS and USER are protected at different levels in shipping mode for read and write access (see Figure 46).

PROT_E2P			
	Section		
	CONF	EDS	USER
RPL	BANK = 0-2	BANK = 3-6	BANK > 6
RP0	r/w	r/w	r/w
RP1	n/a *)	r	r/w
	n/a *): iC-MNF denies access to those register addresses except bank 1, Addr. SER: 0x11-0x18 (data secured with CRC_PRES) r: Registers are readable w: Registers are writeable		

Table 96: Register Read/Write Protection Levels

Overview Register Access: Memory Mapping, Register Protection Levels

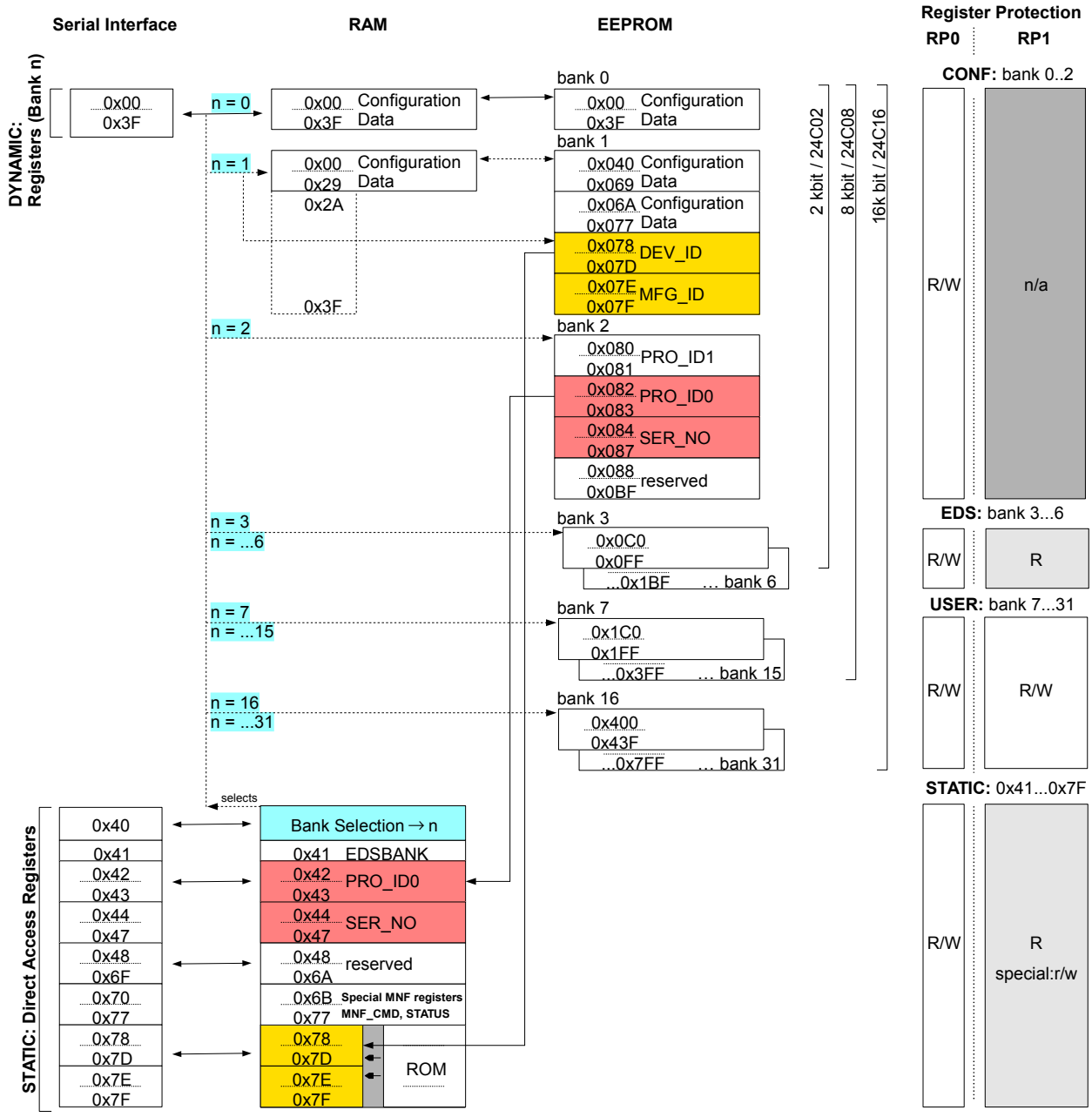


Figure 46: Bankwise memory addressing via I/O interface (I2CDEV = 0x0, BSEL = 0x0 . . . 0x1F)

POSITION OFFSET VALUES AND PRESET FUNCTION

The preset function corrects the output position value of the serial I/O interface to the setpoint given by PRES_ST and PRES_MT. Correction is initiated by writing command **SOFT_PRES** or **SOFT_PRES_E2P** to the command register (see p. 93), or, if one of these commands is configured with PRES_CONF as PRES command at the input pin PRES, by a rising edge at PRES. See Table 172 for PRES_CONF.

When the preset function is started, the current position is determined. A correction factor for the output (OFFS_ST, OFFS_MT) is calculated taking PRES_ST and PRES_MT into account and stored in the internal RAM. If the command **SOFT_PRES_E2P** is used the correction factor is written to the external EEPROM.

The preset function can be restricted to the multiturn part using parameters PRES_MODE and FPRES_MT. If 1 or 2 bits of the multiturn part form part of the singleturn information, parameter CDL_MT can be used to exclude those bits from the multiturn preset (see p. 95).

Note:
Command SOFT_PRES, SOFT_PRES_E2P and execution of these functions via input pin PRES blocks iC-MNF's internal RAM for accesses over a certain time. During this time register operation via the BiSS interface the address will be dismissed and bit CMD_EXE of the status register is set.

ATTENTION!
While the preset sequence is in progress it must be ensured that the supply voltage to the two devices iC-MNF and the EEPROM is maintained. Otherwise the OFFS_ST and OFFS_PRES values will be set to zero and the error bit (EPR_ERR) will be set in the status register on the next system startup because of a faulty CRC_OFFS!

For the sensor data output the OFFS_ST and OFFS_MT values are subtracted from the internal synchronized result with each conversion.

The singleturn offset and preset values in the OFFS_ST and PRES_ST registers are always left aligned with the MSB starting at eeprom address 0x4C, bit 7 and 0x54, bit 7 respectively.

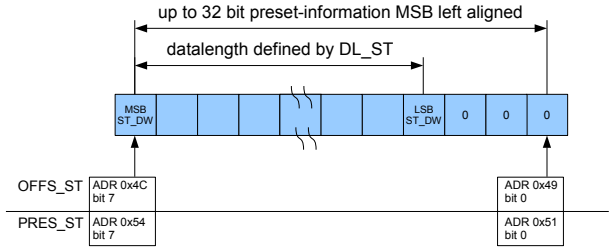


Figure 47: OFFS_ST/PRES_ST data representation

OFFS_ST(7:0)	Addr. 0x49; bit 7:0	
OFFS_ST(15:8)	Addr. 0x4A; bit 7:0	
OFFS_ST(23:16)	Addr. 0x4B; bit 7:0	
OFFS_ST(31:24)	Addr. 0x4C; bit 7:0	
OFFS_ST(7:0)	Addr. SER:0x09; bit 7:0	Bank 1
OFFS_ST(15:8)	Addr. SER:0x0A; bit 7:0	Bank 1
OFFS_ST(23:16)	Addr. SER:0x0B; bit 7:0	Bank 1
OFFS_ST(31:24)	Addr. SER:0x0C; bit 7:0	Bank 1

Code	Function
0x00000 ... 0x7FFFF	Singleturn output offset

Table 97: Position offset for ST data output

PRES_ST(7:0)	Addr. 0x51; bit 7:0	
PRES_ST(15:8)	Addr. 0x52; bit 7:0	
PRES_ST(23:16)	Addr. 0x53; bit 7:0	
PRES_ST(31:24)	Addr. 0x54; bit 7:0	
PRES_ST(7:0)	Addr. SER:0x11; bit 7:0	Bank 1
PRES_ST(15:8)	Addr. SER:0x12; bit 7:0	Bank 1
PRES_ST(23:16)	Addr. SER:0x13; bit 7:0	Bank 1
PRES_ST(31:24)	Addr. SER:0x14; bit 7:0	Bank 1

Code	Function
0x00000 ... 0x7FFFF	Preset register singleturn

Table 98: Preset value for ST data output

The multiturn offset and preset values in the OFFS_MT and PRES_MT registers are always right aligned with the LSB starting at eeprom address 0x4D, bit 0 and 0x55, bit 0 respectively.

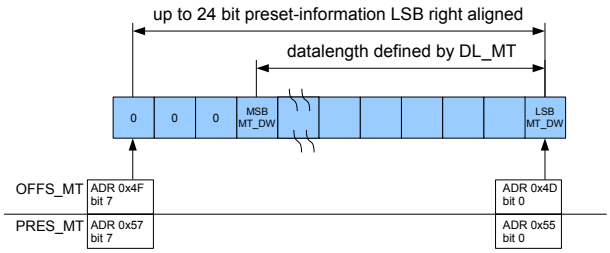


Figure 48: OFFS_MT/PRES_MT data representation

OFFS_MT(7:0)	Addr. 0x4D; bit 7:0	
OFFS_MT(15:8)	Addr. 0x4E; bit 7:0	
OFFS_MT(23:16)	Addr. 0x4F; bit 7:0	
OFFS_MT(7:0)	Addr. SER:0x0D; bit 7:0	Bank 1
OFFS_MT(15:8)	Addr. SER:0x0E; bit 7:0	Bank 1
OFFS_MT(23:16)	Addr. SER:0x0F; bit 7:0	Bank 1

Code	Function
0x000 ... 0xFFF	Multiturn output offset

Table 99: Position offset for MT data output

PRES_MT(7:0)	Addr. 0x55; bit 7:0	
PRES_MT(15:8)	Addr. 0x56; bit 7:0	
PRES_MT(23:16)	Addr. 0x57; bit 7:0	
PRES_MT(7:0)	Addr. SER:0x15; bit 7:0	Bank 1
PRES_MT(15:8)	Addr. SER:0x16; bit 7:0	Bank 1
PRES_MT(23:16)	Addr. SER:0x17; bit 7:0	Bank 1

Code	Function
0x000 ... 0xFFF	Preset register multiturn

Table 100: Preset value for MT data output

Note:
If iC-MNF is used as a simultaneous sampling, 3-channel S/D converter without synchronization, i.e.
- SYNC_S = 0x0
- SYNC_N = 0x0
- MODE_ST = 0x18, 0x1A, 0x1C or 0x1E

OFFS_ST(15:0) can be used to set the offset for the master track, parameter OFFS_ST(31:16) must be set to 0x00 and the preset function can not be used. For further explanation on how to change the offsets of the various tracks see TRACK OFFSET CALIBRATION, p. 72.

S/D CONVERSION: DATA LENGTH AND DATA LENGTH DEPENDENCIES

iC-MNF features a 14 bit sine-to-digital A/D converter. The conversion speed is configurable with CNVSPD.

CNVSPD	Addr. 0x32; bit 3:2
Code	Conversion Time *)
0x1	Fast (default)
0x2	Regular
0x0, 0x3	Reserved
Note	*) see Elec. Char. 605

Table 101: Conversion Speed

iC-MNF offers two different synchronization modes (Nonius and Multiturn) and a simultaneous sampling, up to 3-ch. sine-to-digital conversion without synchronization. Using **Nonius Modes** 2 or 3 tracks are combined by a vernier calculation with synchronization; Using **Multiturn Modes** up to 3 tracks are combined to form an absolute word via gear box code synchronization. For the configuration of the synchronization modes and the type of data to be output see Table 110 and Table 111.

Note:
By setting SYNC_S and SYNC_N to 0x0 in calculated **multiturn modes** it is also possible to output the converted tracks without synchronization.

The used bit lengths (parameters UBL_x) and the synchronization flags (parameters SYNC_x) are selectable for both operating modes.

Internal Bit Lengths

The used bit length is set for the master, segment and nonius tracks using parameters UBL_M, UBL_S and UBL_N. With SYNC_S and SYNC_N one can choose whether the segment or nonius track shall be synchronized using 4 additional synchronization bits.

UBL_M	Addr. 0x38; bit 3:0
UBL_S	Addr. 0x38; bit 7:4
UBL_N	Addr. 0x39; bit 3:0
Code	Used bit length
0x0	0
0x1	2
0x2	3
...	...
0xD	14
0xE, 0xF	Reserved

Table 102: Used bit length for master, segment and nonius

SYNC_S	Addr. 0x39; bit 4
SYNC_N	Addr. 0x39; bit 5
Code	Enable Synchronization
0x0	no synchronization of track
0x1	synchronization of track using 4 synchronization bits

Table 103: Synchronization segment and nonius

Nonius Mode: Principle PPR And Bit Length Dependencies

With a nonius system with three tracks UBL_M must be set so that it is at least as large as the maximum value of MAX(UBL_S+4, UBL_N+4). If only two tracks are used, UBL_S and SYNC_S must be set to zero. UBL_M must then at least match UBL_N+4.

The necessary number of signal periods per revolution (PPR) for the individual tracks is then determined by the selected used bit lengths:

Nonius required signal periods	
Track	Required signal periods
Master	$2^{UBL\_S+UBL\_N}$
Segment	$2^{UBL\_S+UBL\_N} - 2^{UBL\_N}$
Nonius	$2^{UBL\_S+UBL\_N} - 1$

The following tables show the possible settings and required number of signal periods. The total physical angle resolution in nonius mode is obtained from the sum of UBL_M+UBL_S+UBL_N. The limit up to which a nonius calculation is possible is given in Table 106 as the maximum tolerable phase deviation which may occur between the segment and master track or nonius and master track (with reference to the electrical 360° period of the master signal).

Bits/Track		Signal periods/Turn			Physical resolution [a]
UBL_S	UBL_N	Master	Seg.	Nonius	max
2	2	16	12	15	2+2+14
3	2	32	28	31	2+3+14
3	3	64	56	63	3+3+14
4	3	128	120	127	3+4+14
4	4	256	240	255	4+4+14
5	4	512	496	511	4+5+14
5	5	1024	992	1023	5+5+14
6 [b])	5	2048	2016	2047	5+6+14
6 [b])	6	4096	4032	4095	6+6+14

[a]) For configuration of the output data length, see Table 57
[b]) Not recommended due to the small phase deviation of ± 2.46°

Table 104: Settings for 3-track nonius mode

Bits/Track UBL_N	Signal periods/Turn Master	Nonius	Physical resolution [a]) max
2	4	3	2+14
3	8	7	3+14
4	16	15	4+14
5	32	31	5+14
6 [b])	64	63	6+14

[a]) For configuration of the output data length, see Table 57
[b]) Not recommended due to the small phase deviation of ± 2.46°

Table 105: Settings for 2-track nonius mode

UBL_N/ UBL_S	Permissible Max. Phase Deviation [given in degree per signal period of 360°]
2	± 39.38°
3	± 19.69°
4	± 9.84°
5	± 4.92°
6	± 2.46°

Table 106: Tolerable phase deviation for the master versus the nonius or segment track (with reference to 360°, electrical)

Note:
Nonius modes with a UBL_N/UBL_S = 6 are not feasible for standard encoder applications due to the small permissible max. phase deviation of ± 2.46°.

Multiturn Mode With Synchronization: Principle PPR And Bit Length Dependencies

In multiturn modes the selected used bit lengths (UBL_x) determine the reduction ratio required for the multiturn gear box.

Multiturn gear reduction factor	
Synchronization of track	Gear reduction
Master ↔ Singleturn	$2^{UBL\_M - SYNC\_BITS}$ [a])
Segment ↔ Master	2^{UBL_S}
Nonius ↔ Segment	2^{UBL_N}

Note: [a]) for the Master track the SYNC_BITS to the underlying Singleturn have to be taken into account, e.g., gear reduction Master track ↔ Singleturn 16 (≡ 4 Bit); SYNC_BITS to Singleturn 4 → set UBL_M at least to 8 Bit

For the synchronization between the tracks Master, Segment and Nonius, enabled with SYNC_S and SYNC_N always 4 bits are used.

The following tables show the possible settings and required number of signal periods. The total physical angle resolution in multiturn mode is obtained from the sum of UBL_M+UBL_S+UBL_N.

Bits/Track UBL_S	UBL_N	Signal periods/Turn Master	Seg.	Nonius	Physical resolution max
2	2	16	4	1	2+2+14
3	2	32	4	1	3+2+14
3	3	64	8	1	3+3+14
4	3	128	8	1	4+3+14
4	4	256	16	1	4+4+14
5	4	512	16	1	5+4+14
5	5	1024	32	1	5+5+14
6	5	2048	32	1	6+5+14
6	6	4096	64	1	6+6+14

[a]) For configuration of the output data length, see Table 57

Table 107: Settings for 3-track multiturn mode

Bits/Track UBL_N	Signal periods/Turn Master	Nonius	Physical resolution [a]) max
4	16	1	4+14
5	32	1	5+14
6	64	1	6+14

[a]) For configuration of the output data length, see Table 57

Table 108: Settings for 2-track multiturn mode

UBL_N/ UBL_S	Permissible Max. Phase Deviation [given in degree per signal period of 360°]
2 3 4 5 6	± 157.5°

Table 109: Tolerable phase deviation for all tracks to the underlying track: nonius → segment, segment → master (with reference to 360°, electrical of the underlying track)

Direct Output: 3-Ch. Sine-to-Digital Conversion (Multiturn Mode Without Synchronization)

iC-MNF functions as a simultaneous sampling, 3-channel sine-to-digital converter when the multiturn modes are selected with deactivated synchronization, i.e., SYNC_S = 0x0 and SYNC_N = 0x0.

The data length of each channel is controlled by the parameter UBL_M, UBL_S and UBL_N. A channel can be deactivated by setting UBL_x = 0x0. If only 1 track is used a MODE_ST with counted data can be selected, see Table 111. With counted data it is possible to synchronize an external multiturn value to this channel. If more than 1 channel is used a MODE_ST with calculated data must be selected.

S/D CONVERSION: SYNCHRONIZATION MODE AND TYPE OF OUTPUT DATA[1]

iC-MNF offers two synchronization modes following a S/D conversion of the selected tracks called nonius and multiturn mode. By using the nonius mode a nonius synchronization takes place after the S/D conversion. By using the multiturn mode a gear box synchronization takes place after S/D conversion.

Synchronization: Nonius And Multiturn Modes
Table 110 summarizes the possible settings for the nonius synchronization, Table 111 those for the gear box synchronization. Furthermore, iC-MNF works as a simultaneous sampling, 3-channel sine-to-digital converter when the multiturn modes are selected with deactivated synchronization.

MODE_ST: Sync. Mode Nonius Addr. 0x3A; bit 4:0			
Code	Output Mode	Data Generation	Output Data Verification
0x00	After Master	Counted	None
0x02	After Master	Counted	Frequency
0x04	After Master	Counted	Always
0x06	After All Tracks	Counted	Frequency
0x08	After All Tracks	Counted	Always
0x0A	Previously Converted	Counted	None
0x0C	Previously Converted	Counted	Frequency
0x0E	Previously Converted	Counted	Always
0x10	Cyclically Converted	Counted	None
0x12	Cyclically Converted	Counted	Frequency
0x14	Cyclically Converted	Counted	Always
0x16	T3 Triggered	Counted	Always
0x19 *)	After All Tracks	Calculated	None
0x1B *)	Previously Converted	Calculated	None
0x1D *)	Cyclically Converted	Calculated	None
0x1F *)	T3 Triggered	Calculated	None
Notes	If parameter MODE_ST is changed during operation command SOFT_RES should be executed. *) No external multiturn possible (i.e. MODE_MT has to be set to 0x0)		

Table 110: Selection of output data data for Sync. Mode Nonius

[1] For iC-MNF X1: Please refer to the design review on p. 106.

MODE_ST: Sync. Mode Multiturn Addr. 0x3A; bit 4:0			
Code	Output Mode	Data Generation	Output Data Verification
0x01	After Master	Counted	None
0x03	After Master	Counted	Frequency
0x05	After Master	Counted	Always
0x07	After All Tracks	Counted	Frequency
0x09	After All Tracks	Counted	Always
0x0B	Previously Converted	Counted	None
0x0D	Previously Converted	Counted	Frequency
0x0F	Previously Converted	Counted	Always
0x11	Cyclically Converted	Counted	None
0x13	Cyclically Converted	Counted	Frequency
0x15	Cyclically Converted	Counted	Always
0x17	T3 Triggered	Counted	Always
0x18 *)	After All Tracks	Calculated	None
0x1A *)	Previously Converted	Calculated	None
0x1C *)	Cyclically Converted	Calculated	None
0x1E *)	T3 Triggered	Calculated	None
Notes	If parameter MODE_ST is changed during operation command SOFT_RES should be executed. *) No external multiturn possible (i.e. MODE_MT has to be set to 0x0)		

Table 111: Selection of output data for Sync. Mode Multiturn

With a data request via the I/O interface the various conversion modes determine:

- The sample time of the analog signals and thus the ”age” of the output data
- The necessary processing time prior to generation of the output data word.

Op. Mode Descriptions Of Nonius And Multiturn Modes

MODE_ST Codes 0x00-0x05
With this mode the processing time is largely determined by the conversion time of the master track. The conversion procedure is as follows:

1. A data readout request triggers the conversion of all selected tracks
2. Following conversion of the master track: synchronization with the internal flash counter and output of the synchronized position value
3. During data readout: conversion of the remaining tracks and synchronization
4. Generation of ST_CTR with the next data readout cycle

MODE_ST Codes 0x06-0x09
The processing time is largely determined by the sum of the conversion time of the tracks for conversion. The conversion procedure is as follows:

1. A data readout triggers the complete conversion of the set tracks
2. Following conversion of the master track: synchronization with the internal flash counter
3. Following conversion of the remaining tracks: synchronization and generation of ST_CTR
4. Transmission of the synchronized position value. The transmitted ST_CTR counts as part of the current conversion.

MODE_ST Codes 0x0A-0xF
The processing time is low as previously triggered data is transmitted, however the sampling time is known.

Note:
The data from the first readout is invalid following a SOFT_RES/HARD_RES or power-on release.

The conversion procedure is as follows:

1. With a data readout: immediate transmission of the data from the last readout cycle including the relevant ST_CTR
2. With a data readout: start of a new conversion and providing of data for the next data readout cycle. ST_CTR is output directly at the NERR pin.

MODE_ST Codes 0x10-0x15
The processing time is low and the time of sampling not precisely known. The conversion procedure is as follows:

1. Regardless of the data readout: permanent background conversion (with optional linear interpolation between the sampling points enabled with parameter EUS)
2. With a data readout: transmission of current data. Each ST_CTR is output directly at the NERR pin. In data transmission a ST_CTR error is only signaled when the error occurs during the relevant nonius calculation or gear box synchronization.

EUS	Addr. 0x33; bit 3
Code	Function
0x0	Disabled
0x1	enable linear interpolation between the sampling points *)
Note	*) only affects MODE_ST = 0x10-0x15, update rate is 1/fosc (see Elec. Char. no. A01)

Table 112: Enable linear interpolation with MODE_ST = counted, cyclic

Application Hint:
The linear interpolation between sampling points (EUS = 0x1) reduces sampling jitter which is caused by the cyclic conversion. The EUS function adds a constant latency of typ. 12µs to the position data.

MODE_ST Code 0x16-0x17
This mode can be used in systems in which sampling must be synchronized to a frequency determined externally and independent of the data readout cycles. The sampling will be started with a rising edge at pin T3. The conversion procedure is as follows:

1. A conversion with nonius or gear box synchronization is triggered via a rising edge at pin T3. ST_CTR is output directly at the NERR pin.
2. With a data readout the most recent conversion data triggered by pin T3 is transmitted including the relevant ST_CTR.

Note:
After system startup, the error bit in the serial protocol is set for sensor data communications until the first conversion data triggered by pin T3 is available.

MODE_ST Code 0x18-0x19
The processing time is largely determined by the sum of the conversion time of the configured tracks. Procedure of conversion:

1. A data readout request triggers the complete conversion of the set tracks
2. Nonius or gear box synchronization
3. Transmission of the output data

MODE_ST Code 0x1A-0x1B
The processing time is low as previously triggered data is transmitted, however the sampling time is known. The conversion procedure is as follows:

1. With a data readout: immediate transmission of the data from the last readout cycle
2. With a data readout: start of a new conversion and providing of data for the next readout cycle.

Note:
The data from the first readout is invalid following a SOFT_RES/HARD_RES or power-on release.

MODE_ST Code 0x1C-0x1D
The processing time is low and the time of sampling not precisely known. The conversion procedure is as follows:

1. Regardless of the data readout: permanent background conversion
2. With a data readout: transmission of current data.

MODE_ST Code 0x1E-0x1F
This mode can be used in systems which require that asynchronous sampling is independent of the data readout timing. The sampling will be started with a rising edge at pin T3. The conversion procedure is as follows:

1. A conversion is triggered via a rising edge at pin T3, if applicable with nonius or gear box synchronization.
2. With a data readout the most recent output data triggered by pin T3 is transmitted.

Note:
After system startup, the error bit in the serial protocol is set for sensor data communications until the first conversion data triggered by pin T3 is available.

Counted vs. Calculated Data [1]

For the nonius and multiturn modes iC-MNF has a flash counter which counts the zero crossings of the master track. When the system is started this flash counter is preloaded with the absolute period information which has been most recently calculated using the nonius and segment tracks (or only the nonius track).

The type of data which is output via the serial I/O interface can be configured to be the most recently calculated or the counted data of the flash counter synchronized to the master track. If MODE_ST with data output of counted data and data verification is selected the counted data is checked against the recently calculated data and in case of an error status bit ST_CTR is set. Furthermore, it is possible to output synchronized singleturn and external multiturn position data which can be set using the parameter MODE_MT (see p. 73).

Note:
It is possible to use only the master track with a synchronized external multiturn by selecting a counted MT mode and setting UBL_M /= 0x0; UBL_S, UBL_N = 0x0 and SYNC_N, SYNC_S = 0x0.

The synchronization principle for the nonius mode with output of counted data with result verification is summarized in Figure 49, where φ represents the digitized angle of the relevant track. It is also possible to output counted data in multiturn mode.

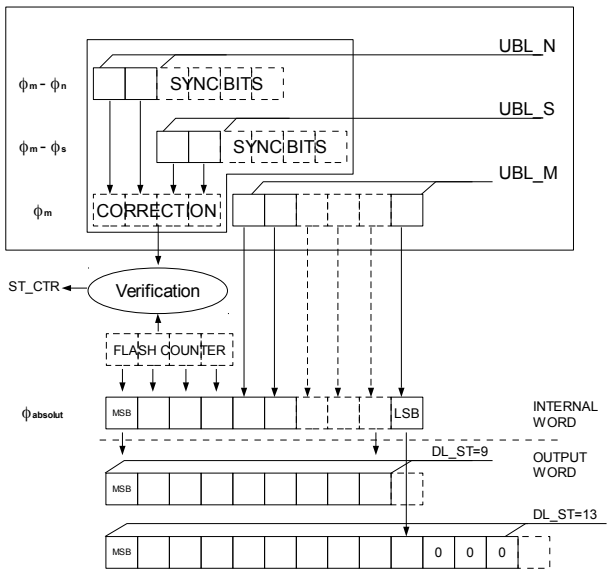


Figure 49: Nonius mode: Output of counted data

Figure 50 shows the synchronization principle for the multiturn mode and the output of calculated data, where φ represents the digitized angle of the relevant track.

[1] For iC-MNF X1: Please refer to the design review on p. 106.

By using calculated data no output verification is possible. It is also possible to output calculated data in nonius mode.

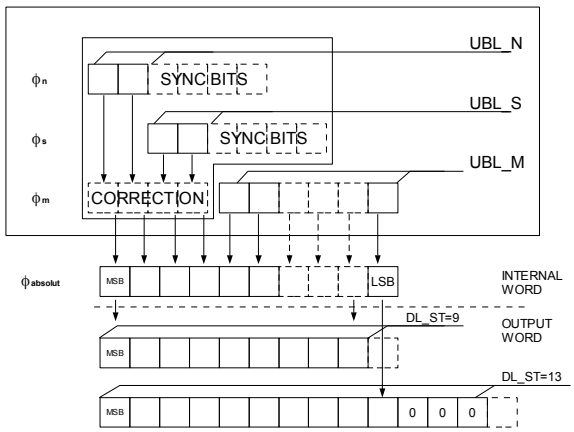


Figure 50: Multiturn mode: Output of calculated data

iC-MNF can also function as a simultaneous sampling, up to 3-channel sine-to-digital converter when the calculated multiturn modes are selected with deactivated synchronization. When SYNC_S = 0x0 and SYNC_N = 0x0 no track synchronization takes place; the data from all three tracks is queued up for output without any further processing (see Fig. 51).

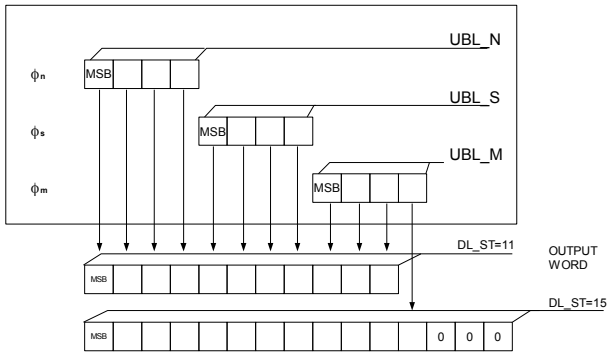


Figure 51: Principle of simultaneous sampling, 3-channel S/D conversion with direct data output

Output Data Verification

It is possible to verify the counted period when a nonius or gear box synchronization has been completed. Possible settings include:

1. No verification of counted periods
2. Frequency-dependent verification of counted periods. Exceeding the maximum master track signal frequency set by FRQ_TH (see Table 113) disables the verification of the internal flash counter

against the result of the nonius or gear box synchronization. If the limit is again undershot, future conversions are again verified.

3. Verification of the internal flash counter against the result of the nonius or gear box synchronization is always enabled and executed with each conversion.

Digital Frequency Monitoring
iC-MNF features an integrated frequency monitoring circuit for the master track. A signal frequency warning threshold can be configured with FRQ_TH.

FRQ_TH	Addr. 0x39; bit 7:6	
Code	Warning Threshold	
0x0	9.7 kHz	A01/2061 *)
0x1	37.8 kHz	A01/529
0x2	73.5 kHz	A01/272
0x3	138.8 kHz	A01/144
Note	*) depends on Electrical Characteristic of the Clock Oscillator: A01 see p. 11	

Table 113: Signal monitoring frequency

FRQ_TH is used by the frequency-dependent period verification feature available for nonius modes (see MODE_ST = 0x02, 0x06, 0x0C and 0x12) and multiturn modes (see MODE_ST = 0x03, 0x07, 0x0D and 0x13) as well as for the external multiturn verification (see CHK_MT = 0x2, p. 75) and disables the verification of the flash counter against the nonius, gear box synchronization or the external multiturn if the maximum master track signal frequency set by FRQ_TH is exceeded.

It also triggers the status bits FQ_WDR (excessive signal frequency on current readout request) see Table 144.

Note:
MODE_ST with output of counted data: if the frequency of the master track is too high at power on, FQ_WDR remain set until the output data verification was successful below the frequency warning threshold.

TRACK OFFSET CALIBRATION

Segment And Nonius Track

According to the track resolution the offset values of the nonius and segment tracks must be set left aligned in the SPO_N and SPO_S registers (see Fig. 52) and are added to the conversion result of the corresponding track. The parameters affecting the track resolution are UBL_x/SYNC_x, see p. 65.

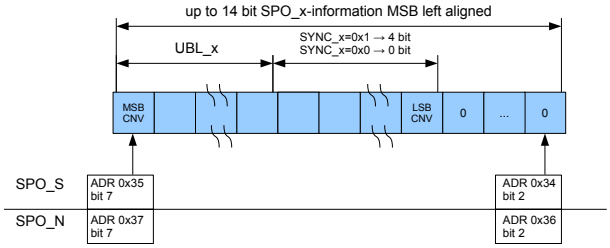


Figure 52: SPO_x (x=S,N)

SPO_N(5:0)	Addr. 0x36; bit 7:2
SPO_N(13:6)	Addr. 0x37; bit 7:0
SPO_S(5:0)	Addr. 0x34; bit 7:2
SPO_S(13:6)	Addr. 0x35; bit 7:0
Code	Track Offset
0x2000	-8192
...	...
0x3FFF	-1
0x0000	0
...	...
0x1FFF	8191

Table 114: Track offsets for nonius and segment

Notes:
If a synchronization of the tracks is configured (SYNC_S/N /= 0x0), please note that SPO_S/N are added prior to synchronization to the corresponding tracks.
Depending on the synchronization mode (see chapter **S/D CONVERSION: DATA LENGTH AND DATA LENGTH DEPENDENCIES**, p. 65 ff.) the purpose of using the track offsets is as follows:

Nonius synchronization: It is important that the tracks that are used to form the absolute position value have a shared zero crossing once within the $2^{UBL\_S+UBL\_N}$ master track periods. The track offsets are used to shift the segment and nonius track relative to the master track.

Multiturn synchronization: The track offsets are used to shift the nonius and segment tracks to the underlying track to make the best possible use of the available tolerance range.

Master Track

Normally OFFS_ST is used as position offset value for the synchronized output position (see p. 63). However if iC-MNF is used as an up to 3-channel sine-to-digital converter without synchronization (see Table 115) it is possible to set the offset for the master track with the lower bits of OFFS_ST (s. Tab 116). The offset value has to be entered left aligned.

Parameter	Description
MODE_ST = 0x18, 0x1A, 0x1C or 0x1E	Multiturn Mode, output of calculated data
SYNC_S/N = 0x0	no synchronization

Table 115: Required settings to use OFFS_ST(15:2) as master track offset

SPO_M(5:0)	Addr. 0x49; bit 7:2	
SPO_M(13:6)	Addr. 0x4A; bit 7:0	
SPO_M(5:0)	Addr. SER: 0x09; bit 7:2	Bank 1
SPO_M(13:6)	Addr. SER: 0x0A; bit 7:0	Bank 1
Code	Track Offset Master*)	
0x2000	-8192	
...	...	
0x3FFF	-1	
0x0000	0	
...	...	
0x1FFF	8191	
Notes	*) only with MODE_ST = 0x18, 0x1A, 0x1C, 0x1E; SYNC_x = 0x0 OFFS_ST(31:16) must be set to 0x00 OFFS_ST(15:2) and SPO_M(13:0) are addressing the same bits	

Table 116: Track offsets for master track in multiturn-mode without synchronization

Automatic Track Offset Calibration

iC-MNF provides an automatic track offset calibration feature that can be started using command CAL_TO and a track offset monitoring feature. See chapter **AUTOMATIC CALIBRATION FEATURE** p. 99 ff. for further information. The automatic calibration can be used in embedded applications.

MULTITURN INTERFACE

General Settings

MODE_ST	
Code	Internal and external MT possible
0x00 - 0x18	✓
0x19 - 0x1F	-

Table 117: Possible MODE_ST settings for internal and external MT

iC-MNF has an internal multiturn (MT) counter to count the multiturn information based on the ST cycles. In counted nonius or multiturn modes (MODE_ST, see Tab. 117 and p. 67 ff.c) iC-MNF can connect to an external multiturn sensor using the serial multiturn interface by using the BiSS, SSI protocol or the parallel two-pin interface. The parallel two-pin interface can read a single bit multiturn position accompanied by a synchronization bit and can double the coverage of the absolute singleturn position if additional sensors provide 180 and 90 degree sector information. If the external MT interface is used the MT counter is preloaded on system startup with the synchronized read-in external MT data.

If the MT interface is not used, the internal 24-bit MT counter can extend the singleturn information to include the internal MT counter. This is done by setting MODE_MT to 0x0, DL_EXT_MT to 0x0 and DL_MT others than 0x0 (Table 56).

MODE_MT Addr. 0x41; bit 7:4 **MODE_MT** Addr. SER:0x01; bit 7:4 Bank 1	
Code	Function
0x0	internal
0x1	BiSS C
0x2	SSI binary
0x3	SSI binary +ERR
0x4	SSI binary +ERR +WRN
0x5	SSI gray
0x6	SSI gray +ERR
0x7	SSI gray +ERR +WRN
0x8	Parallel MT interface active (2-bit mode): Pin MTMA is input for 180° and pin MTSLI input for 90° sector information
0x9	GET_MT
Note	If MODE_MT is changed during operation, command SOFT_RES must be executed (see p. 93).

Table 118: MT Interface operation mode

Note:
Setting ECDL_MT = 0x1 (CDL_MT active) and CDL_MT = 0x1 (no output of multiturn-information via serial I/O interface) deactivates the external multiturn interface, i.e. no further read-in of external multiturn data. For further information on the parameters ECDL_MT and CDL_MT see p. 60.

The polarity of the error and warning bits within the various multiturn protocols are summarized in Table 119.

MODE_MT				
Function	Error		Warning	
	low active	high active	low active	high active
BiSS	✓	-	✓	-
SSI	-	-	-	-
SSI(gray) +ERR	-	✓	-	-
SSI(gray) +ERR+WRN	-	✓	-	✓

Table 119: MODE_MT: error/warning-bit within multiturn protocols

When using the BiSS or SSI protocol SLOW_MT can be used to reduce the frequency at pin MTMA for the external multiturn encoder.

SLOW_MT Addr. 0x43; bit 6 **SLOW_MT** Addr. SER:0x03; bit 6 Bank 1		
Code	MTMA frequency BiSS	MTMA frequency SSI
0x0	1 MHz	125 kHz
0x1	125 kHz	31.25 kHz

Table 120: Reduction of MTMA clock frequency

The code direction of the read multiturn data can be inverted using parameter ROT_MT.

ROT_MT Addr. 0x43; bit 5 **ROT_MT** Addr. SER:0x03; bit 5 Bank 1	
Code	Function
0x0	no inversion of code direction
0x1	inversion of code direction

Table 121: Inverted code direction of external multiturn

The parameter SPO_MT allows to balance an existing static offset between the singleturn and the multiturn. SPO_MT is added before the synchronization of the read multiturn data (see Figure 53).

SPO_MT Addr. 0x42; bit 3:0 **SPO_MT** Addr. SER:0x02; bit 3:0 Bank 1	
Code	Phase Offset: ST ↔ MT referred to ST revolution
0x0	0°
0x1	22.5°
...	...
0x7	157.5°
0x8	-180°
0x9	-157.5°
...	...
0xF	-22.5°

Table 122: Offset of external multiturn

Application Hint:
Due to the mechanical tolerances during assembly, it is recommended to do a multiturn calibration e.g. by shifting the zero crossing point of the multiturn synchronization bits to the zero crossing point of the corresponding upper bits of the singleturn.
The raw position data of the external multiturn system (data length configured with DL_EXT_MT + SBL_MT) and the raw position data of the singleturn is needed for this kind of multiturn calibration. OFFS_ST and OFFS_MT must be set to 0 for this purpose.
For further information on how to access the raw data of the multiturn please refer to p. 82 when using a BiSS MT sensor or to p. 83 when using a SSI MT sensor.

Configuration Of Data Lengths

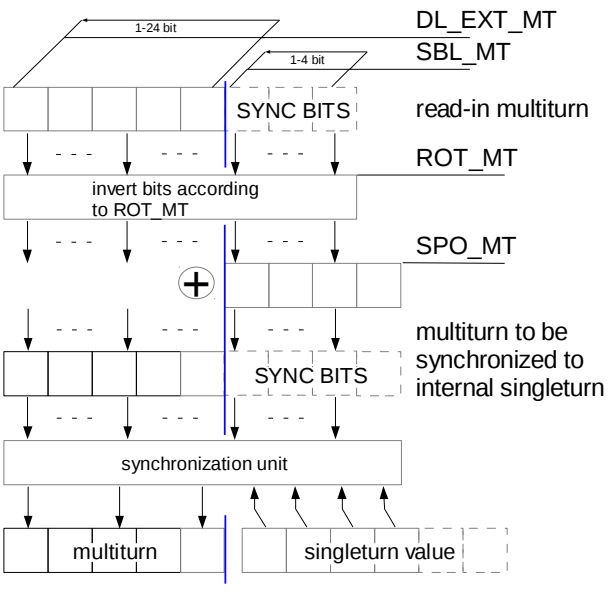


Figure 53: Parameters to configure external multiturn

The bit length of the external multiturn data word is set using parameter DL_MT_EXT. For synchronization purposes the synchronization bit length must be set with SBL_MT. Synchronization occurs between the external multiturn data read in and the period information counted internally. The synchronization can occur automatically within the relevant phase tolerances.

DL_EXT_MT Addr. 0x43; bit 4:0 **DL_EXT_MT** Addr. SER:0x03; bit 4:0 Bank 1	
Code	Multiturn bit count*
0x00	0
0x01	1
...	...
0x18	24
Note	*) Does not include synchronization bits of the external MT sensor.

Table 123: external MT data length (and counter depth)

SBL_MT Addr. 0x42; bit 7:6 **SBL_MT** Addr. SER:0x02; bit 7:6 Bank 1		
Code	MT synchronization bit length	Synchronization range (ST resolution)
0x0	1 bit	± 90°
0x1	2 bit	± 135°
0x2	3 bit	± 157.5°
0x3	4 bit	± 168.75°

Table 124: MT synchronization bit length

Figure 54 shows the principle of a 2 bit MT synchronization for ideal signals (without indication of synchronization tolerance limits).

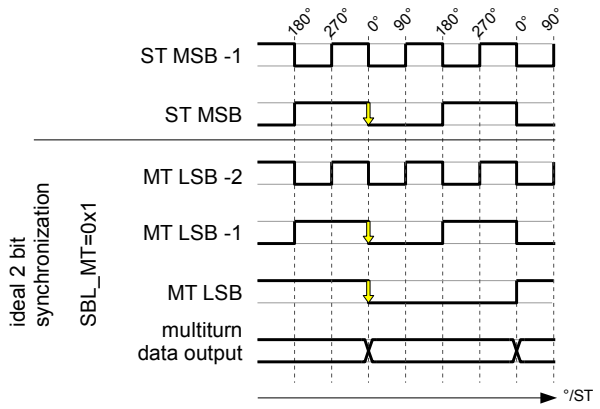


Figure 54: Principle of 2 bit MT synchronization

Figure 55 shows the principle of a 1 bit MT synchronization for ideal signals (without indication of synchronization tolerance limits) for leading and trailing signals.

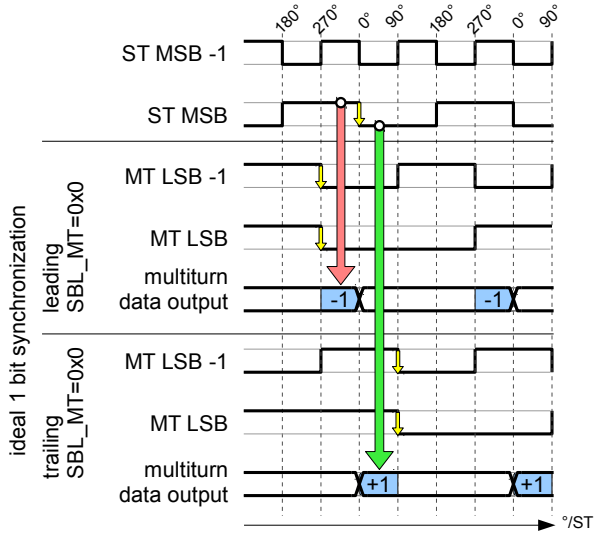


Figure 55: Principle of 1 bit MT synchronization

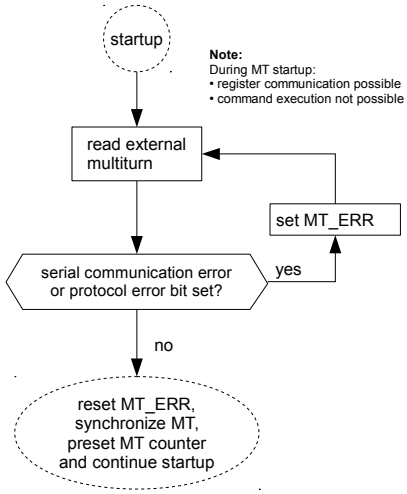


Figure 56: Startup external multiturn

Multiturn: BiSS/SSI Error Handling On Startup And Multiturn Check

If a communication error occurs when reading in external multiturn data using the SSI or BiSS protocol during the **startup procedure** (such as pin MTSLI reading a permanent logic 0 or the external MT sensor not responding), the request for the external multiturn data is repeated, the NERR pin is set to low and status bits MT_ERR as well as CMD_EXE remain set until read in is successful. Register communication with iC-MNF is possible whereas commands can not be executed.

Note:
The multiturn startup sequence shown in Figure 56 can be initiated with command SOFT_RES or by Power-Up. To exit the startup loop in case of an communication error during MT startup set MODE_MT = 0x0 (internal).

With CHK_MT the device can be configured so that the counted multiturn period is verified every 8 ms against the synchronized read-in MT data. An error in the multiturn check (the comparison of the counted multiturn period and the external multiturn position data) is reported via the error bit and MT_CTR is set in the status register (see p. 86 ff.).

CHK_MT	Addr. 0x42; bit 5:4	
CHK_MT	Addr. SER:0x02; bit 5:4	Bank 1
Code	Function	
0x0	Verification disabled	
0x1	Cyclic verification every 8 ms	
0x2	Frequency dependent[1] verification every 8 ms	
0x3	Reserved	
Note	[1]no verification if frequency of master track above warning threshold (see FRQ_TH, p. 71)	

Table 125: MT Period counter verification

If there is an error in the multiturn sensor communication (such as pin MTSLI reading a permanent logic 0 or 1 or the external MT sensor not responding) in **normal operating mode** status bit MT_ERR is set and the read in procedure is repeated after 8 ms.

The parameter WI2C_MT can be used in MT-System where the MT device is connected directly to the I2C Bus and can not handle I2C communication in parallel with sensor data communication. With WI2C_MT set to 0x1, iC-MNF waits until the I2C communication is finished before a new MT read in is started.

WI2C_MT Addr. 0x43; bit 7 **WI2C_MT** Addr. SER:0x03; bit 7	Bank 1
Code	Function *)
0x0	not affected by I2C communication: 8 ms
0x1	ongoing I2C communication may increase verification cycle time (see Fig. 57)
Note	*) for verification to take place CHK_MT has to be set to 0x1

Table 126: Verification cycle time with ongoing I2C communication (CHK_MT = 0x1)

The parameters affecting the external MT verification are summarized in Fig. 57.

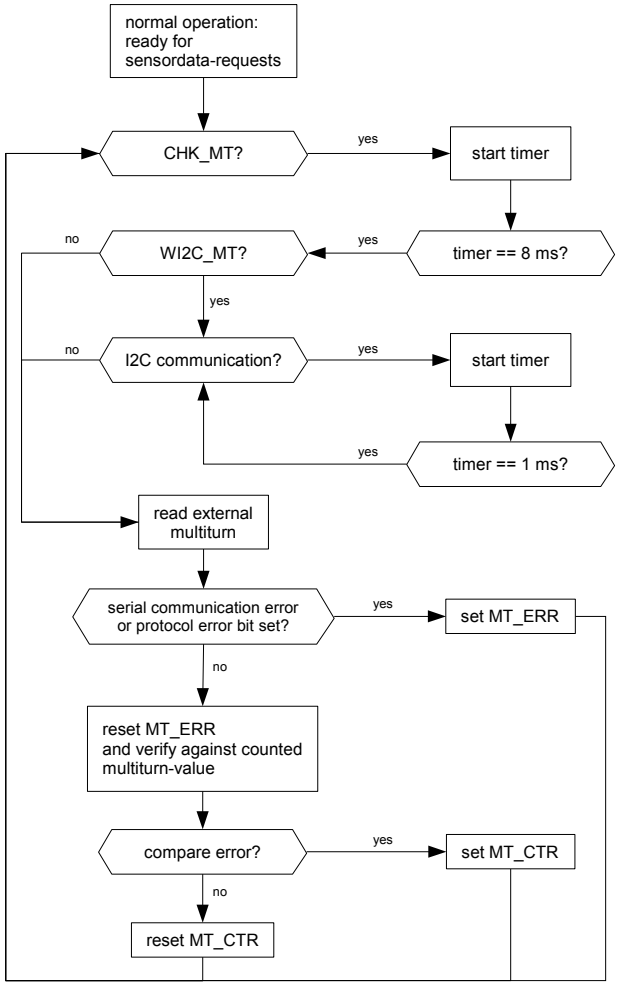


Figure 57: External multiturn control

Multiturn: BiSS Interface

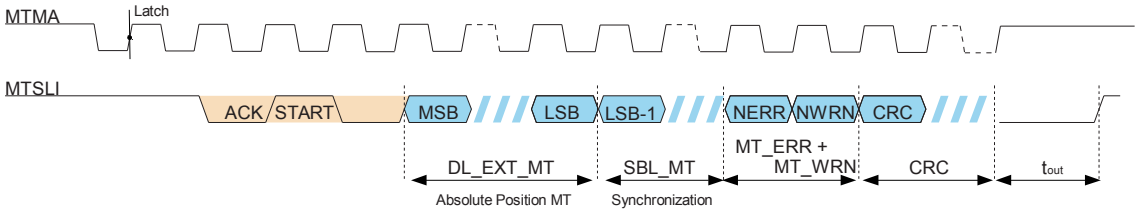


Figure 58: Example of the MT interface line signals with BiSS C protocol

MODE_MT	
Code	Function
0x1	BiSS C

Table 127: MT Interface operation mode

The multiturn interface can read in multiturn data using the BiSS C protocol. The BiSS C MT serial bit stream is binary coded, error and warning bits are low active. A fixed CRC polynomial is used for the CRC check, see Table 128. The read in frequency is configurable, see Table 120.

The multiturn data length of the external multiturn can be calculated with

$$datalength_{MT\_BISS} = bits(DL\_EXT\_MT) + bits(SBL\_MT) + error + warning + 6\ bit\ CRC.$$

data-channel*)	type of CRC	CRC HEX Code	Polynomial
SCD (sensor)	normal	0x43	x^6+x^1+1
Note	*) explanation s. BiSS-C specification		

Table 128: BiSS MT CRC polynomial

For a description of the multiturn interface error behavior refer to **Multiturn: BiSS/SSI Error Handling On Startup And Multiturn Check** p. 75. Note that, with MODE_MT set to BiSS C mode a set error bit (low) or a CRC error is also classified as a communication error.

Multiturn: SSI Interface

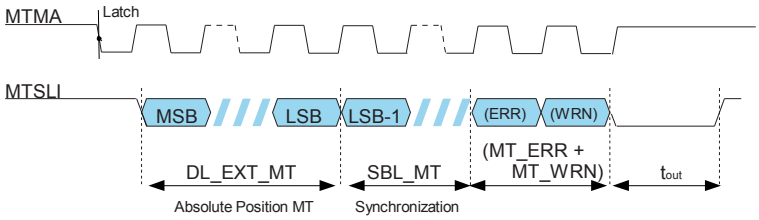


Figure 59: Example of the MT interface line signals with SSI protocol

MODE_MT	
Code	Function
0x2	SSI binary
0x3	SSI binary +ERR
0x4	SSI binary +ERR +WRN
0x5	SSI gray
0x6	SSI gray +ERR
0x7	SSI gray +ERR +WRN

Table 129: MT Interface operation mode

The multiturn interface can read in multiturn data using the SSI protocol. An optional error and warning bit (both high active) can be configured. The read in frequency is configurable, see Table 120. The format option Gray or binary code covers the MT data word in its entirety; the optional error bit and warning bit remains untouched. The multiturn data package containing sensor data and the optional error and warning bit must be terminated by a stop (0).

The multiturn data length of the external multiturn can be calculated with

$datalength_{MT\_SSI} = bits(DL\_EXT\_MT) + bits(SBL\_MT) + optional(error) + optional(warning)$.

For a description of the multiturn interface error behavior refer to **Multiturn: BiSS/SSI Error Handling On Startup And Multiturn Check** p. 75. Note that, with MODE_MT set to SSI+ERR(+WRN) a set error bit (high active) is classified as a communication error.

Multiturn: 2-Bit Mode Parallel[1]

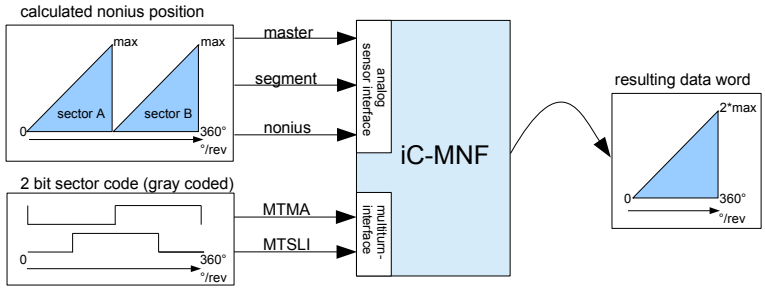


Figure 60: Principle of 2-bit mode

MODE_MT	
Code	Function
0x8	Parallel MT interface active (2-bit mode): Pin MTMA is input for 180° and pin MTSLI input for 90° sector information
Note	If MODE_MT is changed during operation, command SOFT_RES must be executed (see p. 93).

Table 130: MT Interface operation mode

By setting MODE_MT to 2-bit mode, MTMA and MTSLI are configured as inputs. These inputs now expect digital signals phase shifted by 90°. MTMA reads the single bit period information and MTSLI the shifted synchronization bit. Figure 60 illustrates the principle and Table 131 summarizes the necessary settings.

Parameter	Description
MODE_MT = 0x8	MT interface op. mode: 2-bit mode
DL_EXT_MT = 0x01	MT data length: 1 bit
SBL_MT = 0x0	Synchronization bit length: 1 bit

Table 131: Required settings for 2-bit mode

Note:
With MODE_MT set to 0x8, the relative position of the signals at pins MTSLI and MTMA to each other and to the ST position can be checked by cyclically reading the STATUS4 register (see p. 87, bits 5 and 6).

Figure 61 shows examples of leading and trailing MTSLI/MTMA signals with respect to iC-MNFs ST position. The green arrows are indicating the permissible relative position tolerances. The synchronization can occur automatically within the relevant phase tolerances. Parameter SPO_MT offers the possibility to adjust the synchronization range (see Tab. 122).

[1] For iC-MNF X1: Please refer to the design review on p. 106.

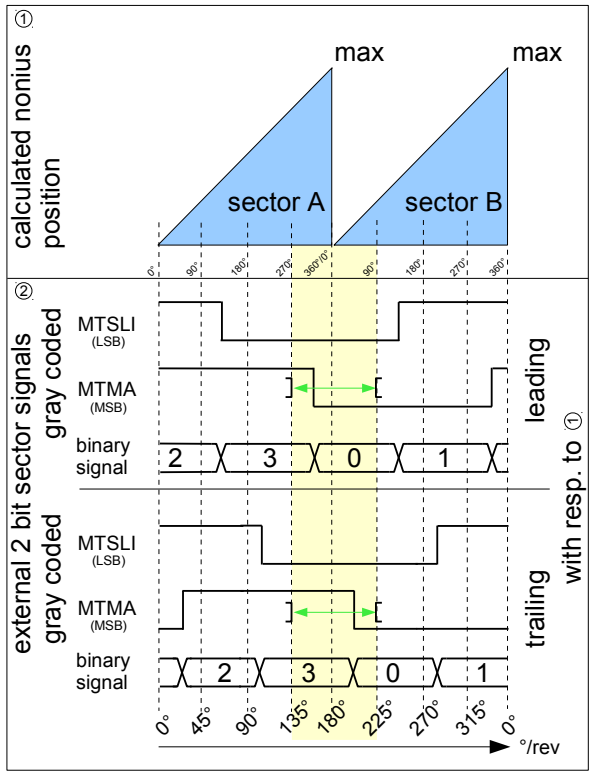


Figure 61: Multiturn 2-Bit Mode: Example of leading and trailing input signals

This mode can be used together with the optical encoder ICs of the iC-PNH series. iC-PNH provides 3 analog tracks (master, segment and nonius) as well as 2 digital tracks for the 2-bit sector code. The corresponding code discs are designed in a way that the 2-bit sector code is 45° leading to the singleturn value given by master, segment and nonius. If the mechanical adjustment of iC-PNH to the corresponding code disc is ideal, the 45° shift of the 2-bit sector code can be compensated by setting parameter SPO_MT (Table 122) to 0xC. In general it is recommend to use parameter SPO_MT to adjust the zero point of the 2-bit sector

code to the singleturn zero point. The actual offset can be derived by monitoring the singleturn position and MTSLI/MTMA in STATUS4.

Another typical application example for the 2-bit mode is a magnetic angle encoder scanning the pole wheel with MR sensors. A nonius coded wheel of 16, 15 and 12 pole pairs yields 32, 30 and 24 sine periods per turn on iC-MNF's analog inputs. The nonius calculation would not produce absolute angle position data over a single revolution since the maximum singleturn value is achieved twice. The distinction as to which half of the revolution the axis is in can only be made using section sensors, two Hall sensors for example, whose digital outputs are connected up directly to MTMA and MTSLI.

Multiturn: Direct Communication To Multiturn Sensor using the BiSS protocol

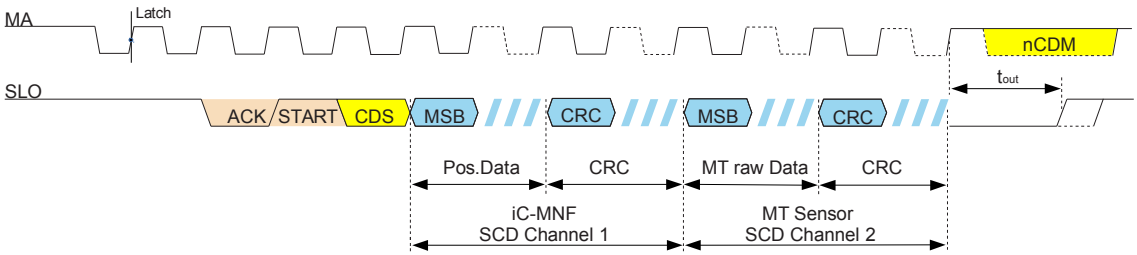


Figure 62: Example of the MT interface line signals with BiSS C protocol: direct communication to BiSS C multiturn sensor (MODE_MT = 0x9, MODE_SER = 0x0/0x1)

MODE_SER	
Code	Protocol
0x0	BiSS C
0x1	BiSS C Extended CRC

Table 132: Direct communication to BiSS multiturn sensor MODE_SER configuration

MODE_MT	
Code	Function
0x9	GET_MT

Table 133: MT Interface operation mode

iC-MNF can connect an external BiSS C multiturn sensor to the master controller when GET_MT is enabled. To this end pin MA receiving the BiSS master's clock signal is fed through to pin MTMA and the MTSLI pin is activated in place of the SLI pin. The output data length of the position data of iC-MNF (SCD Channel 1) remains unchanged.

Upon enabling this mode the single cycle timeout must have elapsed and an additional init command carried out by the BiSS master, before it can run the first register communication. This temporal BiSS chain operation eases device parameterization during encoder manufacturing.

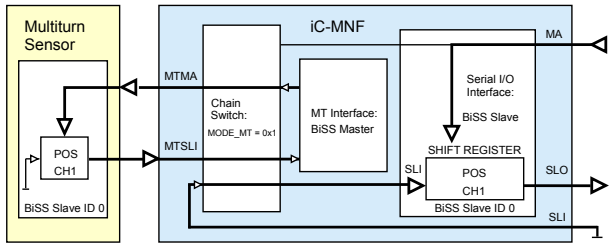


Figure 63: Normal operation (MODE_MT = 0x1)

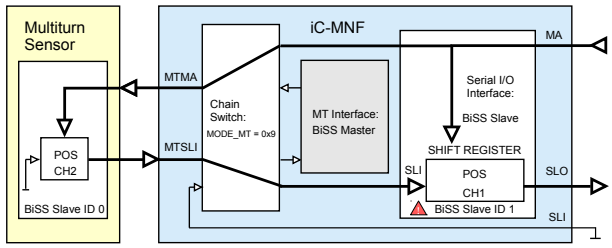


Figure 64: MT operated in BiSS chain (MODE_MT = 0x9, MODE_SER = 0x0/0x1)

Note:
With GET_MT enabled due to the temporary build BiSS chain, the external multiturn can be addressed with BiSS ID 0 and the iC-MNF (singleturn) with BiSS ID 1 (see Fig. 64).
This means, after setting GET_MT the BiSS ID of iC-MNF switches from ID 0 to ID 1!

Multiturn: Direct Communication To Multiturn Sensor using the SSI protocol

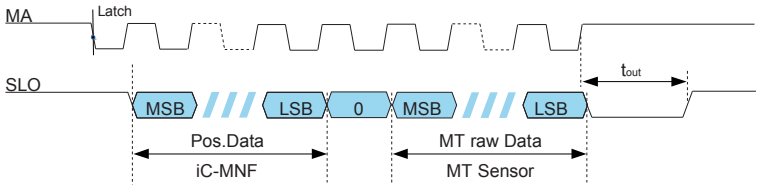


Figure 65: Example of the MT interface line signals with SSI protocol: direct communication to SSI multiturn sensor (MODE_MT = 0x9, MODE_SER = 0x2-0x7, 0xF)

MODE_SER	
Code	Protocol
0x2	SSI binary
0x3	SSI binary +ERRL
0x4	SSI binary +ERRH
0x5	SSI gray
0x6	SSI gray +ERRL
0x7	SSI gray +ERRH
0xF	ExtSSI

Table 134: Direct communication to SSI multiturn sensor MODE_SER configuration

MODE_MT	
Code	Function
0x9	GET_MT

Table 135: MT Interface operation mode

To read out the single-turn raw data of an external SSI multiturn sensor, iC-MNF can connect the external sensor to the master controller. To do this, the SSI protocol must be selected via MODE_SER and GET_MT must be activated. The pin MA, which receives the clock signal of the SSI master, is fed through to the pin MTMA. The MTSLI pin is connected to the internal SLI signal (see Fig. 67). The output data length of the position data of iC-MNF remains unchanged.

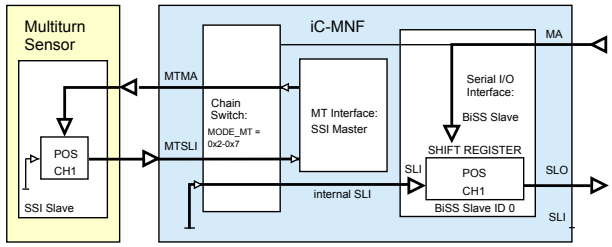


Figure 66: Normal operation (MODE_MT = 0x1)

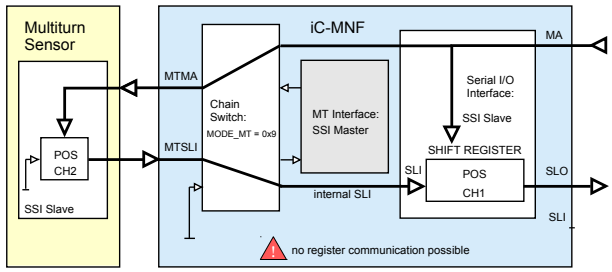


Figure 67: MT operated in SSI chain (MODE_MT = 0x9, MODE_SER = 0x2-0x7, 0xF)

Note:
Register communication is not possible if the SSI protocol is used. It is best practice to restart iC-MNF to return to normal operation mode.

TEMPERATURE SENSOR [1]

General Settings

iC-MNF includes an internal digital 8 bit temperature sensor. The digital temperature representation of TEMP is shown in Table 136.

TEMP	Addr. SER:0x6C; bit 7:0
Code	Temperature
0x00	-64 °C
0x01	-63 °C
...	...
0x18	-40 °C
...	...
0x40	0 °C
...	...
0x54	20 °C
...	...
0xA4	100 °C
...	...
0xFF	191 °C

Table 136: Temperature sensor value representation

Its offset can be calibrated with parameter OFF_TEM.

OFF_TEM	Addr. 0x45; bit 5:0	
OFF_TEM	Addr. SER:0x05; bit 5:0	Bank 1
Code	Temperature Correction	
0x00	0 °C	
0x01	1 °C	
...		
0x0F	15 °C	
0x10	-48 °C	
0x11	-47 °C	
...		
0x3F	-1 °C	

Table 137: Temperature sensor offset

Error Thresholds

Temperature error thresholds can be defined for high and low temperature errors. The high temperature error threshold can be defined using parameter ETH_TEM. If the measured temperature is above the warning threshold status bit TH_WRN is set. If the temperature is above the error threshold status bit TH_ERR is set.

ETH_TEM [1]	Addr. 0x46; bit 6:4	
ETH_TEM	Addr. SER:0x06; bit 6:4	Bank 1
Code	Warning Temperature	Error Temperature
0x0	70 °C	85 °C
0x1	80 °C	95 °C
0x2	90 °C	105 °C
0x3	100 °C	115 °C
0x4	110 °C	125 °C
0x5	115 °C	130 °C
0x6	120 °C	135 °C
0x7	125 °C	140 °C
Note	Default is 0x7: warning: 125 °C, error: 140 °C	

Table 138: Temperature high warning and error thresholds

The low temperature error threshold can be defined with ETL_TEM. If the measured temperature is below the error threshold status bit TL_ERR is set (for a description of status registers see p. 86).

ETL_TEM [1]	Addr. 0x46; bit 2:0	
ETL_TEM	Addr. SER:0x06; bit 2:0	Bank 1
Code	Error Temperature	
0x0	no temperature low error	
0x1	0 °C	
0x2	-5 °C	
0x3	-10 °C	
0x4	-20 °C	
0x5	-25 °C	
0x6	-30 °C	
0x7	-40 °C	

Table 139: Temperature low error thresholds

[1] For iC-MNF X1: Please refer to the design review on p. 106.

Additional BiSS Temperature Data Channel

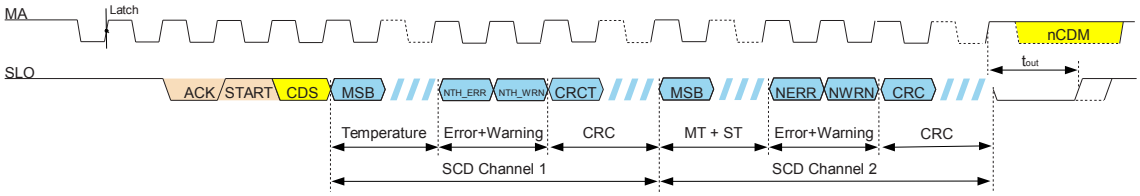


Figure 68: Example of line signals BiSS C protocol with temperature data channel enabled

ETS	Addr. 0x3C; bit 7
Code	Additional temperature channel
0x0 0x1	disabled enabled
Note	requires MODE_SER = 0x0/0x1

Table 140: Enable temperature data channel in BiSS Mode

If the serial I/O interface is set to BiSS (MODE_SER = 0x0,0x1) it is possible to readout the temperature data by activating an additional data channel using parameter ETS (SCD channel 1, see Fig. 68). The additional data channel is output before the sensor data channel of iC-MNF. The 8 bit temperature data is output in binary form. The error and warning bits TH_ERR/TL_ERR and TH_WRN are transmitted low active (description of status registers see p. 86). The CRC value is output inverted (CRCT).

data-channel*)	CRC HEX Code	Polynomial
SCD (temperature)	0x25	x^5+x^2+1
CDM, CDS (register)	0x13	x^4+x^1+1
Note	*) explanation s. BiSS-C specification	

Table 141: Temperature data channel BiSS CRC polynomial

A restricted register communication is possible. The temperature data channel can be addressed with BiSS ID 1 (see Fig. 69). The accessible registers are PRO_ID1, SER_NO, DEV_ID and MFG_ID. The returned values for SER_NO, DEV_ID and MFG_ID are the same as in the iC-MNF data-channel. The access to the other registers is denied when addressing the temperature data channel.

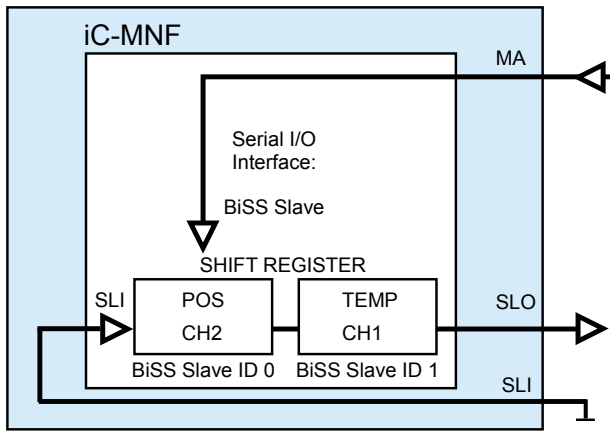


Figure 69: MNF with activated temperature data channel (ETS = 0x1)

Addr. SER	**Content**	**RPL**	
		RP0	**RP1**
0x00 .. 0x3F	Register bank	n.a.	n.a.
0x40	Bank selection	n.a.	n.a.
0x41	EDSBANK	n.a.	n.a.
0x42 .. 0x43	PRO_ID1	R / W	R
0x44 .. 0x47	SER_NO	R	R
0x48 .. 0x77	-	n.a.	n.a.
0x78 .. 0x7D	DEV_ID	R	R
0x7E .. 0x7F	MFG_ID	R	R

Table 142: Register access via serial I/O interface when addressing the temperature data channel (ETS = 0x1, for RPL see p. 61)

STATUS REGISTERS AND ERROR MONITORING

Status Register

Various Status-information can be obtained by reading out status bytes STATUS0 to STATUS4.

- STATUS0 to STATUS2 are used to collect error and status information such as amplitude, temperature, EEPROM communication error etc.
- STATUS3 and STATUS4 provide a quick overview of the pin configuration, pin status and of the register protection level.

If an error occurs the relevant bit will be set and maintained until the command CLEAR_STAT is executed (see Table 165) or if RR_STAT is activated until the relevant status register is read out.

RR_STAT Addr. 0x44; bit 7 **RR_STAT** Addr. SER:0x4; bit 7		Bank 1
Code	CLEAR_STAT resets STATUS0...STATUS4	STATUSx read out resets information of STATUSx (x = 0-4)
0x0	✓	-
0x1	✓	✓

Table 143: Readout resets status

STATUS0 Addr. SER:0x72; bit 7:0		R
Bit	Name	Description of status message
7	TH_WRN	Excessive temperature warning
6	EPR_ERR	I2C/Configuration Error: - I2C communication error - Invalid check sum
5	FQ_WDR	Excessive signal frequency on master track*: during current readout request
4	CIF_ERR	Automatic calibration: input signals too fast
3	ST_CTR	Period counter consistency error: counted period ↔ calculated position
2	MT_CTR	Multiturn data consistency error: counted multiturn ↔ external MT data
1	MT_ERR	Multiturn communication: - Error bit set - CRC error [1)] - No start bit [1)] - General communication error
0	MT_WRN	Multiturn communication: - Warning bit set[1), 2)]
	Notes:	*) Relevant for all synchronization modes, i.e., MODE_ST with SYNC_S, SYNC_N set; for warning threshold see FRQ_TH, Table 113 [1)] MODE_MT = 0x1; [2)] MODE_MT = 0x4, 0x7 Error indication logic: 1 = true, 0 = false

Table 144: Status register: STATUS0

EPR_ERR indicates that a CRC error of the internal configuration was detected or an I2C communication error occurred during normal operation.

Note:
In case of an I2C communication error EPR_ERR is only reset after an error free I2C communication or with command SOFT_RES.

STATUS1 Addr. SER:0x73; bit 7:0		R
Bit	Name	Description of status message
7	ACS_MAX	Control error: range at max. limit (segment)
6	AM_MIN	Signal error: poor level (master)
5	AM_MAX	Signal error: clipping (master)
4	ACM_MIN	Control error: range at min. limit (master)
3	ACM_MAX	Control error: range at max. limit (master)
2	CT_ERR	New data request, although the conversion of the previous sensor data request has not yet completed*
1	RF_ERR	Conversion data not valid when latching data for output: e.g., excessive SSI clock frequency
0	TH_ERR	Excessive temperature error
	Notes	*) Relevant for synchronization modes MODE_ST = 0x00 to 0x0F, 0x18 to 0x1B (calculation routines must end before a new sensor data request) Error indication logic: 1 = true, 0 = false

Table 145: Status register: STATUS1

STATUS2 Addr. SER:0x74; bit 7:0		R
Bit	Name	Description of status message
7	TL_ERR	Temperature low error
6	AN_MIN	Signal error: poor level (nonius)
5	AN_MAX	Signal error: clipping (nonius)
4	ACN_MIN	Control error: range at min. limit (nonius)
3	ACN_MAX	Control error: range at max. limit (nonius)
2	AS_MIN	Signal error: poor level (segment)
1	AS_MAX	Signal error: clipping (segment)
0	ACS_MIN	Control error: range at min. limit (segment)
	Note	Error indication logic: 1 = true, 0 = false

Table 146: Status register: STATUS2

Note:
The status information Ax_MIN, Ax_MAX, ACx_MIN and ACx_MAX (x = M,S,N) is valid only if the regarding m, s or n track is configured with UBL_x (see p. 65) and is set to zero otherwise.

The status bits EPx_STAT (x = 1,2) change their behaviour according to CFGEW1 configuration (see Table 160). If EPx_STAT (x = 1,2) is configured to be visible

on the error/warning bit the captured EPx (x = 1,2) pin status is reported, i.e. once set externally the status information is maintained until the status register is reset. If EPx_STAT (x = 1,2) is not configured to be visible on the error/warning bit the actual pin status is reported.

Status bit EXT_ERR is set when the logic-level at pin NERR is low. It is only displayed in STATUS3 and not latched. It permits iC-MNF to report an error state of further ICs to the PLC, when the messaging IC pulls down the NERR pin. With devices featuring open-drain alarm outputs a wired-or bus logic can be installed.

CAL_ACT indicates an active calibration process, see chapter **AUTOMATIC CALIBRATION FEATURE**, p. 99 for details.

STATUS3		Addr. SER:0x75; bit 7:0	R
Bit	Name	Description of status message	
7	CMD_EXE	Command execution in progress, or iC-MNF in startup procedure	
	CMD_CNV	internal converter busy with MNF_CMD	
6	MT_CTR_E2P	Multiturn data consistency error stored in EEPROM *)	
5	ST_CTR_E2P	Period counter data consistency error stored in EEPROM *)	
4	CMD_ERR	Requested CMD could not be executed	
3	EXT_ERR	external NERR pin is at '0' (set by iC-MNF or other participants of the NERR-bus)	
2	CAL_ACT	calibration process in progress	
Bit	Name	not configured to error/warning bit with CFGEW1	configured to error/warning bit with CFGEW1
1	EP2_STAT	Pin EP2 is set (actual status)	Pin EP2 was set (captured status)
0	EP1_STAT	Pin EP1 is set (actual status)	Pin EP1 was set (captured status)
	Note	Error indication logic: 1 = true, 0 = false *) C2EPR must be enabled, see Tab. 148	

Table 147: Status register: STATUS3

CMD_CNV and CMD_EXE are indicated with the same status bit and are not stored, as opposed to the other status bits. CMD_CNV is set on the initialization of a command (MNF_CMD) which requires the internal converter. CMD_EXE is set on command execution and on system startup. Please refer to Table 157 to distinguish both messages.

C2EPR enables the storage of multiturn and period counter check errors (ST_CTR, MT_CTR) to the EEPROM. During the startup procedure the stored counter check errors (ST_CTR_E2P, MT_CTR_E2P) are read from the EEPROM (STATUS3_E2P) and displayed in STATUS3. If the status information of STATUS3 is cleared, then ST_CTR_E2P and MT_CTR_E2P will be reset in the EEPROM as well.

C2EPR	Addr. 0x40; bit 7	
C2EPR	Addr. SER:0x0; bit 7	Bank 1
Code	EEPROM savings of status bits ST_CTR, MT_CTR	
0x0	Disabled	
0x1	Enabled	

Table 148: Save counter check errors to EEPROM

Note:
To get an error message after system startup if either ST_CTR_E2P or MT_CTR_E2P are set, please note that the visibility of the ST_CTR_E2P and MT_CTR_E2P on the error bit has to be enabled with CFGEW1 (see Table 160).

STATUS3_E2P	Addr. 0x75; bit 7:0	
STATUS3_E2P	Addr. SER:0x35; bit 7:0	Bank 1
Bit	Name	Description of status message
7	-	not used
6	MT_CTR_E2P	
5	ST_CTR_E2P	
4..0	-	not used

Table 149: Actual status of MT_CTR_E2P and MT_CTR_E2P of corresponding bits in STATUS3

STATUS4		Addr. SER:0x76; bit 7:0	R
Bit	Name	Description of status message	
7	EPR_NO	No EEPROM on startup	
6	MT_MA	Pin MTMA is set *)	
5	MT_SLI	Pin MTSLI is set *)	
4	CMD_ACT	Command-register enabled → corresponding parameter PROT_CMD	
3	DIR_ACT	Dir-pin enabled → corresponding parameter NENDIR_P	
2	PRE_ACT	Preset-pin enabled → corresponding parameter PRES_CONF	
1	RES_ACT	0: HARD_RES configured to RES-pin 1: SOFT_RES configured to RES-pin → corresponding parameter RES_MODE	
0	RPL_ACT	Register protection enabled → corresponding parameter PROT_E2P	
	Note	Error indication logic: 1 = true, 0 = false *) visible with MODE_MT = 0x8 see p. 73	

Table 150: Status register: STATUS4

EPR_NO indicates that no EEPROM was found on system startup, the status bit remains set after the command SOFT_RES/CLEAR_STAT.

Registers STATEXT0 and STATEXT1 offer direct read-/write access to addresses 0x00 resp. 0x01 of an I2C device connected to the I2C bus with I2C Device ID = 0xC.

STATEXT0	Addr. SER:0x70; bit 7:0	R/W
Code	Function	
0x00 ... 0xFF	direct access to address 0x00 of I2C-Slave with I2C-Device-ID = b'110 0 000 *)	
Note	*) first 7 bit of I2C addressing sequence in binary representation (b'): 4 bit Device ID and upper 3 bit of 11 bit address	

Table 151: Status register: STATEXT0

STATEXT1	Addr. SER:0x71; bit 7:0	R/W
Code	Function	
0x00 ... 0xFF	direct access to address 0x01 of I2C-Slave with I2C-Device-ID = b'110 0 000 *)	
Note	*) first 7 bit of I2C addressing sequence in binary representation (b'): 4 bit Device ID and upper 3 bit of 11 bit address	

Table 152: Status register: STATEXT1

Non-Volatile Diagnosis Memory
E2EPR enables the storage of the individual status messages of STATUS0, STATUS1 and STATUS2 to the external EEPROM the first time they occur. EEPROM registers STATUS0_E2P, STATUS1_E2P and STATUS2_E2P are used for this purpose.

E2EPR **E2EPR**	Addr. 0x40; bit 6 Addr. SER:0x0; bit 6	 Bank 1
Code	EEPROM savings of cumulative status messages	
0x0 0x1	Disabled Enabled	

Table 153: Diagnosis memory enable

On a system startup iC-MNF reads in the status messages already stored in the EEPROM. As soon as an error message occurs which has not been stored in the external memory the corresponding status register bit is transferred to the EEPROM. This way a "cumulative" error register is compiled in which all messages are stored which occur during operation.

STATUS0_E2P **STATUS0_E2P**	Addr. 0x72; bit 7:0 Addr. SER:0x32; bit 7:0	 Bank 1
Bit	Name	Description of status message
7	TH_WRN	Cumulative error messages of STATUS0
6	EPR_ERR	
5	FQ_WDR	
4	CIF_ERR	
3	ST_CTR	
2	MT_CTR	
1	MT_ERR	
0	MT_WRN	

Table 154: Cumulative error messages of STATUS0

STATUS1_E2P **STATUS1_E2P**	Addr. 0x73; bit 7:0 Addr. SER:0x33; bit 7:0	 Bank 1
Bit	Name	Description of status message
7	ACS_MAX	Cumulative error messages of STATUS1
6	AM_MIN	
5	AM_MAX	
4	ACM_MIN	
3	ACM_MAX	
2	CT_ERR	
1	RF_ERR	
0	TH_ERR	

Table 155: Cumulative error messages of STATUS1

STATUS2_E2P **STATUS2_E2P**	Addr. 0x74; bit 7:0 Addr. SER:0x34; bit 7:0	 Bank 1
Bit	Name	Description of status message
7	TL_ERR	Cumulative error messages of STATUS2
6	AN_MIN	
5	AN_MAX	
4	ACN_MIN	
3	ACN_MAX	
2	AS_MIN	
1	AS_MAX	
0	ACS_MIN	

Table 156: Cumulative error messages of STATUS2

Only the current errors can be read out via the status register (BiSS Addr. SER: 0x72 to 0x74). The cumulative errors which are stored at EEPROM addresses 0x72 to 0x74 can only be read out through the I/O interface with PROT_E2P = 0x0 addressing bank 1, Addr. SER: 0x32-0x34 (see p. 59 ff. for memory map).

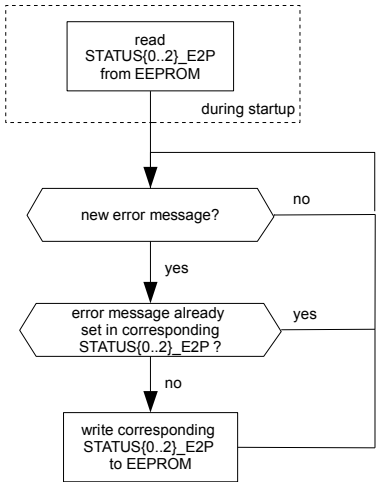


Figure 70: E2EPR: behavior in case of a new error message

Note:
Once configuration has been completed and before the system is delivered the data at the EEPROM addresses 0x72 to 0x74 should be initialized with zeroes.

Error And Warning Bit Configuration: Serial Protocol And NERR Pin

For further information regarding the output and the polarity of the error and warning bit within the different serial protocols see parameter MODE_SER Table 55.

With the exception of CMD_EXE, CMD_CNV, EPx_STAT (x = 1,2) and an external system error message (read in via I/O pin NERR and assigned to status bit EXT_ERR) all error codes mentioned in the following are stored in the status register should the corresponding error event occur (see p. 86) regardless of the configuration of the error/warning bit.

Some error messages are allocated fixed to the error and warning bit (see Table 157). There are others where the visibility on the error and warning bit can be changed with the CFGEWx (x = 0...2) parameters (see Table 158).

Note:
Parameters CFGEW0..2 also select the status bits which are enabled to switch the sin/cos output drivers to tristate if configured with DRVDIS, DRVMASK (see p. 37 for more information).

Fixed Allocation Of Error Messages		
Message	Visibility via error bit	Conditions
CMD_EXE CMD_CNV *) CT_ERR	•	None
RF_ERR	•	Visible when MODE_SER = 0x0-0x7, 0x9-0xF
MT_ERR	•	Visible when MODE_MT = 0x01 - 0x07
MT_CTR	•	Visible when MODE_MT ≠ 0x0 and CHK_MT = 0x01
ST_CTR	•	Visible when MODE_ST is set to counted nonius or multiturn synch. with output data verification
Notes	• visible see Conditions *) CMD_CNV is also visible for warning bit.	

Table 157: Fixed allocation of messages for error bit indication

Variable Allocation Of Error Messages		
Message	Visibility via error bit	Visibility via warning bit
Ax_MAX	○	○
Ax_MIN	○	○
ACx_MAX	△	○
ACx_MIN	△	○
TH_ERR	○	n/a
TH_WRN	n/a	○
TL_ERR	◊	n/a
MT_WRN	n/a	○
MT_CTR_E2P	△	n/a
ST_CTR_E2P	△	n/a
EP1_STAT	△	△
EP2_STAT	△	△
FQ_WDR	n/a	○
EXT_ERR	○	n/a
EPR_ERR	△	n/a
CMD_ERR	◊	n/a
Notes	○ = configurable with CFGEW0 △ = configurable with CFGEW1 ◊ = configurable with CFGEW2	

Table 158: Variable allocation of error messages for error/warning bit indication

CFGEW0	Addr. 0x3E; bit 7:0
Bit	**Visibility for error bit**
7	Ax_MAX, Ax_MIN
6	EXT_ERR
5	TH_ERR
Bit	**Visibility for warning bit**
4	FQ_WDR
3	Ax_MAX and Ax_MIN
2	ACx_MAX and ACx_MIN
1	TH_WRN
0	MT_WRN
Notes	Default is 0xFF: all messages enabled x = M, S, N **Encoding of bit 7...0:** **0 = message disabled, 1 = message enabled**

Table 159: Error and warning bit configuration: CFGEW0

CFGEW1	Addr. 0x3F; bit 7:0
Bit	**Visibility for error bit**
7	EPR_ERR
6	ACx_MAX, ACx_MIN
5	MT_CTR_E2P *)
4	ST_CTR_E2P *)
3	EP2_STAT
2	EP1_STAT
Bit	**Visibility for warning bit**
1	EP2_STAT
0	EP1_STAT
Notes	Default is 0x80 **Encoding of bit 7...0:** **0 = message disabled, 1 = message enabled** *) see parameter C2EPR, Tab. 148

Table 160: Error and warning bit configuration: CFGEW1

Note:
Configuring EPx_STAT (x = 1,2) to the error/warning bit using CFGEW1 also changes the type of status information (actual/captured) displayed in the status register STATUS3 (see Table 147).

CFGEW2 **CFGEW2**	Addr. 0x40; bit 1:0 Addr. SER: 0x0; bit 1:0 Bank 1
Bit	**Visibility for error bit**
1	TL_ERR
0	CMD_ERR
Note	**Encoding of bit 1...0:** **0 = message disabled, 1 = message enabled**

Table 161: Error bit configuration: CFGEW2

Error And Warning Bit Output Modes: Serial Protocol And NERR Pin
Different output modes for the protocol error and warning bit can be configured with parameter EWM. The NERR pin always behaves like the protocol error bit.

Note:
A status message that sets the protocol error bit also leads to an error reported by the NERR pin.

Only when active: Status messages configured to the error/warning bit are only reported if they are active at the current sensor data request.

At least once: Status messages configured to the error/warning bit are sampled when they occur and reported with the next sensor data communication.

As in status register: Status messages configured to the error/warning bit and stored in the status register are output to the error/warning bit. In this case the error/warning bit remains set until the relevant status register is reset.

EWM **EWM**	Addr. 0x40; bit 3:2 Addr. SER: 0x40; bit 3:2 Bank 1
Code	Error/Warning messages are reported
0x0	only when active[1]
0x1	at least once[1]
0x2	as in status register
0x3	as in status register, exception RF_ERR[2]
Note	[1]exception: CMD_ERR must be cleared according to RR_STAT (Tab. 143). [2]non saved value, only reported if triggered by current sensor data request

Table 162: Output modes for error and warning bit

General Purpose I/O Pins

iC-MNF offers two general purpose pins EP1 and EP2 which can be configured to be an input (high- or low-active) or an output (default state after startup: high or low).

If configured as an input the corresponding status EPx_STAT (x = 1,2) can be read out with STATUS3 and can be configured to the error/warning bit of the serial protocol with CFGEW1.

If configured as an output the default polarity (high or low) after startup can be configured with EPx_HL (x = 1,2). For a temporary change of the output polarity the commands SET0_EPx and SET1_EPx (x = 1,2) (see p. 93) can be used.

Note:
Changes to the parameters EPx_IO and EPx_HL (x = 1,2) only take effect after command SOFT_RES (see p. 93).

The visibility on the error/warning bit of the pin status EP1_STAT resp. EP2_STAT shall be disabled with CFGEW1 if pin EP1 resp. EP2 is configured as output pin.

EP1_IO	Addr. 0x32; bit 0
EP2_IO	Addr. 0x32; bit 1
Code	Function
0x0	input
0x1	output
Note	The command SOFT_RES should be executed for the changes to take effect

Table 163: EP1/2: input/output configuration

EP1_HL	Addr. 0x58; bit 0	
EP1_HL	Addr. SER:0x18; bit 0	Bank 1
EP2_HL	Addr. 0x58; bit 1	
EP2_HL	Addr. SER:0x18; bit 1	Bank 1
Code	EPx_IO = 0x0	EPx_IO = 0x1
0x0	input low-active	output 0
0x1	input high-active	output 1
Note	The command SOFT_RES should be executed for the changes to take effect x = 0,1	

Table 164: EP1/EP2: polarity

COMMAND REGISTER

Execution Of Internal Commands

Depending on the data value written to the command register at address 0x77 the execution of an implemented command is triggered.

MNF_CMD	Addr. SER:0x77; bit 7:0	W
Code	Command	Description
0x0	SOFT_RES	Soft reset (new startup using internal config. data)
0x1	WRITE_CONF	with RP0 *): Transfers internal config. data to the EEPROM with RP1 *): Transfers internal preset data to the EEPROM
0x2	SOFT_PRES_E2P	Calls preset routine and writes resulting offset values into EEPROM ***)
0x3	SOFT_PRES	Calls preset routine without writing the offset values into the EEPROM
0x4	CRC_CHECK	CRC verification of the internal config. data ***)
0x5	FORCE_BISS	force serial I/O interface to use BiSS protocol **)
0x6	FORCE_SPI	force serial I/O interface to use SPI protocol **)
0x7	UNFORCE_IF	release possible force to BiSS or SPI protocol; internal configuration for serial I/O interface is used
0x8	CLEAR_STAT	clear all status information in STATUS registers
0x9	SET0_EP1	with EP1 configured as output: set EP1 to low
0xA	SET1_EP1	with EP1 configured as output: set EP1 to high
0xB	SET0_EP2	with EP2 configured as output: set EP2 to low
0xC	SET1_EP2	with EP2 configured as output: set EP2 to high
0xD	CRC_CALC	Recalculate internal CRC_CFG, CRC_OFF and CRC_PRES values
0xE	HARD_RES	Hard reset (Startup with new read-in of the EEPROM)
0x21	FORCE_ERR	Force Error bit of serial interface to be set
0x22	UNFORCE_ERR	Release forced Error bit of serial interface
0x23	FORCE_WRN	Force Warning bit of serial interface to be set
0x24	UNFORCE_WRN	Release forced Warning bit of serial interface
Calibration Commands (detailed explanations see chapter AUTOMATIC CALIBRATION FEATURE, p. 99 ff.)		
0x10	CAL_SLC_M	calibrate signal level controller Master
0x11	CAL_GO_M	calibrate gain/offset (GO) Master
0x12	CAL_GOP_M	calibrate gain/offset/phase (GOP) Master
0x14	CAL_SLC_S	calibrate signal level controller Segment
0x15	CAL_GO_S	calibrate gain/offset Segment
0x16	CAL_GOP_S	calibrate gain/offset/phase Segment
0x18	CAL_SLC_N	calibrate signal level controller Nonius
0x19	CAL_GO_N	calibrate gain/offset Nonius
0x1A	CAL_GOP_N	calibrate gain/offset/phase Nonius
0x1C	CAL_TO	calibrate track offsets
0x1D	CAL_STOP	stop GO/GOP calibration
Reserved		
0xF, 0x1E, 0x1F, 0x25...0xFF	No function	reserved for future use
Notes	*) register protection levels configured with PROT_E2P see Table 94 **) has only effect if FORCE_SPI or FORCE_BISS is not conf. to inp. pin PRES (see PRES_CONF Table 172) ***) also available as BiSS protocol command see p. 47	

Table 165: Implemented commands

With PROT_CMD the execution of commands using the command register as well as BiSS Protocol Commands 0x2 and 0x3 (see p. 47) can be disabled.

PROT_CMD Addr. 0x44; bit 4 **PROT_CMD** Addr. SER:0x04; bit 4 Bank 1	
Code	MNF_CMD, BiSS Protocol Commands 0x2, 0x3
0x0 0x1	enabled disabled
Note	The command SOFT_RES should be executed for the protection of the command register to take effect

Table 166: Protection of command register

Note:
After enabling the MNF_CMD register protection by setting PROT_CMD to 0x1 the command SOFT_RES should be executed for the MNF_CMD register protection to take effect.
If PROT_CMD = 0x1 should be written to the external EEPROM the command WRITE_CONF should be executed before command SOFT_RES.
Since the CLEAR_STAT command is disabled with PROT_CMD = 0x1 it is recommended to set RR_STAT to 0x1, so that the status registers can be reset.

SOFT_RES resets internal state machines, counters, and the status registers, starts a 60 µs timeout. The configuration RAM is not reset here. During the 60 µs timeout, register access is not possible. During the rest of the command execution accessing the internal RAM is possible, whereas the external EEPROM is not accessible.

If the device is in counted nonius or multiturn mode (see p. 67), the first conversion is used to determine the period and the result stored as an initial value for the period fraction of the internal flash counter. If an external multiturn device is configured (MODE_MT ≠ 0x0), its data is read in and stored as the initial value for the multiturn data fraction of the internal flash counter. The startup after command SOFT_RES is described in Figure 17, p. 42.

Note:
Changes to the parameters PROT_CMD, PROT_E2P, EPx_IO and EPx_HL (x = 1,2) only take effect after command SOFT_RES.

Note:
The command SOFT_RES must be executed after an incorrect EEPROM configuration (e.g. empty EEPROM or CRC checksum error). For more information see section Startup Behavior on page 41.

HARD_RES resets internal state machines, counters, status registers and the internal configuration RAM and initiates a new startup with a read-in of the external EEPROM configuration data. For the startup sequence please refer to chapter **Startup**, p. 41 ff.

ATTENTION:
When using the SPI interface (MODE_SER = 0x8, see Tab. 54) a time of tready()cfg * 1.3 (see Elec. Char. 904) must be waited for after the **HARD_RES** command. Then the REGISTER status/data opcode must be sent. The read-back value can be discarded.

With **WRITE_CONF** and PROT_E2P set to RP0 the internal configuration, offset and preset-values are stored to the EEPROM. The CRCs (CRC_CFG/CRC_OFF and CRC_PRES) are automatically updated and written.

With **WRITE_CONF** and PROT_E2P set to RP1 the internal preset values are stored to the EEPROM. The CRC (CRC_PRES) is automatically updated and written.

Note:
Commands **WRITE_CONF** and **SOFT_PRES_E2P / SOFT_PRES** block iC-MNF's internal RAM for accesses for a certain time. During this time the addresses of the register operations via the I/O interface will be dismissed and bit CMD_EXE of the status register is set.

ATTENTION!
During the **WRITE_CONF** and **SOFT_PRES_E2P** wait time it must be ensured that the supply voltage to the two devices iC-MNF and the EEPROM is maintained. If this is not the case, on the next system startup the whole configuration parameter may be recognized as being faulty and this will trigger the setting of the error bit (EPR_ERR) in the status register!

SOFT_PRES initiates a preset sequence (see p. 63 ff.) with preset values PRES_ST and PRES_MT. The internal offset values OFFS_ST and OFFS_MT are changed to set the output value to the value given by PRES_ST and PRES_MT. The internal CRC_OFF is automatically updated.

SOFT_PRES_E2P initiates a preset sequence (see p. 63 ff.) with preset values PRES_ST and PRES_MT. The altered offset values OFFS_ST and OFFS_MT are stored in the EEPROM. CRC_OFF is automatically updated.

Both commands **SOFT_PRES** and **SOFT_PRES_E2P** can be restricted to preset only the multiturn part

using parameters PRES_MODE and FPRES_MT. PRES_MODE is located in the protectable configuration data area. FPRES_MT is located in the PRESET configuration area which is accessible in PROT_E2P = RP1.

PRES_MODE Addr. 0x44; bit 3 **PRES_MODE** Addr. SER:0x04; bit 3 Bank 1	
Code	Function
0x0 0x1	ST+MT preset restrict to MT part *)
Note	*) CDL_MT affects bits used for preset see Table 169

Table 167: Preset mode for SOFT_PRES, SOFT_PRES_E2P

FPRES_MT Addr. 0x58; bit 3 **FPRES_MT** Addr. SER:0x18; bit 3 Bank 1	
Code	Function
0x0 0x1	no force (see PRES_MODE) restrict to MT part *)
Note	*) CDL_MT affects bits used for preset see Table 169

Table 168: Restrict SOFT_PRES, SOFT_PRES_E2P to MT part

In systems where the preset is restricted with PRES_MODE and FPRES_MT but 1 or 2 bits of the multiturn data form part of the singleturn information, parameter CDL_MT can be used to exclude those bits for the multiturn preset.

CDL_MT Addr. 0x3C; bit 6:5	
Code	Unchanged bits
0x2 0x3	LSB of MT i.e. OFFS_MT(0) LSB+1 and LSB of MT i.e. OFFS_MT(1:0)
Note	for more information on CDL_MT, see Table 59, p. 45

Table 169: Excluded bits from OFFS_MT recalculation in restricted MT preset modes (FPRES_MT = 0x1 or PRES_MODE = 0x1)

Note:
CDL_MT in combination with parameter ECDL_MT also affects the multiturn output data length via the I/O interface (see p. 45).

CRC_CHECK starts a CRC verification of the internal configuration RAM. During the check the internal data bus may not be accessed. Should the check not confirm the configuration data as error free, status bit EPR_ERR is set.

CRC_CALC starts a recalculation of CRC_CFG, CRC_OFF and CRC_PRES. The CRC values are saved internally in iC-MNF and are used for later CRC verifications.

FORCE_BISS forces the serial I/O interface to use the BiSS protocol (MODE_SER = 0x0, see p. 44).

FORCE_SPI forces the serial I/O interface to use the SPI protocol (MODE_SER = 0x8, see p. 44).

UNFORCE_IF releases an active **FORCE_BISS** or **FORCE_SPI** and the internal configuration of the serial I/O interface is used.

SET1_EPx (x = 1,2) sets pin EP1/EP2 to logic level 1 if EP1/EP2 is configured as output.

SET0_EPx (x = 1,2) resets pin EP1/EP2 to logic level 0 if EP1/EP2 is configured as output.

CLEAR_STAT clears the status information of STATUS0, STATUS1, STATUS2 and STATUS3 (see chapter **Status Register**, p. 86).

Automatic Reset Function

An automatic reset function triggered with the AM_MIN error can be activated with parameter AUTORES.

If AUTORES is activated then for as long as the amplitude of the master track is too low, i.e. the AM_MIN error is set, iC-MNF is held in SOFT_RES state which resets internal state machines, counters, and the status registers. When AM_MIN is no longer set, the timeout configured using AUTORES expires. After the timeout the SOFT_RES state is left and the device subsequently returns to normal operation. This behaviour is described in Figure 71.

Should an AM_MIN error occur during the execution of a command or the preset function, SOFT_RES is delayed until the command in execution has been terminated.

The behavior of the I/O interface with an active SOFT_RES depends on the protocol selected. For **BiSS C** a zero is returned as a data value and the error and warning bits are set; for **SSI** the SLO pin is set to high level. A connected control unit can detect this error by checking the stop-bit which is send after each SSI datagram. In both cases (SSI and BiSS C) the error state is indicated at pin NERR with a low signal.

AUTORES	Addr. 0x30; bit 1:0
Code	Function
0x0	No automatic reset
0x1	SOFT_RES after error AM_MIN, timeout 8 ms
0x2	SOFT_RES after error AM_MIN, timeout 16 ms
0x3	SOFT_RES after error AM_MIN, timeout 32 ms

Table 170: Automatic reset function

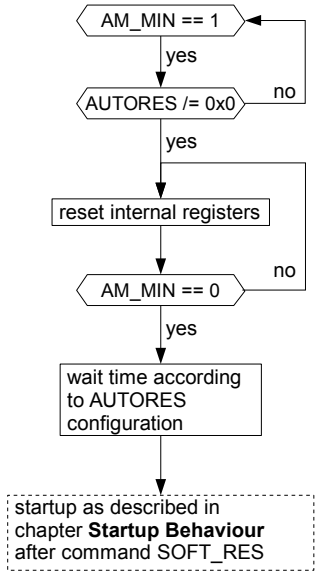


Figure 71: Automatic Reset Function (startup after SOFT_RES see Fig. 17, p. 42)

Configurable Reset Pin

iC-MNF has a configurable reset pin (RES) which is high-active. The RES-Pin behaviour can be configured using parameter RES_MODE.

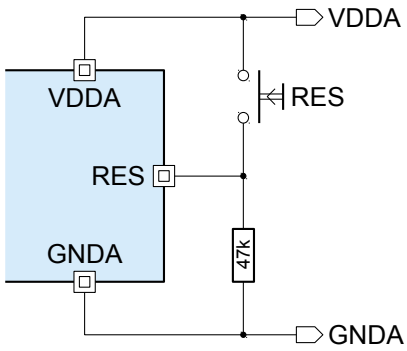


Figure 72: Example of external circuitry for RES functionality

Note:
During startup the RES pin is configured to execute the command HARD_RES. After a successful read-in of valid data from the external EEPROM a high level of the RES pin triggers the command configured with RES_MODE.

The minimum time that the RES pin must be active for the reset command to be recognized internally is given by Elec. Char. no. K05.

RES_MODE	Addr. 0x44; bit 6	
RES_MODE	Addr. SER:0x04; bit 6	Bank 1
Code	RES pin configuration	
0x0	HARD_RES	
0x1	SOFT_RES	

Table 171: RES pin configuration

If RES_MODE is configured to **SOFT_RES** and pin RES is high iC-MNF is held in SOFT_RES state. This resets internal state machines, counters, and the status registers. The configuration RAM is not reset. During the command execution a write access to the configuration RAM is still possible, whereas the external EEPROM is not accessible.
If pin RES is set back to low the SOFT_RES state is left. If the device is in counted nonius or multiturn mode (see p. 67), the first conversion is used to determine the period and the result stored as an initial value for the period fraction of the internal flash counter. If an external multiturn device is configured (MODE_MT ≠ 0x0), its data is read in and stored as the initial value for the multiturn data fraction of the internal flash counter (startup after SOFT_RES see Fig. 17, p. 42).

If RES_MODE is configured to **HARD_RES** and pin RES is high iC-MNF is held in HARD_RES state. This resets internal state machines, counters, status registers, and the configuration RAM. During the command execution a write access to the configuration RAM is still possible, whereas the external EEPROM is not accessible.
If pin RES is set back to low the HARD_RES state is left and the startup sequence is started as described in chapter **Startup**, p. 41 ff.

Configurable Command Input PRES

iC-MNF has a configurable command input, the high active input pin PRES, which can be used to execute a command configured with parameter PRES_CONF.

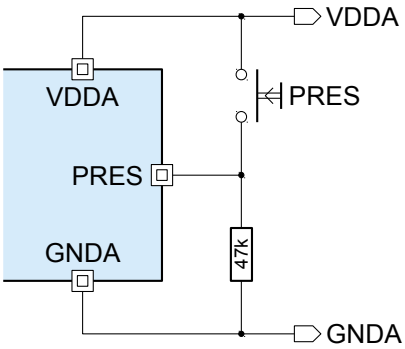


Figure 73: Example of external circuitry for PRES functionality

Execution of all commands except the FORCE_BISS and FORCE_SPI commands starts after a rising edge at input pin PRES. The FORCE_BISS and FORCE_SPI command is active dependent on the logic level at input pin PRES (high → active, low → inactive).

Note:
The minimum time that the input pin PRES must be active for the configured command to be recognized internally is given by Elec. Char. no. K05.

PRES_CONF Addr. 0x44; bit 2:0 **PRES_CONF** Addr. SER:0x04; bit 2:0 Bank 1			
Code	Command	started with rising edge	logic level dependent
0x0	SOFT_PRES_E2P	✓	-
0x1	SOFT_PRES	✓	-
0x2	CRC_CHECK	✓	-
0x3	FORCE_BISS *)	-	✓
0x4	FORCE_SPI *)	-	✓
0x5 . . . 0x7	DISABLED / NO_FUNCTION		
Note	*) disables FORCE_BISS and FORCE_SPI commands in command register (MNF_CMD)		

Table 172: Command configured to input pin PRES

Note:
Configuring FORCE_BISS or FORCE_SPI to pin PRES deactivates the related commands MNF_CMD 0x5, 0x6, 0x7.

AUTOMATIC CALIBRATION FEATURE

iC-MNF offers self calibration functions which can be used to refine the analog calibration parameters in a special setup procedure. Those functions require a clean basic setup and a final review of the resulting parameter set. The recommended proceeding is summarized in Fig. 74.

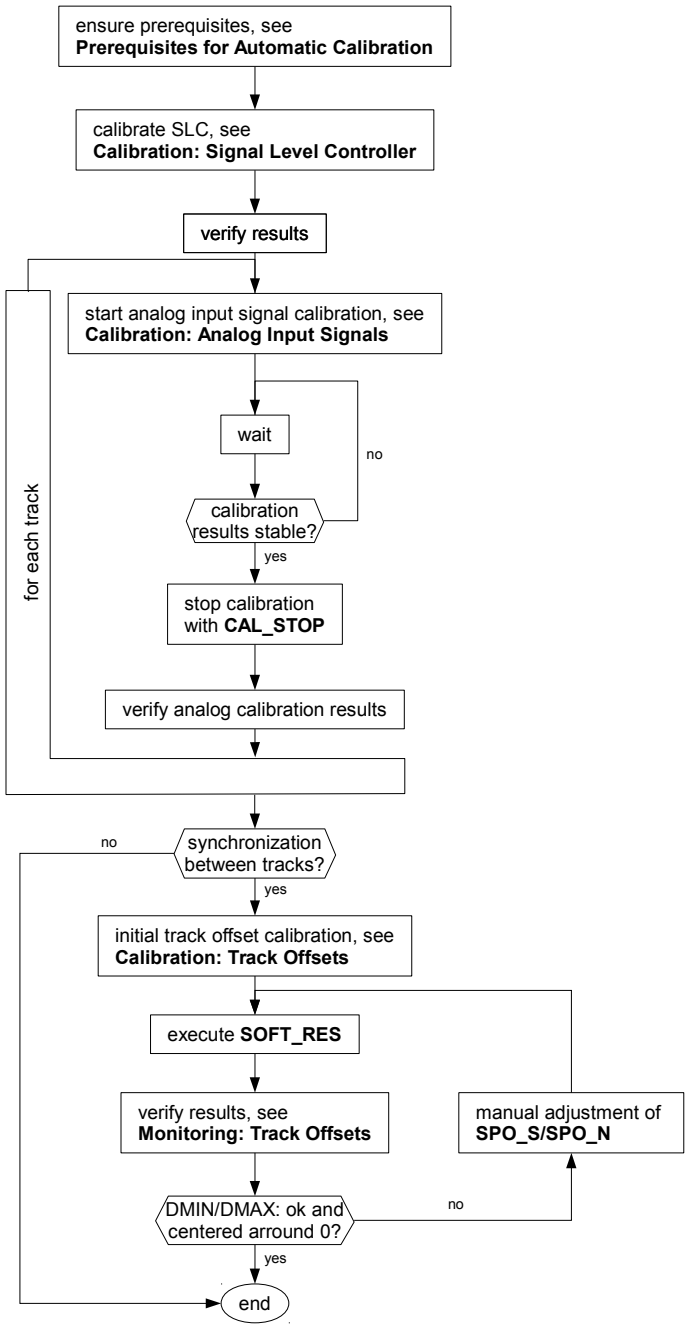


Figure 74: Automatic calibration: recommended proceeding

Calibration Commands and Status

There are two groups of self calibration functions. The first group is used to compensate gain, offset and phase errors in the analog input signals. The second group optimizes the track offset parameters for the nonius calculation.

Those self calibration functions go along with monitoring functions to determine the safety margins for the nonius calibration.

MNF_CMD	Addr. SER: 0x77; bit 7:0	W
Calibrate: Signal Level Controller		
0x10	CAL_SLC_M	calibrate signal level controller Master
0x14	CAL_SLC_S	calibrate signal level controller Segment
0x18	CAL_SLC_N	calibrate signal level controller Nonius
Calibrate: Analog Input Signals		
0x12	CAL_GOP_M	calibrate gain/offset/phase (GOP) Master
0x16	CAL_GOP_S	calibrate gain/offset/phase Segment
0x1A	CAL_GOP_N	calibrate gain/offset/phase Nonius
Calibrate: Track Offsets		
0x1C	CAL_TO	calibrate track offsets
Calibration Stop Command		
0x1D	CAL_STOP	stop calibration/measurement

Table 173: Calibration Commands

After an automatic calibration function is started, status bit CAL_ACT (see STATUS3, Table 147) is set.

STAT_CAL gives feedback over the state of the calibration process (s. Fig. 75, 76, 78).

STAT_CAL	Addr. SER:0x6B; bit 2:0 Addr. SER:0x29; bit 2:0	Bank 1
Code	Function	
0x00	idle	
0x01	searching operating point to start calibration	
0x02	doing coarse calibration	
0x03	doing fine calibration	
0x07	CAL_SLC and CAL_TO: Calibration finished	

Table 174: Status: Automatic Calibration

When the current input frequency of the analog signals is too fast status bit STAT_CIF is set.

STAT_CIF	Addr. SER:0x6B; bit 7 Addr. SER:0x29; bit 7	Bank 1
Code	Function	
0x0	-	
0x1	input signals too fast	

Table 175: Status: input signals too fast

Note:
STAT_CIF is also latched and visible as CIF_ERR in status register STATUS0 (see p. 86).

Prerequisites for Automatic SLC and Analog Input Signal Calibration

1. Operating mode must be set to "Normal".

Operating Mode Normal	
Code	Description
TRACMODE	Addr. 0x30; bit 7:5
0x0	normal operation
TEST	Addr. 0x31; bit 5:0
0x0	normal operation
BYP_M	Addr. 0x0B; bit 7
0x0	no bypass
BYP_S	Addr. 0x1B; bit 7
0x0	no bypass
BYP_N	Addr. 0x2B; bit 7
0x0	no bypass

Table 176: Addresses of parameters affecting the operation mode

2. Output Mode MODE_ST must be set to "Cyclically Converted" (see Table 110 and 111).

3. Signal level controller (SLC) used for the application must be set to "Constant current source mode" (see Table 31).

4. Sine/cosine coarse gain factors GR_x (x = M,S,N) should be set to the target value (see Table 16).

5. Maximum output current ACOR_x (x = M,S,N) should be in the correct range (see Table 29 f).

6. Current source setpoint ACOCON_x (x = M,S,N) should be set to the expected target values given by the actual implementation (see Table 33).

7. Sine/cosine fine gain factor GFS_x and GFC_x (x = M,S,N) should be set to the expected target values given by the actual implementation (see Table 17 f.).

Calibration: Signal Level Controller
iC-MNF has three signal level controllers, one for each track. So that the output signals can be calibrated without control interference, the relevant signal level controller output ACOx has to be set to constant current (see Table 31). The parameter for the maximum output current ACOR_X (see Table 29 f) must be set properly. Parameter ACOCON_x (see Table 33) must be set to a plausible start value and can be automatically optimized with the self calibration function CAL_SLC_x.

CAL_SLC_M is the self calibration function for the 'master signal level controller' which monitors the sine and cosine amplitudes of the master channel. The ACOCON_M parameter is modified until the amplitude of the master channel is just below the optimal working point. The calibration function ends automatically when the operating point was found.

CAL_SLC_S is the self calibration function for the 'segment signal level controller' which monitors the amplitudes of the segment channel and modifies the ACOCON_S parameter.

CAL_SLC_N is the self calibration function for the 'nonius signal level controller' which monitors the amplitudes of the nonius channel and modifies the ACOCON_N parameter.

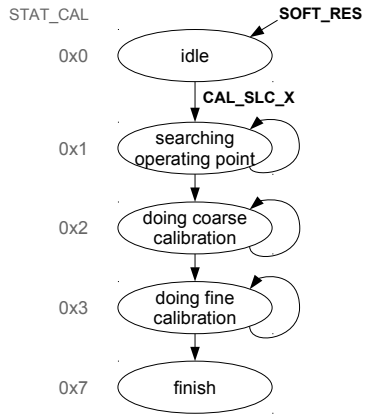


Figure 75: Status information sequence of CAL_SLC_X (STAT_CAL, see Table 174)

Note:
The automatic signal level controller calibration requires a signal change on the sine/cosine input signals which corresponds to a sine frequency below 10 kHz.

Calibration: Analog Input Signals
The self calibration function (CAL_GOP_x) monitors the sine and cosine input signal of a channel to derive residual errors which are used for an iterative optimization of the gain, offset and phase parameters. The quality of the calibration results depend on the equality of the sine periods. Residual errors are calculated after each sine period and small correction factors are applied immediately.

No correction is applied when the residual error calculation was not possible. This can happen if the initial input signal conditioning is too bad (Out of Range Error; visible when STAT_CAL stays in "searching operating point"), when the input signal frequency is too high (CIF_ERR) or when the *rotation direction* is changing.

The self calibration function is active until it is stopped with command **CAL_STOP**.

The self calibration function **CAL_GOP_M** monitors the input signals of the master channel and optimizes the parameters GFS_M, GFC_M, OFS_M, OFC_M and PH_M (see chapter SIGNAL CONDITIONING for MASTER-, SEGMENT- and NONIUS-Channel, p. 29 ff).

The self calibration function **CAL_GOP_S** monitors the input signals of the segment channel and optimizes the parameters GFS_S, GFC_S, OFS_S, OFC_S and PH_S.

The self calibration function **CAL_GOP_N** monitors the input signals of the nonius channel and optimizes the parameters GFS_N, GFC_N, OFS_N, OFC_N and PH_N.

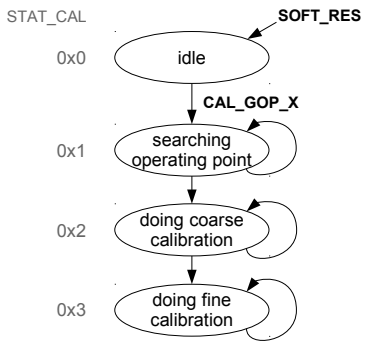


Figure 76: Status information sequence of CAL_GOP_X (STAT_CAL, see Table 174)

Note:
The automatic calibration of the analog input signals requires a signal change on the sine/cosine input signals which corresponds to a sine frequency below 10 kHz.

Prerequisites for Track Offset Calibration

1. Operating mode must be set to "Normal".

Operating Mode Normal	
Code	Description
TRACMODE	Addr. 0x30; bit 7:5
0x0	normal operation
TEST	Addr. 0x31; bit 5:0
0x0	normal operation
BYP_M	Addr. 0x0B; bit 7
0x0	no bypass
BYP_S	Addr. 0x1B; bit 7
0x0	no bypass
BYP_N	Addr. 0x2B; bit 7
0x0	no bypass

Table 177: Addresses of parameters affecting the operation mode

2. Analog signals must be calibrated.

Calibration: Track Offsets
iC-MNF can be used in a 2-track or 3-track nonius mode. The result of the S/D conversion is used to compute the absolute single turn position in these synchronization modes. The static phase shift between the tracks must be compensated with the corresponding track offset parameter (SPO_S, SPO_N) to avoid ambiguous input data for the synchronization logic.

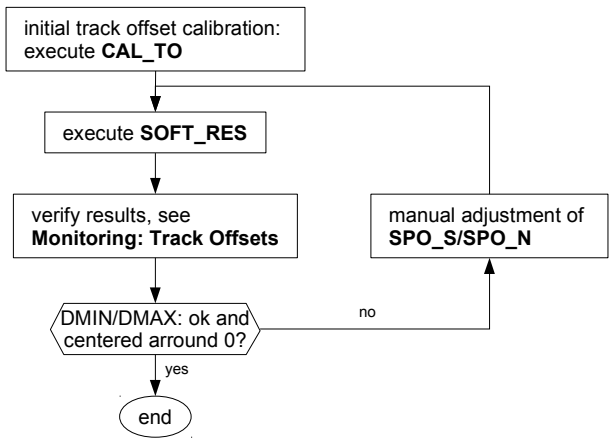


Figure 77: Recommended proceeding: track offset calibration

CAL_TO starts the function to get the optimal values for the track offset parameters at the current position. The calibration function ends automatically after setting the track offset parameters.

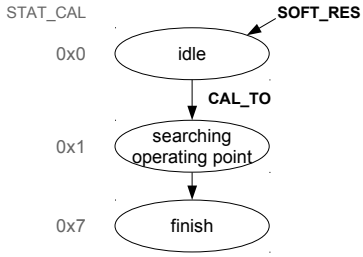


Figure 78: Status information sequence of CAL_TO (STAT_CAL, see Table 174)

It is recommended to do a check for unambiguousness over all possible positions after setting the track offset parameters, e.g. with the integrated **Monitoring: Track Offsets**.

Note:
After a successful calibration of the track offsets, the command WRITE_CONF should be executed to save the new SPO_x (x = S,N) values to the EEPROM.

Monitoring: Track Offsets

The track offset monitoring is always active and monitors the phase margin of each nonius synchronization. The minimum and maximum values are stored in DMIN_N, DMAX_N, DMIN_S and DMAX_S. The command SOFT_RES can be used to reset those values.

The track offset monitoring can be used to determine the optimal values for the parameters SPO_N and SPO_S (see Fig. 77) or for quality monitoring during assembly. To do so, please set MODE_ST to a *cyclically converted* synchronization mode with always enabled output data verification to ensure an exhaustive track offset monitoring. Please change the position so that the significant traveling distance is covered by the test and return to the original position, so that this test is done for both directions.

The DMIN/DMAX_X values can be used to benchmark the quality of the phase difference of the input signals. The min/max track offset values should be centered around 0. The system is expected to fail if one of the values reaches ±7.5.

DMIN_N	Addr. SER:0x6D; bit 3:0	
DMAX_N	Addr. SER:0x6D; bit 7:4	
DMIN_S	Addr. SER:0x6E; bit 3:0	
DMAX_S	Addr. SER:0x6E; bit 7:4	
Code	Value	
0x0	-7.5	↯ lower limit ↯
0x1	-6.5	
...		
0x5	-2.5	
0x6	-1.5	↑
0x7	-0.5	ideal
0x8	0.5	ideal
0x9	1.5	↓
0xA	2.5	
...		
0xF	7.5	↯ upper limit ↯

Table 178: Min/Max track offset

DEVICE TEST (iC-Haus internally)

Registers which have to be set to 'default operation mode' to ensure proper operation of the device:

OPTEST	Addr. 0x31; bit 7:6
Code	Function
0x0	Reserved for test
0x1	Reserved for test
0x2	Reserved for test
0x3	Default operation mode

Table 179: OPTEST

NHYS	Addr. 0x1D; bit 3
Code	Function
0x0	Reserved for Test
0x1	Default operation mode

Table 180: NHYS

LGSH	Addr. 0x2D; bit 3
Code	Function
0x0	Default operation mode
0x1	Reserved for test

Table 181: LGSH

APPLICATION NOTES: PLC Operation

PLC Operation

There are PLCs with a remote sense supply which require longer for the voltage regulation to settle. At the same time the PLC inputs can have high-impedance resistances relative to an internal, negative supply voltage which define the input potential for open inputs.

In this instance iC-MNF's reverse polarity protection feature can be activated as the outputs are tristate during the start phase and the resistances in the PLC determine the pin potential. During the start phase neither the supply VDD nor the output pins, which are also monitored, must fall to below ground potential (pin GND); otherwise the device is not configured and the outputs remain permanently set to tristate.

In order to ensure that iC-MNF starts with the PLCs mentioned above pull-up resistors can be used in the encoder. Values of 100 kΩ are usually sufficient; it is, however, recommended that PLC specifications be specifically referred to here.

DESIGN REVIEW: Notes On Chip Functions

iC-MNF X1		
No.	Function, Parameter/Code	Description and Application Notes
1	Temperature high thresholds ETH_TEM ETL_TEM	Temperature high warning/error threshold (ETH_TEM) and temperature low error threshold (ETL_TEM) have an offset of -2°C, e.g.: ETH_TEM = 0x0 = 68/83°C and ETL_TEM = 0x1 = -2°C
2	S/D Conversion MODE_ST = 0x02 to 0x05	It is not allowed to set UBL_M = 0x0 & UBL_S = 0x0 & UBL_N = 0x0. Otherwise, there will be no access to the communication interface.
3	Multiturn: 2-Bit Mode Parallel MODE_MT = 0x8; CHK_MT = 0x1	In 2-bit MT mode, the multiturn data check may fail and trigger the MT_CTR error if the signals applied to MTSLI or MTMA change synchronously at the time of the check. This error message is displayed until the next check after 8 ms, although the position data is still valid. If the signals applied to MTSLI or MTMA change synchronously with scanning during start-up, initialization may be incorrect. In this case, the MT_CTR error is displayed with the first check (after 8 ms) and all further checks. A system reboot is required to re-initialize.
4	Output Modes: MODE_ST = 0x00 to 0x17 (Data Generation: counted)	If during start-up the internal flash counter is sampled simultaneously with the zero crossing of a noisy sine signal of the master track, the internal flash counter can be incorrectly initialized by ±1 master period. If MODE_ST with Output Data Verification is used, this state is detected and displayed via the status message ST_CTR or MT_CTR, starting with the first and all further checks. A system restart (power cycle) or execution of the SOFT_RES command is required for re-initialization.
5	I/O Interface: ExtSSI with sign-of-life counter MODE_SER = 0xF, ELC = 0x1	Function not implemented. The sign-of-life counter would always returns "111111".
6	I/O Interface: SSI, ExtSSI MODE_SER = 0x2 to 0x7, 0x9 to 0xF	The first SSI communication may return 0.
7	Status Message: FQ_STUP STATUS0, Bit 4	The status message FQ_STUP is not operational.
8	BiSS Protocol Commands	Command CMD = 0x01 (Deactivate control communication) works only if ETS = 1.
9	Configurable Preset Pin PRES_CONF = 0x3, 0x4	Command MNF_CMD = 0x05 - 0x7 (Interface force: BiSS/SPI/Unforce) are disabled when either FORCE_BISS or FORCE_SPI is configured to pin PRES

Table 182: Notes on chip functions regarding iC-MNF chip release X1

iC-MNF X3		
No.	Function, Parameter/Code	Description and Application Notes
1	BiSS Protocol Commands	Command CMD = 0x01 (Deactivate control communication) works only if ETS = 1.
2	Configurable Preset Pin PRES_CONF = 0x3, 0x4	Command MNF_CMD = 0x05 - 0x7 (Interface force: BiSS/SPI/Unforce) are disabled when either FORCE_BISS or FORCE_SPI is configured to pin PRES

Table 183: Notes on chip functions regarding iC-MNF chip release X3

REVISION HISTORY

Rel.	Rel. Date[1]	Chapter	Modification	Page
A1	2018-03-09		Initial release	all

Rel.	Rel. Date[1]	Chapter	Modification	Page
A2	2018-08-17	PACKAGING INFORMATION	Updated Figure PIN CONFIGURATION QFN48-7x7	5
		ELECTRICAL CHARACTERISTICS	Item 110: changed name VREFin to VREFI Item 605: reduced conversion times (e.g. CNVSPD= 0x1, ≤ 14 bit, 2.3µs → 1.8µs) Item F12: corrected Item F13: added	8, 10, 13
		I/O Interface	Operating Conditions BiSS C Protocol: Item I108: corrected max. value Item I112, I113 and I114: values added Updated Figure 5	17
		REGISTER ASSIGNMENTS (EEPROM)	Updated Figure 8	22
		REGISTER ACCESS USING THE I/O INTERFACE	Updated Figure 43	58
		MULTITURN INTERFACE	Updated Figure 65	83
		DESIGN REVIEW: Notes On Chip Functions	Removed iC-MNF chip release Y and Y1 Updated notes on chip functions regarding iC-MNF chip release X1	106

Rel.	Rel. Date[1]	Chapter	Modification	Page
B1	2019-09-16	ELECTRICAL CHARACTERISTICS	New items 512, 513 Item 710 deleted Item 904 corrected: 13.8ms → 15.1ms and 21.8ms → 25ms Item C01 corrected: all values + 2 Item F02: condition corrected, typ. value changed 20kOhm → 23kOhm, max. value changed 25kOhm → 32kOhm Item F15 corrected: 2ms → 8ms Item L09 deleted	10
		OPERATING REQUIREMENTS	SPI Protocol: Added items I126, I127, I128, I129 Updated Figure 7	17
		BATTERY MANAGEMENT AND MNFOK OUTPUT	Chapter revised, switch conditions for MNFOK added	38
		EEPROM AND I2C INTERFACE	Chapter "I2C INTERFACE AND STARTUP BEHAVIOR" divided into: - EEPROM AND I2C INTERFACE - STARTUP BEHAVIOR	39, 41
		STARTUP BEHAVIOR	Note regarding CMD_EXE and NERR pin during startup added Figure 17: 60 µs timeout after CMD = SOFT_RES added New: Startup with BiSS after configuration error (CRC or no EEPROM)	41 f
		I/O INTERFACE	Configuring data length: text regarding multiturn data length DL_MT revised BiSS protocol - description about the build-in RS422 line driver added ExtSSI - New for iC-MNF X3: sign-of-life counter can be configured for output SPI: Recommendation to terminate Write REGISTER (single) with REGISTER status/-data SPI: SDAD transmission can be used with MODE_ST set to T3 triggered data SPI: updated Figure 34 and Figure 42 SPI: Read/Write REGISTER (cont.) address areas for these commands specified SPI: Note added regarding opcode Write INSTRUCTION and command HARD_RES	44, 49, 51 ff
		REGISTER ACCESS USING THE I/O INTERFACE	Updated Figure 44 Table 93: CHIP_REL for iC-MNF X3 added New Figure 45: set/reset of register protection Note added explaining restriction for WRITE_CONF when RP1 is active Table 95: note added	59, 60, 61 f
		S/D CONVERSION: SYNCHRONIZATION MODE AND TYPE OF OUTPUT DATA	Note added for MODE_ST=0x16-0x17 and 0x1E-0x1F: sensor data error bit within serial protocol set until first T3 trigger Application Hint regarding parameter EUS (tab. 112) enhanced	69 f
		TRACK OFFSET CALIBRATION	data length for SPO_x corrected from 16 bit to 14 bit	72
		MULTITURN INTERFACE	Table 117 added Table 123: description of DL_EXT_MT = 0x0 corrected (setting does not deactivate the external MT interface) Description for direct communication with MT sensor using SSI protocol revised	73 f, 83

		STATUS REGISTERS AND ERROR MONITORING	Table 144, Bit 4: status message FQ_STUP (Excessive signal frequency on master track: during startup) removed Table 147: MT_CTR_E2P and ST_CTR_E2P description revised Added Table 149: STATUS3_E2P Table 150: added corresponding parameters for status bits Changed caption Error And Warning Bit Configuration: BiSS/SSI → Serial Protocol Table 162: exception for status bit CMD_ERR added General Purpose I/O Pins: Note added regarding output mode and visibility on protocol error/warning	86 ff
		COMMAND REGISTER	Table 165: new commands FORCE_ERR, UNFORCE_ERR, FORCE_WRN, UNFORCE_WRN PROT_CMD: note added regarding CLEAR_STAT command HARD_RES command: Note added regarding opcode Write INSTRUCTION and command HARD_RES SOFT_RES command: information added on 60 µs timeout after SOFT_RES and restriction during timeout on register access Table 167, 168: minor changes Configurable Reset Pin: note added regarding minimum active time Configurable Preset Pin: note added regarding minimum active time	93 ff
		DESIGN REVIEW: Notes On Chip Functions	Updated notes on chip functions regarding iC-MNF chip release X1 Added notes on chip functions regarding iC-MNF chip release X3	106

Rel.	Rel. Date[1]	Chapter	Modification	Page
C1	2023-12-19	PACKAGING INFORMATION	Description of pin functions, update of footnotes	5
		ELECTRICAL CHARACTERISTICS	Item 102 corrected: from +-20nA to +- 100nA	8
		OPERATING REQUIREMENTS	Revised Figure 1: SSI sampling at rising clock edge	16
		REGISTER ASSIGNMENTS (EEPROM)	Table 3, 5, 6, 8, 9, 10: changed byte order of parameters DEV_ID, MFG_ID, PRO_ID1, PRO_ID0, SER_NO	25 f
		BATTERY MANAGEMENT AND MNFOK OUTPUT	Figure 15: battery management circuit overview updated	38
		EEPROM AND I2C INTERFACE	Revised application hint about interconnection with iC-PVL	39
		STARTUP BEHAVIOR	Updated note boxes, note added regarding MAO internal pull-down for selection of the BiSS interface as default.	41
		I/O INTERFACE	BiSS busy shift register length corrected from 16 to 15 bits	46
		I/O INTERFACE	Table 67 updated, added condition ETS = 1	47
		I/O INTERFACE	Revised REGISTER commands which are not executed with RACTIVE = 0: added Read REGISTER (cont.) delayed, Write REGISTER (cont.)	52
		REGISTER ACCESS USING THE I/O INTERFACE	Table 91: changed byte order of parameters PRO_ID0, SER_NO, DEV_ID, MFG_ID	60
		S/D CONVERSION: DATA LENGTH AND DATA LENGTH DEPENDENCIES	Table 105: added settings for 2-track nonius mode with 8/7 and 4/3 Master/Nonius track signal periods	66
		MULTITURN INTERFACE	Table 125: caption updated	75
		STATUS REGISTERS AND ERROR MONITORING	Table 145: CT_ERR description revised	86
		COMMAND REGISTER	Added Note regarding commands MNF_CMD 0x5-0x7 in combination with PRES_CONF = 0x3/0x4	98
		DESIGN REVIEW: Notes On Chip Functions	Updated notes on chip functions regarding iC-MNF chip release X1 (item 8 and 9) Updated notes on chip functions regarding iC-MNF chip release X3 (item 1 and 2)	106

[1] Release Date format: *YYYY-MM-DD*

ORDERING INFORMATION

Type	Package	Order Designation
iC-MNF	48-pin QFN 7x7 mm	iC-MNF QFN48-7x7

Please send your purchase orders to our order handling team:

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