iC-JX

16-FOLD 24 V HIGH-SIDE DRIVER WITH µC INTERFACE

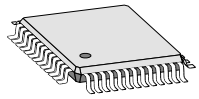
FEATURES

- 16 bidirectional input/output stages at 24 V
- Input/output mode programmable in 4-channel blocks
- Short-circuit-proof high-side drivers with diagnosis function
- 500 mA pulse and 150 mA permanent load driving capability
- Active flyback circuit
- Load diagnosis for driver current, output voltage and impedance (cable break, resistance and short circuits)
- 10-bit A/D converter for the generation of diagnosis measurement values
- Safety devices (voltage monitor, temperature sensor with warning and shutdown features, power output enable pin)
- Programmable interrupt generation with event storage facility
- Variable digital filters for the debouncing of I/O signals
- Fast 8-bit parallel or serial SPI™-compatible µC interface permits SPI bus and daisy chain configuration
- Logic supply from 3 V upwards

APPLICATIONS

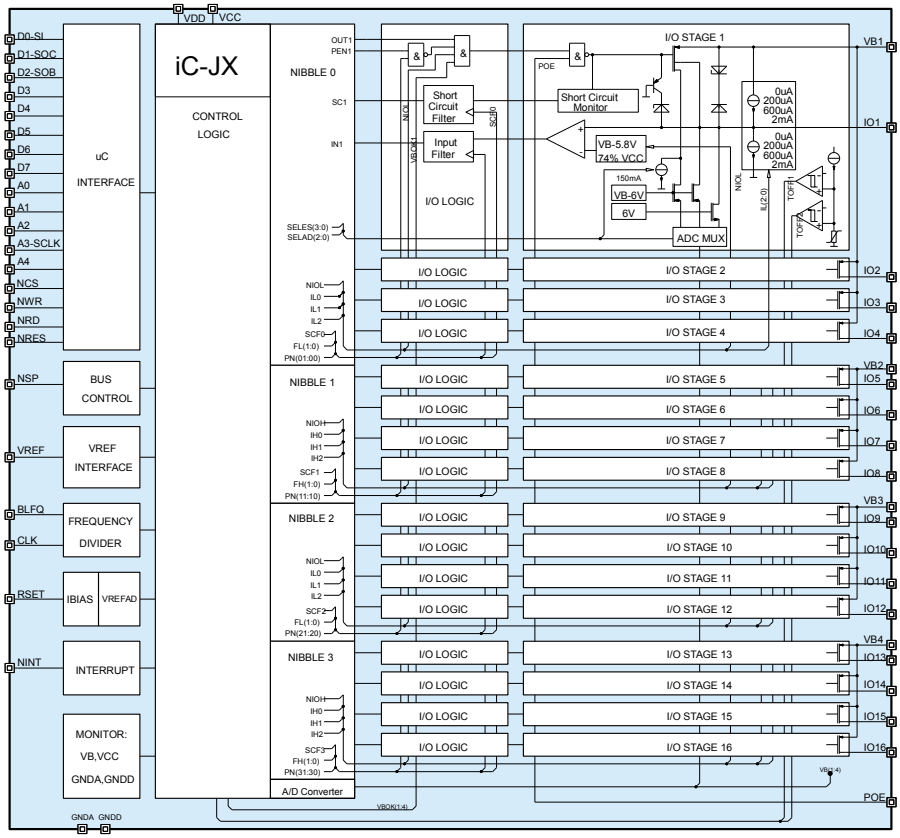
- Industrial 24 V applications
- Lamp switches with diagnostic features
- Inductive load driver circuits for relays and valves etc.

PACKAGES



MQFP52

BLOCK DIAGRAM



DESCRIPTION

iC-JX is a bidirectional I/O device with 4x4 high-side driver stages. The input or output function can be separately selected for blocks or nibbles of four I/O stages.

Each block can also be individually programmed with various filtering options for the debouncing of I/O pin signals or overcurrent messages, with current sources for the defining of levels at the inputs (low-side sources) or for load diagnosis at the outputs (high-side sources) and also with a flash pulse function.

To enable communication with the controller the device includes a parallel interface (with eight data, five address and three control pins) and also an SPI-compatible serial interface (with one pin for the clock, chip selection, data input and data output respectively). The type of interface is selected via pin NSP.

I/O stages with an input function can record logic levels at 24 V where a programmable pull-down/pull-up current source (of up to 2 mA) either defines the level for open inputs or supplies a bias current for external switch contacts. Connecting safety circuits with integrated serial/parallel resistors to the device also enables leakage currents and short circuits to be pinpointed. The contact status can be read out using the microcontroller interface.

I/O stages with an output function drive various loads (such as lamps, cables or relays, for example) to a common ground with 150 mA of permanent current or 500 mA in pulse operation. Spikes and flyback currents are discharged by the integrated flyback circuits.

For synchronous flash display, as used for indicator lamps in plugboards, for example, a flash pulse enable can be individually set for each output to offload the controller. A common inhibiting input (POE) permits the global shut down of all outputs and can be operated by an autonomous watchdog circuit.

All output stages are short-circuit-proof and protected against thermal destruction in the event of extreme power dissipation. Each stage has its own temperature sensor which is evaluated in two stages and generates interrupt messages for the controller. The latter is warned before the device is forcibly shut down. A short circuit also triggers an interrupt message; the current status here can be read out by the controller.

For the purpose of load diagnosis a programmable pull-up current source (of up to 2 mA) can be used to determine an initial load breakage or open loop (caused by a cable break, for example) before an output is switched on. The I/O pin status can always be read back via comparators. A load current measurement circuit then permits the load to be assessed; failed valves and faulty or wrongly implemented indicator lamps can be verified in this way. In addition, the analog measurement of voltage at the I/O pins allows safety switches to be analyzed with reference to ground, here without the driver function.

All analog measurements for the load current (per stage), for the I/O pin voltage (per stage, either referenced to Ground or VB), for the driver supply (all VB pins) , for the internal voltage reference (VBG) and for the chip temperature are made available to the microcontroller as digital measurements by an integrated A/D converter which has 10 bits of resolution.

An interrupt pipeline which limits the loss of interrupts allows reliable processing of interrupts by the microcontroller. Registers provide information as to current events; messages can be individually enabled for all available interrupt sources.

iC-JX monitors all supply voltages and also the GND-D-GNDA connection to ground.

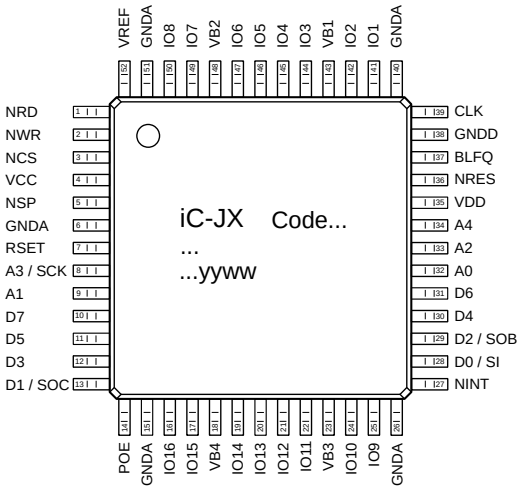
Monitored separately, undervoltage in the range of 2.5V at analog supply VCC or even short disruption of digital supply VDD causes all registers to be reset and the output stages to be shut down.
Undervoltage at 24 V driver supply VB triggers a shutdown of the output stages without deleting the contents of the registers.

Diodes protect all inputs and outputs against destruction by ESD. iC-JX is also immune to burst transients according to IEC 1000-4-4 (4 kV; previously IEC 801-4).

CONTENTS

PACKAGING INFORMATION MQFP52 to JEDEC Standard

PIN CONFIGURATION MQFP52, pitch 0.65 mm



PIN FUNCTIONS

No.	Name	Function
1	NRD	Not Read Enable
2	NWR	Not Write Enable
3	NCS	Not Chip Select
4	VCC	Supply Voltage (analog, 3...5.5 V)
5	NSP	Not Serial / Parallel (Mode)
6	GNDA	Ground (analog)
7	RSET	Resistor Setting (10 kΩ)
8	A3	Address Bus
9	A1	Address Bus
10	D7	Data Bus
11	D5	Data Bus
12	D3	Data Bus
13	D1	Data Bus
14	POE	Power Output Enable
15	GNDA	Ground (analog)
16	IO16	I/O Stage 16
17	IO15	I/O Stage 15
18	VB4	Supply Voltage for I/O Stages 13...16
19	IO14	I/O Stage 14
20	IO13	I/O Stage 13
21	IO12	I/O Stage 12

PIN FUNCTIONS

No.	Name	Function
22	IO11	I/O Stage 11
23	VB3	Supply Voltage for I/O Stages 9...12
24	IO10	I/O Stage 10
25	IO9	I/O Stage 9
26	GNDA	Ground (analog)
27	NINT	Not Interrupt
28	D0	Data Bus
29	D2	Data Bus
30	D4	Data Bus
31	D6	Data Bus
32	A0	Address Bus
33	A2	Address Bus
34	A4	Address Bus
35	VDD	Supply Voltage (logic, 3...5.5 V)
36	NRES	Not Reset
37	BLFQ	Blink Frequency
38	GNDD	Ground (logic)
39	CLK	Clock (optional)
40	GNDA	Ground (analog)
41	IO1	I/O Stage 1
42	IO2	I/O Stage 2
43	VB1	Supply Voltage for I/O Stages 1...4
44	IO3	I/O Stage 3
45	IO4	I/O Stage 4
46	IO5	I/O Stage 5
47	IO6	I/O Stage 6
48	VB2	Supply Voltage for I/O Stages 5...8
49	IO7	I/O Stage 7
50	IO8	I/O Stage 8
51	GNDA	Ground (analog)
52	VREF	External Voltage Reference (optional)
		Additional Pin Function in SPI Mode (NSP = low)
3	NCS	Not Chip Select
8	SCK	Serial Clock
9	A1	Device ID Bit 1
13	SOC	Serial Out Chain
28	SI	Serial In
29	SOB	Serial Out Bus
32	A0	Device ID Bit 0
33	A2	Select Chain / Bus
34	A4	Enable Interrupt Report SOC/SOB

Separate supply voltages at VB1..4 are possible. All GNDA pins must be connected up externally. GNDA must be connected to GNDD externally when just one voltage supply is available. VCC and VDD can be powered either mutually or separately.

Only the Pin 1 mark on the front or backside is determinative for package orientation (P-CODE ➊ JX and other codes are subject to change).

ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed. Absolute Maximum Ratings are no Operating Conditions. Integrated circuits with system interfaces, e.g. via cable accessible pins (I/O pins, line drivers) are per principle endangered by injected interferences, which may compromise the function or durability. The robustness of the devices has to be verified by the user during system development with regards to applying standards and ensured where necessary by additional protective circuitry. By the manufacturer suggested protective circuitry is for information only and given without responsibility and has to be verified within the actual system with respect to actual interferences.
(Legend: x = 1..16, y = 1..4)

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VCC, VDD	Voltage at VCC, VDD		-0.3	6	V
G002	VBy	Voltage at VBy		-0.3	40	V
G003	V(IOx)	Voltages at IO1...16	IOx = off; see additional remark [1]	-10	40	V
G004	Idc(IOx)	Current in IO1...16	see Figure 1	-500	150	mA
G005	Ipk(IOx)	Pulse current in IO1...16	IOx = hi, τ = 2 ms, T $\leq$ 2 s see Figure 2	-1.0		A
G006	Imax()	Current in VCC, VDD		-100	100	mA
G007	Imax(VBy)	Current in VB1...4		-8	8	A
G008	Ic()	Current in NCS, NWR, NRD, A0...4, D0...7, NRES, CLK, BLFQ, POE, NSP, RSET, VREF	D0...7 with input function	-20	20	mA
G009	I()	Current in D0...7, NINT,	D0...7 with output function	-25	25	mA
G010	Ilu()	Pulse current in NCS, NWR, NRD, A0...4, D0...7, NRES, CLK, BLFQ, NINT, NSP, POE, IO1...16, RSET, VREF (latch up test)	Pulse width < 10 µs, all inputs / outputs open	-100	100	mA
G011	Vd()	ESD-voltage, all pins	HBM 100 pF discharged over 1.5 kΩ		2	kV
G012	Vb()	Burst transients at IO1...16	according to IEC 1000-4-4		4	kV
G013	Tj	Chip temperature		-40	150	°C
G014	Ts	Storage temperature		-40	150	°C

[1] If the voltage supplies can not be guaranteed to be present at the time signals appear at the pins IO1..IO16, additional diodes or sufficient current limiting ohmic resistors have to be connected in series to the IO-pins to prevent reverse back biasing of the device.

THERMAL DATA

Operating conditions: VCC = VDD = 3 ... 5.5 V, VBy = 12 ... 36 V, GNDA = GNDD = 0 V, all inputs on defined logic states (high or low)

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Ambient temperature	extended temperature range on request	-40		85	°C
T02	Rthja	Thermal resistance chip/ambient	package mounted on PCB		55		K/W

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating conditions: VCC = VDD = 3 ... 5.5 V, VBy = 12 ... 36 V, GNDA = GNDD = 0 V, RSET = 10 kΩ ±1% . All inputs on defined logic states (high or low), Tj = -40 ... 125 °C unless otherwise stated. Functionality and parameters beyond operating conditions (for example w.r. to independent voltage supplies) are to be verified within the individual application by FMEA methods.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
General							
001	VCC	Permissible Supply Voltage VCC		3		5.5	V
002	I(VCC)	Supply Current in VCC			10	20	mA
003	I(VCC)	Supply Current in VCC	no supply voltage VBy			30	mA
004	VDD	Permissible Supply Voltage VDD		3		5.5	V
005	I(VDD)	Supply Current in VDD (static)	all logic inputs lo = 0 V or hi = VDD		3	6	mA
006	I(VDD)	Supply Current in VDD (dynamic)	continuous reading cycle all 200ns, data word '00' and 'FF' is alternating read, CL(D0... 7) = 200 pF			30	mA
007	I(VDD)	Supply Current in VDD	all logic inputs lo = 0.8V		3		mA
008	I(VDD)	Supply Current in VDD	all logic inputs hi = 2.0V		5		mA
009	VBy	Permissible Supply Voltage VB1...4 (operating range)		12		36	V
010	I(VBy)	Supply Current in VB1...4	POE = hi, IOx = hi, no load		7	20	mA
011	I(VBy)	Supply Current in VB1...4	IOx = off		5	10	mA
012	Vc()lo	ESD Clamp Voltage lo at VCC, VDD, VB1...4, RSET, VREF	I() = -10 mA	-1.4		-0.3	V
013	Vc()hi	ESD Clamp Voltage hi at VCC, VDD	I() = 10 mA	6			V
014	Vc()hi	ESD Clamp Voltage hi at VB1...4	I() = 10 mA	30		55	V
015	Vc()lo	ESD Clamp Voltage lo at IO1...16	I() = 10 mA, IOx = off	-25		-19	V
016	Vc()hi	ESD Clamp Voltage hi at IO1...16	I() = 10 mA	30		55	V
017	Vc()hi	ESD Clamp Voltage hi at NCS, NWR, NRD, A0...4, NRES, CLK, BLFQ, D0...7, NINT, POE, NSP	Vc()hi = V() - VDD, D0...7 as input, I() = 10 mA	0.4		1.5	V
018	Vc()lo	ESD Clamp Voltage lo at NCS, NWR, NRD, A0...4, NRES, CLK, BLFQ, D0...7, NINT, POE, NSP	D0...7 as input, I() = -10 mA	-1.5		-0.4	V
019	Ifl(IOx)	Leakage Current of I/O Pins (x = 1..16) beyond operating conditions of VDD, VCC, VB	VCC = 0 V and VDD = 0 V, VBy = 2..30 V	-0.2			mA
I/O Stages: High-Side Driver IO1...16							
101	Vs()hi	Saturation Voltage hi	Vs()hi = VBy - V(IOx), I(IOx) = -15 mA; see Fig. 1			0.2	V
102	Vs()hi	Saturation Voltage hi	Vs()hi = VBy - V(IOx), I(IOx) = -150 mA; see Fig. 1			0.6	V
103	Vs()hi	Saturation Voltage hi for pulse load	Vs()hi = VBy -V(IOx), I(IOx)= -500 mA, τ = 2 ms, T $\leq$ 2 s; see Fig. 2			2.3	V
104	Isc()hi	Overcurrent Cut-off	V(IOx) = 0 .. VBy - 3 V	-1.6		-0.50	A
105	It()scs	Threshold Current for Overcurrent Message		-1.2		-0.51	A
106	Vc()lo	Free-wheeling Clamp Voltage low	I(IOx) = -150 mA	-18		-12	V
107	SR()hi	Slew Rate hi	CL = 0 ... 100 pF, I(IOx) = -150mA	5		17	V/µs

ELECTRICAL CHARACTERISTICS

Operating conditions: VCC = VDD = 3 ... 5.5 V, VBy = 12 ... 36 V, GNDA = GNDD = 0 V, RSET = 10 kΩ ±1% . All inputs on defined logic states (high or low), Tj = -40 ... 125 °C unless otherwise stated. Functionality and parameters beyond operating conditions (for example w.r. to independent voltage supplies) are to be verified within the individual application by FMEA methods.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
108	SR()lo	Slew Rate lo	CL = 0 ... 100 pF, I(IOx) = -150mA	5		17	V/µs
109	tplh()	Propagation Delay until IOx: lo → hi	V(IOx) > V0(IOx) + 1 V			6	µs
110	tphl()	Propagation Delay until IOx = off	V(IOx) < 80 % (VBy - Vs(IOx)hi)			6	µs
I/O Stages: Current Sources at IO1...16							
201	Ipd()	Pull-down Current Source (200 µA)	V(IOx) = 3 V .. VBy;	160	200	240	µA
202	Ipd()	Pull-down Current Source (600 µA)	V(IOx) = 3 V .. VBy;	510	600	690	µA
203	Ipd()	Pull-down Current Source (2 mA)	V(IOx) = 3 V .. VBy;	1.6	2	2.4	mA
204	Ipu()	Pull-up Current Source (200 µA)	IOx = off, V(IOx) = 0 V .. VBy - 3 V	150	200	250	µA
205	Ipu()	Pull-up Current Source (600 µA)	IOx = off, V(IOx) = 0 V .. VBy - 3 V	510	600	690	µA
206	Ipu()	Pull-up Current Source (2 mA)	IOx = off, V(IOx) = 0 V ..VBy - 3 V	1.6	2	2.4	mA
207	tp()Ion	Turn-on Time Current Source active	I(IOx) > 90 % Ipd(IOx) resp. I(IOx) > 90 %Ipu(IOx)			5	µs
208	tp()Ioff	Turn-off Time Current Source inactive	I(IOx) < 10 % Ipd(IOx) resp. I(IOx) < 10 % Ipu(IOx)			5	µs
209	Ifu()	Leakage Current	IOx with Input Function or Output Function with IOx = off; VBy = 30 V IL2 = IH2 = IL1 = IH1 = IL0 = IH0 = 0, V(IOx) = 0V .. VBy	-50		70	µA
210	Irb()	Leakage Current	Conditions see Item-No. 209; V(IOx) = -10 V .. 0 V, VBy = 30 V	-1.5			mA
211	Irb()	Leakage Current	Conditions see Item-No. 209; only Input Function V(IOx) = VBy ... VBy + 0.3 V			250	µA
212	Irb()	Leakage Current	Conditions see Item-No. 209; only Input Function V(IOx) = VBy + 0.3V ... VBy + 2V			1	mA
213	Irb()	Leakage Current	no supply voltages VBy $V(IO)_{max}$ = 36V			5	mA
I/O Stages: Comparator IO 1..16							
301	Vt()hi	Threshold voltage hi	IOx with input function			82	%VCC
302	Vt()lo	Threshold voltage lo	IOx with input function	66			%VCC
303	Vt()hys	Hysteresis	IOx with input function, Vt()hys = Vt()hi - Vt()lo	100			mV
304	Vt()hi	Threshold voltage hi referenced to VBy	IOx with output function, Vt()hi = VBy - V(IOx)	5.0			V
305	Vt()lo	Threshold voltage lo referenced to VBy	IOx with output function, Vt()lo = VBy - V(IOx)			6.7	V
306	Vt()hys	Hysteresis	IOx with output function, Vt()hys = Vt()lo - Vt()hi	100			mV
307	tp(IOx-Dx)	Propagation Delay Input IOx to Data Output Dx	I/O-Filter inactive			20	µs
Thermal Shutdown							
401	Toff1	Overtemperature threshold level 1: warning		120		145	°C
402	Ton1	Level 1 Release		115		140	°C
403	Thys1	Level 1 Hysteresis	Thys1 = Toff1 - Ton1	2		7	°C
404	Toff2	Overtemperature threshold level 2: shutdown		140		165	°C
405	Ton2	Level 2 Release		120		145	°C
406	Thys2	Level 2 Hysteresis	Thys2 = Toff2 - Ton2	13		35	°C
407	ΔT	Temperature Difference Level 2 to Level 1	ΔT = Toff2 - Toff1	13		35	°C

ELECTRICAL CHARACTERISTICS

Operating conditions: VCC = VDD = 3 ... 5.5 V, VBy = 12 ... 36 V, GNDA = GNDD = 0 V, RSET = 10 kΩ ±1% . All inputs on defined logic states (high or low), Tj = -40 ... 125 °C unless otherwise stated. Functionality and parameters beyond operating conditions (for example w.r. to independent voltage supplies) are to be verified within the individual application by FMEA methods.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Bias and Low Voltage Detection							
501	VCCon, VDDon	Turn-on Threshold VCC, VDD (Power-on release)		2.4	2.6	2.9	V
502	VCCoff, VDDoff	Undervoltage Threshold VCC, VDD (Power-down reset)		2.3	2.5	2.8	V
503	VCChys, VDDhys	Hysteresis	VCChys = VCCon - VCCoff, VDDhys = VDDon - VDDoff	60	100	140	mV
504	tmin()lv	Power Down Time required for low voltage detection	VCC = 0.8 V .. VCCoff, VDD = 0.8 V .. VDDoff	1			µs
505	tpoff	Propagation Delay until Reset after Low Voltage at VCC, VDD				12	µs
A/D-Converter							
701	VR1	ADC - Measurement Range 1	Current and voltage measurement High at IO, SELAD = '0b001' resp. '0b010', EME = 0	VBy - 0.6 V		VBy	V
702	VR2	ADC - Measurement Range 2	Voltage measurement High at IO, SELAD = '0b010', EME = 1	VBy - 5V		VBy	V
703	VR3	ADC - Measurement Range 3	Voltage measurement Low at IO, SELAD = '0b100', EME = 0	0		0.6	V
704	VR4	ADC - Measurement Range 4	Voltage measurement Low at IO SELAD = '0b100'; VB or VBG measurement SELAD = '0b101' or. '0b110', EME = 1	0		5	V
705	VR5	ADC - Measurement Range 5	Total voltage measurement range SELAD = '0b011'	0		VB	V
706	VR6	ADC - Measurement Range 6	Temperature measurement SELAD = '0b111'	-40		125	°C
707	Vbitlo	Bit-Equivalent of voltage	EME = 0, SVREF = 1, SELAD = '0b010', '0b100'		0.66		mV
708	Vbithi	Bit-Equivalent of voltage	EME = 1, SVREF = 1, SELAD = '0b010', '0b100'		5.4		mV
709	Dtemp1	Digital value of temperature measurement 1	SVREF = 0, TEMP = (774-Dtemp1)/TKtemp1 Tj = -40°C Tj = 27°C Tj = 95°C	 826 670 519	 863 712 563	 900 755 608	
710	TKtemp1	Temperature coefficient 1	SVREF = 0	2.16	2.22	2.27	1/°C
711	Dtemp2	Digital value of temperature measurement 2	SVREF = 1, V(VREF) = 2.5V ±0.2% TEMP = (861-Dtemp2)/TKtemp2 Tj = -40°C Tj = 27°C Tj = 95°C	 931 761 585	 957 800 632	 984 839 679	
712	TKtemp2	Temperature coefficient 2	SVREF = 1, V(VREF) = 2.5V ±0.2%	2.26	2.41	2.55	1/°C
713	f_{ICLK}	Internal oscillating frequency		0.9	1.25	1.5	MHz
714	t_{SAR1}	Conversion time SAR-converter 1	Current measurement SELAD = '0b001'		154 / f_{ICLK}		µs
715	t_{SAR2}	Conversion time SAR-converter 2	Voltage measurement Low resp. High; SELAD = '0b010' resp. '0b100'		90 / f_{ICLK}		µs
716	t_{SAR3}	Conversion time SAR-converter 3	Total voltage measurement SELAD = '0b011'; VBy voltage measurement SELAD = '0b101'; VBG voltage measurement SELAD = '0b110'; temperature measurement SELAD = '0b111'		26 / f_{ICLK}		µs
717	$D_{VBG,1}$	Digital value of VBG measurement (external reference)	SELAD = '0b110', SVREF = 1	480	520	560	
718	$D_{VBY,1}$	Digital value of VBy measurement (external reference)	SVREF = 1, V(VBy) = 36 V, SELAD = '0b101'	940	990	1022	
719	$DR_{VBY,1}$	Relative value of VBy measurement (external reference)	SVREF = 1; $DR_{VBY,1} = D_{VBY,1}(V) / D_{VBY,1}$ V(VBy) = 24 V, SELAD = '0b101' V(VBy) = 12 V, SELAD = '0b101'	 64.6 31.3	 66.6 33.3	 68.6 35.2	 % %
720	$D1_{IO,1}$	Digital value using VR1 range (external reference)	SELAD = '0b010', EME = '0b0', SVREF = 1, V(IOx) = V(VBy) – 0.6V	840	900	1022	

ELECTRICAL CHARACTERISTICS

Operating conditions: VCC = VDD = 3 ... 5.5 V, VBy = 12 ... 36 V, GNDA = GNDD = 0 V, RSET = 10 kΩ ±1% . All inputs on defined logic states (high or low), Tj = -40 ... 125 °C unless otherwise stated. Functionality and parameters beyond operating conditions (for example w.r. to independent voltage supplies) are to be verified within the individual application by FMEA methods.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
721	$DR1_{IO,1}$	Digital relative value using VR1 range (external reference)	SELAD = '0b010', EME = '0b0', SVREF = 1; $DR1_{IO,1} = D1_{IO,1}(V) / D1_{IO,1}$; V(IOx) = V(VBy) − 0.3 V V(IOx) = V(VBy) − 0.1 V	 46 12	 49 15	 52 18	 % %
722	$D2_{IO,1}$	Digital value using VR2 range (external reference)	SELAD = '0b010', EME = '0b1', SVREF = 1, V(IOx) = V(VBy) − 5.0 V	870	930	1022	
723	$DR2_{IO,1}$	Digital relative value using VR2 range (external reference)	SELAD = '0b010', EME = '0b1', SVREF = 1; $DR2_{IO,1} = D2_{IO,1}(V) / D2_{IO,1}$; V(IOx) = V(VBy) − 2.5 V V(IOx) = V(VBy) − 0.6 V	 48 9.5	 50 11.5	 52 14	 % %
724	$D3_{IO,1}$	Digital value using VR3 range (external reference)	SELAD = '0b100', EME = '0b0', SVREF = 1, V(IOx) = 0.6 V;	880	940	1022	
725	$DR3_{IO,1}$	Digital relative value using VR3 range (external reference)	SELAD = '0b100', EME = '0b0', SVREF = 1; $DR3_{IO,1} = D3_{IO,1}(V) / D3_{IO,1}$; V(IOx) = 0.3 V V(IOx) = 0.1 V	 48 14.5	 50 16	 52 18.5	 % %
726	$D4_{IO,1}$	Digital value using VR4 range (external reference)	SELAD = '0b100', EME = '0b1', SVREF = 1; V(IOx) = 5.0V	870	930	1022	
727	$DR4_{IO,1}$	Digital relative value using VR4 range (external reference)	SELAD = '0b100', EME = '0b1', SVREF = 1; $DR4_{IO,1} = D4_{IO,1}(V) / D4_{IO,1}$ V(IOx) = 2.5V V(IOx) = 0.6V	 48 9.5	 50 11.5	 52 14	 % %
728	$D5_{IO,1}$	Digital value using VR5 range (external reference)	SELAD = '0b011', SVREF = 1, V(IOx) = 36.0V	930	980	1022	
729	$DR5_{IO,1}$	Digital relative value using VR5 range (external reference)	SELAD = '0b011', SVREF = 1; $DR5_{IO,1} = D5_{IO,1}(V) / D5_{IO,1}$ V(IOx) = 24.0V V(IOx) = 5.0V	 64.6 11.8	 66.6 13.8	 68.6 15.8	 % %
730	$DC_{IO,1}$	Digital value of current measurement (external reference)	SELAD = '0b001',SVREF = 1, I(IOx) = 150mA	700	800	1022	
731	$DRC_{IO,1}$	Relative value of current measurement (external reference)	SELAD = '0b001', SVREF = 1; $DRC_{IO,1} = DC_{IO,1}(I) / DC_{IO,1}$ I(IOx) = 75mA I(IOx) = 15mA	 48 6.2	 51 9.2	 54 12.2	 % %
732	$D_{VBg,0}$	Digital value of VBG measurement (internal reference)	SELAD = '0b110', SVREF = 0	435	460	485	
733	$D_{VBY,0}$	Digital value of VBy measurement (internal reference)	SVREF = 0, V(VBy) = 36V, SELAD = '0b101'	830	880	1022	
734	$DR_{VBY,0}$	Relative value using VBy measurement (internal reference)	SVREF = 0, SELAD = '0b101'; $DR_{VBY,0} = D_{VBY,0}(V) / D_{VBY,0}$ V(VBy) = 24V V(VBy) = 12V	 64.6 31.3	 66.6 33.3	 68.6 35.3	 % %
735	$D1_{IO,0}$	Digital value using VR1 range (internal reference)	SELAD = '0b010', EME = '0b0', SVREF = 0, V(IOx) = V(VBy) - 0.6V	760	820	1022	
736	$DR1_{IO,0}$	Relative value using VR1 range (internal reference)	SELAD = '0b010', EME = '0b0', SVREF = 0; $DR1_{IO,0} = D1_{IO,0}(V) / D1_{IO,0}$ V(IOx) = V(VBy) - 0.3V V(IOx) = V(VBy) - 0.1V	 46 12	 49 15	 52 18	 % %
737	$D2_{IO,0}$	Digital value using VR2 range (internal reference)	SELAD = '0b010', EME = '0b1', SVREF = 0, V(IOx) = V(VBy) - 5.0V	790	840	1022	
738	$DR2_{IO,0}$	Relative value using VR2 range (internal reference)	SELAD = '0b010', EME = '0b1', SVREF = 0; $DR2_{IO,0} = D2_{IO,0}(V) / D2_{IO,0}$ V(IOx) = V(VBy) - 2.5V V(IOx) = V(VBy) - 0.6V	 48 9.5	 50 11.5	 52 14	 % %
739	$D3_{IO,0}$	Digital value using VR3 range (internal reference)	SELAD = '0b100', EME = '0b0', SVREF = 0, V(IOx) = 0.6V	790	840	1022	

ELECTRICAL CHARACTERISTICS

Operating conditions: VCC = VDD = 3 ... 5.5 V, VBy = 12 ... 36 V, GNDA = GNDD = 0 V, RSET = 10 kΩ ±1% . All inputs on defined logic states (high or low), Tj = -40 ... 125 °C unless otherwise stated. Functionality and parameters beyond operating conditions (for example w.r. to independent voltage supplies) are to be verified within the individual application by FMEA methods.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
740	$DR3_{IO,0}$	Relative value using VR3 range (internal reference)	SELAD = '0b100', EME = '0b0', SVREF = 0; $DR3_{IO,0} = D3_{IO,0}(V) / D3_{IO,0}$ V(IOx) = 0.3V V(IOx) = 0.1V	 48 14.5	 50 16	 52 18.5	 % %
741	$D4_{IO,0}$	Digital value using VR4 range (internal reference)	SELAD = '0b100', EME = '0b1', SVREF = 0, V(IOx) = 5.0V	790	840	1022	
742	$DR4_{IO,0}$	Relative value using VR4 range (internal reference)	SELAD = '0b100', EME = '0b1', SVREF = 0; $DR4_{IO,0} = D4_{IO,0}(V) / D4_{IO,0}$ V(IOx) = 2.5V V(IOx) = 0.6V	 48 9.5	 50 11.5	 52 14	 % %
743	$D5_{IO,0}$	Digital value using VR5 range (internal reference)	SELAD = '0b011', SVREF = 0 V(IOx) = 36.0V	810	870	1022	
744	$DR5_{IO,0}$	Relative value using VR5 range (internal reference)	SELAD = '0b011', SVREF = 0; $DR5_{IO,0} = D5_{IO,0}(V) / D5_{IO,0}$ V(IOx) = 24.0V V(IOx) = 5.0V	 64.6 11.8	 66.6 13.8	 68.6 15.8	 % %
745	$DC_{IO,0}$	Digital value of current measurement (internal reference)	SELAD = '0b001', SVREF = 0, I(IOx) = 150mA	720	820	1022	
746	$DRC_{IO,0}$	Relative value of current measurement (internal reference)	SELAD = '0b001', SVREF = 0; $DRC_{IO,0} = DC_{IO,0}(I) / DC_{IO,0}$ I(IOx) = 75mA I(IOx) = 15mA	 48 6.2	 51 9.2	 54 12.2	 % %
747	Vrefad	Internal reference voltage for A/D-Converter	SVREF = 0	2.6	2.75	3.0	V
748	Vref	Optional external reference voltage for A/D-Converter at VREF	SVREF = 1	2.45	2.5	2.55	V
749	Ivref()	Current in VREF	SVREF = 1, SELAD ≥ '0b010'		210	300	uA
Input RSET							
B01	V(RSET)	Voltage at RSET		1.15	1.22	1.30	V
B02	R(RSET)	Range value for RSET		9	10	14	kΩ
Burst-Indication							
C01	VSPon	Input On-Threshold for burst recognition		1.3		2.9	V
C02	VSPoff	Input Off-Threshold for Burst-recognition		1.4		3	V
C03	tpoff	Delay time to Reset after spike at VCC, VDD	Spike duration: 10 ns	2		110	µs
Pin monitoring GNDA, GNDD							
H01	Vt()gnd	Threshold voltage for open circuit detection on pins GNDA, GNDD		35		65	mV
H02	tmin()gnd	Minimum duration for open circuit detection	V(GNDA,GNDD) = 0 V ... Vt()gnd	1			µs
H03	tpoff	Delay time to reset after open circuit detection at GNDA, GNDD				15	µs
Undervoltage detection VBy (y=1..4)							
I01	VByon	Undervoltage message VB1...4 on		10.6	11.2	11.8	V
I02	VByoff	Undervoltage message VB1...4 off		10.0	10.6	11.2	V
I03	VByhys	Hysteresis	VByhys = VByon - VByoff	400			mV
I04	tmin()lv	Minimum duration for Power-Down detection	VBy = 0.8 V ... VByoff	1			µs
I05	tpoff	Delay time for undervoltage message VB1...4				6	µs

ELECTRICAL CHARACTERISTICS

Operating conditions: VCC = VDD = 3 ... 5.5 V, VBy = 12 ... 36 V, GNDA = GNDD = 0 V, RSET = 10 kΩ ±1% . All inputs on defined logic states (high or low), Tj = -40 ... 125 °C unless otherwise stated. Functionality and parameters beyond operating conditions (for example w.r. to independent voltage supplies) are to be verified within the individual application by FMEA methods.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
µC-Interface, I/O-Logic, Frequency divider, Interrupt							
K01	Vt()hi	Threshold voltage High at Schmitt-Trigger-Inputs NCS, NWR, NRD, A0...4, NRES, CLK, BLFQ, D0...7, NSP, POE	D0...7 with input function			2	V
K02	Vt()lo	Threshold voltage Low at Schmitt-Trigger-Inputs NCS, NWR, NRD, A0...4, NRES, CLK, BLFQ, D0...7, NSP, POE	D0...7 with input function	0.8			V
K03	Vt()hys	Schmitt-Trigger-Hysteresis at inputs NCS, NWR, NRD, A0...4, NRES, CLK, BLFQ, D0...7, NSP, POE	Vt()hys = Vt()hi - Vt()lo; D0...7 with input function	150			mV
K04	Vs()hi	Saturation voltage high an NINT, Dx	Vs()hi = VDD - V( ); I( ) = -4 mA			0.8	V
K05	Vs()lo	Saturation voltage low an NINT, Dx	I( ) = 4 mA			0.49	V
K06	Ipd()	Pull Down current sources at A0...4, NRES, CLK, BLFQ, D0...7, POE	V() = 1V .. VDD	2		70	µA
K07	Ipu()	Pull Up current sources at NSP, NCS, NWR, NRD	V() = 0V .. VDD - 1 V	-70		2	µA
K08	tp(POE-IOx)	Delay time output enable: POE to IOx disabled	RL = 240 Ω... 1 kΩ, POE: hi → lo to V(IOx) < 80 % (VBy - Vs(IOx)hi)			6	µs
K09	tw()lo	Permissible pulse width for enable/disable at POE		600			ns
K10	tw()	Permissible burst pulse width at POE				100	ns
K11	tmin()nres	minimum duration for reset at NRES		200			ns
Frequency BLFQ, CLK							
P01	f_{CLK}	frequency at CLK				1.25	MHz
P02	f_{BLFQ}	frequency at BLFQ				10	Hz

CHARACTERISTICS: DIAGRAMS

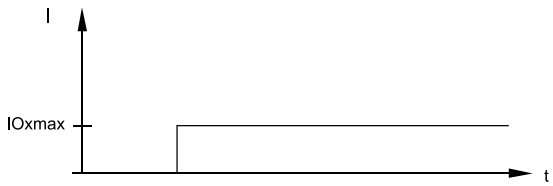


Figure 1: DC load

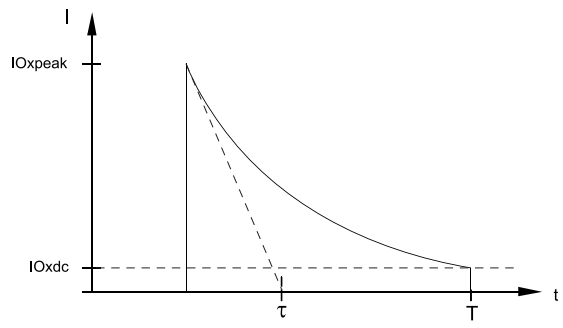


Figure 2: Pulse load

OPERATING REQUIREMENTS: Parallel µC Interface

Operating Conditions: VCC = VDD = 3...5.5 V, VBy = 12...36 V, GNDA = GNDD = 0 V, RSET = 10 kΩ ±1 %
Ta = 0...70 °C, CL() = 150 pF, input level lo = 0.8 V, hi = 2.0 V, reference levels according to figure 3

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
Read Cycle						
I001	t_{AR1}, t_{AR2}	Setup Time: NCS, A0...4 set before NRD hi → lo	see Figure 4	30		ns
I002	t_{RA}	Hold Time: NCS, A0...4 set before NRD lo → hi	see Figure 4	0		ns
I003	t_{RD}	Wait Time : Data valid after NRD hi → lo	see Figure 4		120	ns
I004	t_{DF}	Hold Time: Data Bus high impedance after NRD lo → hi	see Figure 4		65	ns
I005	t_{RL}	Required Read Signal Duration at NRD		50		ns
Write Cycle						
I006	t_{AW1}, t_{AW2}	Setup Time: NCS, A0...4 set before NWR lo → hi	see Figure 4	30		ns
I007	t_{DW}	Setup time : Data valid before NWR lo → hi	see Figure 4	100		ns
I008	t_{WA}	Hold time: NCS, A0...4 stable after NWR lo → hi	see Figure 4	10		ns
I009	t_{WD}	Hold time: Data valid after NWR lo → hi	see Figure 4	10		ns
I010	t_{WL}	Required Write Signal Duration at NWR	see Figure 4	50		ns
Read/Write Timing						
I011	t_{cyc}	Recovery Time between cycles: NRD lo → hi to NRD hi → lo, NRD lo → hi to NWR hi → lo, NWR lo → hi to NWR hi → lo, NWR lo → hi to NRD hi → lo	see Figure 4	165		ns

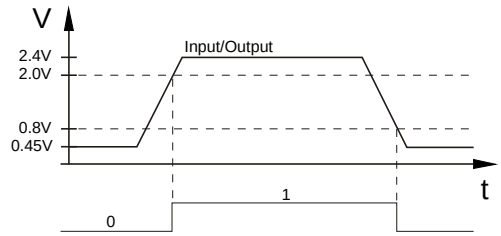


Figure 3: Reference levels for displayed values of time

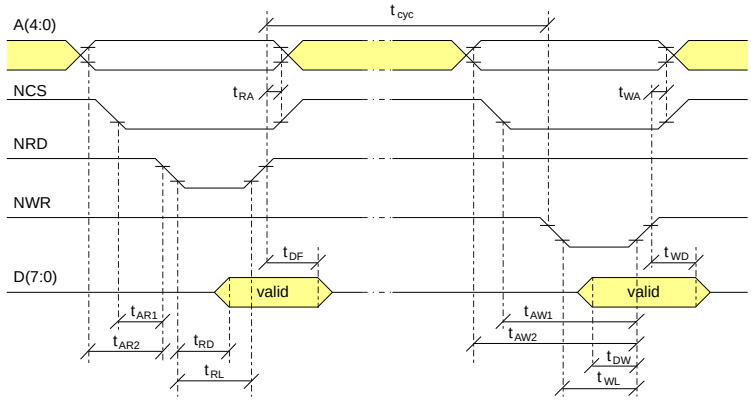


Figure 4: Read and write cycle for the parallel interface

OPERATING REQUIREMENTS: Serial µC Interface (SPI)

Operating Conditions: VCC = VDD = 3...5.5 V, VBy = 12...36 V, GNDA = GNDD = 0 V, RSET = 10 kΩ ±1 %
Ta = 0...70 °C, CL() = 150 pF, input level lo = 0.8 V, hi = 2.0 V, reference levels according to figure 3

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
I101	t_{sCCL}	Setup time: NCS hi → lo to SCK(A3) lo → hi	see Figure 5	50		ns
I102	t_{sDCL}	Setup time: SI(D0) stable before SCK(A3) lo → hi	see Figure 5	40		ns
I103	t_{hDCL}	Hold time: SI(D0) stable after SCK(A3) lo → hi	see Figure 5	30		ns
I104	t_{CLh}	Clock duration SCK(A3) hi	see Figure 5	165		ns
I105	t_{CLl}	Clock duration SCK(A3) lo	see Figure 5	165		ns
I106	t_{CSh}	Pulse duration NCS hi	see Figure 5	100		ns
I107	t_{pCLD}	Delay time: SOC(D1) resp. SOB(D2) stable after SCK(A3) hi → lo	see Figure 5	0	145	ns
I108	t_{pCSD}	Delay time: SOC(D1) resp. SOB(D2) high impedance after NCS lo → hi	see Figure 5	0	145	ns

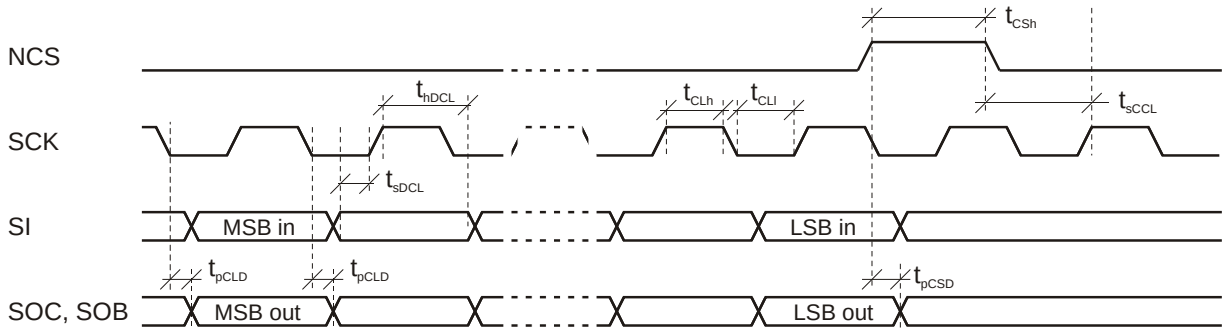


Figure 5: µC interface in SPI mode

CONFIGURATION PARAMETERS

REGISTER OVERVIEW

General programming register overview. Detailed description of the programming bits can be found in the chapter REGISTER DETAILS. A detailed description of the chip functions can be found in the chapter DESCRIPTION OF FUNCTIONS. For a description of the I/O interfaces and its protocols please refer to chapter I/O INTERFACES.

Register Overview							
Address							
A(4...0)	A4	A3	A2	A1	A0	**Write**	**Read**
0x00	0	0	0	0	0	-	Input Register A[1,2]
0x01	0	0	0	0	1	-	Input Register B[1,2]
0x02	0	0	0	1	0	-	Change-of-input Message A[1,3]
0x03	0	0	0	1	1	-	Change-of-input Message B[1,3]
0x04	0	0	1	0	0	-	Interrupt Status Register A
0x05	0	0	1	0	1	-	Interrupt Status Register B
0x06	0	0	1	1	0	-	Overcurrent Message A[1,4]
0x07	0	0	1	1	1	-	Overcurrent Message B[1,4]
0x08	0	1	0	0	0	-	Overcurrent Status A[1]
0x09	0	1	0	0	1	-	Overcurrent Status B[1]
0x0A	0	1	0	1	0	-	A/D-Converter Data 1
0x0B	0	1	0	1	1	-	A/D-Converter Data 2
0x0C	0	1	1	0	0	Output Register A[1]	
0x0D	0	1	1	0	1	Output Register B[1]	
0x0E	0	1	1	1	0	Flash Pulse Enable A[1]	
0x0F	0	1	1	1	1	Flash Pulse Enable B[1]	
0x10	1	0	0	0	0	Change-of-input Interrupt Enable A[1,5]	
0x11	1	0	0	0	1	Change-of-input Interrupt Enable B[1,5]	
0x12	1	0	0	1	0	Overcurrent Interrupt Enable A[1]	
0x13	1	0	0	1	1	Overcurrent Interrupt Enable B[1]	
0x14	1	0	1	0	0	Control Word 1A (I/O filters)[1]	
0x15	1	0	1	0	1	Control Word 1B (I/O filters)[1]	
0x16	1	0	1	1	0	Control Word 2A (I/O pin functions)[1]	
0x17	1	0	1	1	1	Control Word 2B (I/O pin functions)[1]	
0x18	1	1	0	0	0	Control Word 3A (flash pulse settings)[1]	
0x19	1	1	0	0	1	Control Word 3B (reference clock)[1]	
0x1A	1	1	0	1	0	Control Word 4 (Overcurrent message filter settings)	
0x1B	1	1	0	1	1	Control Word 5 (I/O Stage selection for AD Converter)	
0x1C	1	1	1	0	0	Control Word 6 (ADC settings)	
0x1D	1	1	1	0	1	-	Interconnection Error, Device-ID
0x1E	1	1	1	1	0	Test Register 1	
0x1F	1	1	1	1	1	Test Register 2	
Notes:	[1] A: I/O-Stages 1...8, B: I/O-Stages 9...16 [2] Reads the inputs or reads back the outputs, depending on I/O pin mode [3] For I/O pins in input mode (register is '0' in output mode) [4] For I/O pins in output mode (register is '0' in input mode) [5] Only writable in input mode						

Table 1: Register assignment

REGISTER DETAILS

The register contents and configuration possibilities are described in this chapter. A detailed description of the chip functions can be found in the chapter DESCRIPTION OF FUNCTIONS. The order of the register description is:

1. Configuration of the chip functions (I/O pins, filters, ADC, Output)
2. Status messages (general and those enabled for interrupt)
3. Interrupt configuration and interrupt messages
4. Interconnection Error and Device ID

General remark regarding the following register tables:
'-' is used for spare storage space with no function; '0' after reset.
(r) is used to mark the reset entry.

Control Word 1: I/O filters

Control Word 1A (I/O filters)								**Addr. 0x14**
								reset entry: 0x00
	Nibble 1: I/O-Pins 5..8				**Nibble 0: I/O-Pins 1..4**			
Bit	7	6	5	4	3	2	1	0
Name	BYP1	-	FH1	FH0	BYP0	-	FL1	FL0

Control Word 1A: Nibble 1					
Bit7 BYP1	0 1	I/O filters active Bypass for I/O filters: the I/O signals are reprocessed in their unfiltered state.			(r)
Bit5..4 FH1..0		FH1	FH0	Filter time[1]	
		0	0	$(14.5 \pm 1) * \frac{1}{f(SECLK)}$ ≈ 11.6 ± 0.8 us[a]	(r)
		0	1	$(896.5 \pm 64) * \frac{1}{f(SECLK)}$ ≈ 717.2 ± 51.2 us[a]	
		1	0	$(3584.5 \pm 256) * \frac{1}{f(SECLK)}$ ≈ 2867.6 ± 204.8 us[a]	
		1	1	$(7168.5 \pm 512) * \frac{1}{f(SECLK)}$ ≈ 5734.8 ± 409.6 us[a]	

Control Word 1A: Nibble 0					
Bit3 BYP0	0 1	I/O filter active Bypass for I/O filters: the I/O signals are reprocessed in their unfiltered state.			(r)
Bit1..0 FL1..0		FL1	FL0	Filter time[1]	
		0	0	$(14.5 \pm 1) * \frac{1}{f(SECLK)}$	(r)
		0	1	$(896.5 \pm 64) * \frac{1}{f(SECLK)}$	
		1	0	$(3584.5 \pm 256) * \frac{1}{f(SECLK)}$	
		1	1	$(7168.5 \pm 512) * \frac{1}{f(SECLK)}$	

[1] SECLK: see Control Word 3B on page 20
[a] Filter times derived from system clock configured with f(SECLK[1]) @ 1.25MHz

Control Word 1B (I/O filters)								**Addr. 0x15**
								reset entry: 0x00
	Nibble 3: I/O-Pins 13..16				**Nibble 2: I/O-Pins 9..12**			
Bit	7	6	5	4	3	2	1	0
Name	BYP3	-	FH1	FH0	BYP2	-	FL1	FL0

Control Word 1B: Nibble 3					
Bit7	0	I/O filters active			(r)
BYP1	1	Bypass for I/O filters: the I/O signals are reprocessed in their unfiltered state.			
Bit5..4		FH1	FH0	Filter time[1]	
FH1..0		0	0	$(14.5 \pm 1) * \frac{1}{f(SECLK)}$ $\approx 11.6 \pm 0.8$ us[a]	(r)
		0	1	$(896.5 \pm 64) * \frac{1}{f(SECLK)}$ $\approx 717.2 \pm 51.2$ us[a]	
		1	0	$(3584.5 \pm 256) * \frac{1}{f(SECLK)}$ $\approx 2867.6 \pm 204.8$ us[a]	
		1	1	$(7168.5 \pm 512) * \frac{1}{f(SECLK)}$ $\approx 5734.8 \pm 409.6$ us[a]	

Control Word 1B: Nibble 2					
Bit3	0	I/O filters active			(r)
BYP0	1	Bypass for I/O filters: the I/O signals are reprocessed in their unfiltered state.			
Bit1..0		FL1	FL0	Filter time[1]	
FL1..0		0	0	$(14.5 \pm 1) * \frac{1}{f(SECLK)}$	(r)
		0	1	$(896.5 \pm 64) * \frac{1}{f(SECLK)}$	
		1	0	$(3584.5 \pm 256) * \frac{1}{f(SECLK)}$	
		1	1	$(7168.5 \pm 512) * \frac{1}{f(SECLK)}$	

[1] SECLK: see Control Word 3B on page 20
[a] Filter times derived from system clock configured with f(SECLK[1]) @ 1.25MHz

Control Word 2: I/O pin functions

Control Word 2A (I/O pin functions)								**Addr. 0x16**
								reset entry: 0x11
	Nibble 1: I/O-Pins 5..8				**Nibble 0: I/O-Pins 1..4**			
Bit	7	6	5	4	3	2	1	0
Name	NIOH	IH2	IH1	IH0	NIOL	IL2	IL1	IL0

Control Word 2A: Nibble 1						
Bit7	0	Input mode				(r)
NIOH	1	Output mode				
Bit6..4		IH2	IH1	IH0	Current sources	
IH2..0		0	0	0	disabled	
		0	0	1	200µA Pull-Down	(r)
		0	1	0	600µA Pull-Down	
		0	1	1	2mA Pull-Down	
		1	0	0	disabled	
		1	0	1	200µA Pull-Up	
		1	1	0	600µA Pull-Up	
		1	1	1	2mA Pull-Up	

Control Word 2A: Nibble 0						
Bit3	0	Input mode				(r)
NIOL	1	Output mode				
Bit2..0		IL2	IL1	IL0	Current sources	
IL2..0		0	0	0	disabled	
		0	0	1	200µA Pull-Down	(r)
		0	1	0	600µA Pull-Down	
		0	1	1	2mA Pull-Down	
		1	0	0	disabled	
		1	0	1	200µA Pull-Up	
		1	1	0	600µA Pull-Up	
		1	1	1	2mA Pull-Up	

Control Word 2B (I/O-pin function)								**Addr. 0x17**
								reset entry: 0x11
	Nibble 3: I/O-Pins 13..16				**Nibble 2: I/O-Pins 9..12**			
Bit	7	6	5	4	3	2	1	0
Name	NIOH	IH2	IH1	IH0	NIOL	IL2	IL1	IL0

Control Word 2B: Nibble 3						
Bit7	0	Input mode				(r)
NIOH	1	Output mode				
Bit6..4		IH2	IH1	IH0	Current sources	
IH2..0		0	0	0	disabled	
		0	0	1	200µA Pull-Down	(r)
		0	1	0	600µA Pull-Down	
		0	1	1	2mA Pull-Down	
		1	0	0	disabled	
		1	0	1	200µA Pull-Up	
		1	1	0	600µA Pull-Up	
		1	1	1	2mA Pull-Up	

Control Word 2B: Nibble 2						
Bit3	0	Input mode				(r)
NIOL	1	Output mode				
Bit2..0		IL2	IL1	IL0	Current sources	
IL2..0		0	0	0	disabled	
		0	0	1	200µA Pull-Down	(r)
		0	1	0	600µA Pull-Down	
		0	1	1	2mA Pull-Down	
		1	0	0	disabled	
		1	0	1	200µA Pull-Up	
		1	1	0	600µA Pull-Up	
		1	1	1	2mA Pull-Up	

Control Word 3: flash pulse and reference clock

Control Word 3A (flash pulse settings)								**Addr. 0x18**
								Reset-state : 0x00
	Nibble 3: I/O-Pins 13..16		**Nibble 2: I/O-Pins 9..12**		**Nibble 1: I/O-Pins 5..8**		**Nibble 0: I/O-Pins 1..4**	
Bit	7	6	5	4	3	2	1	0
Name	PN31	PN30	PN21	PN20	PN11	PN10	PN01	PN00

Control Word 3A: Nibble 0-3					
Nibble3, Bit7..6 Nibble2, Bit5..4 Nibble1, Bit3..2 Nibble0, Bit1..0	PN31 PN21 PN11 PN01	PN30 PN20 PN10 PN00	Flash frequency SEBLQ[1] = 0	Flash frequency SEBLQ[1] = 1	
	0	0	f(BLFQ)	f(SECLK)/2^{19} ≈ 2.38 Hz[a]	(r)
	0	1	f(BLFQ)/2	f(SECLK)/2^{20} ≈ 1.19 Hz[a]	
	1	0	f(BLFQ)/4	f(SECLK)/2^{21} ≈ 596 mHz[a]	
	1	1	f(BLFQ)/16	f(SECLK)/2^{23} ≈ 149 mHz[a]	

[1] SEBLQ: see Control Word 3B
[a] Flash frequency derived from system clock configured with f(SECLK[1]) @ 1.25MHz

Control Word 3B (reference clock)								**Addr. 0x19**
								reset entry: 0x00
Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	SECLK1	SECLK0	-	SEBLQ

Bit0	SEBLQ	Settings for flash frequency	
SEBLQ	0	The flashing pulse is derived from the external clock signal at BLFQ	(r)
	1	The flashing pulse is derived from the system clock SECLK	

Bit3..2	SECLK1	SECLK0	Settings for system clock SECLK	
SECLK1..0	0	0	Operation with the clock signal at CLK	(r)
	0	1	Operation with the internal clock signal ICLK (see Elec. Charac. 713)	
	1	0	Operation without the clock signal at CLK (filtering etc. deactivated)	
	1	1	reserved	

Control Word 4: filter for overcurrent message

Control Word 4 (Overcurrent message filter settings)								**Addr. 0x1A**
								reset entry : 0x00
					Nibble3	**Nibble2**	**Nibble1**	**Nibble0**
Bit	7	6	5	4	3	2	1	0
Name	EOI	-	-	BYPSCF	SCF3	SCF2	SCF1	SCF0

Bit7	EOI	Interrupt acknowledge (change-of-input, overcurrent message)	(r)
EOI	0	No effect	(r)
	1	"DELETE"s the interrupt message (change-of-input message; interrupt status register, overcurrent message) accepts successive interrupts from the pipeline, deletes the messages at NINT resp. D1/SOC or D2/SOB when the pipeline is empty. Bit automatically resets to '0'.	

Bit4	BYPSCF	Bypass overcurrent filter	(r)
BYPSCF	0	Filters for the overcurrent message are active	(r)
	1	Bypass for the filters: overcurrent messages are reprocessed in their unfiltered state.	

	SCFx	Filter time[1] overcurrent message	
Bit3		**Nibble 3**	
SCF3	0	$(2689.5 \pm 192) * \frac{1}{f(SECLK)} \approx 2.15 \pm 0.15$ ms[a]	(r)
	1	$(5378.5 \pm 384) * \frac{1}{f(SECLK)} \approx 4.3 \pm 0.3$ ms[a]	
Bit2		**Nibble 2**	
SCF2	0	$(2689.5 \pm 192) * \frac{1}{f(SECLK)} \approx 2.15 \pm 0.15$ ms[a]	(r)
	1	$(5378.5 \pm 384) * \frac{1}{f(SECLK)} \approx 4.3 \pm 0.3$ ms[a]	
Bit1		**Nibble 1**	
SCF1	0	$(2689.5 \pm 192) * \frac{1}{f(SECLK)} \approx 2.15 \pm 0.15$ ms[a]	(r)
	1	$(5378.5 \pm 384) * \frac{1}{f(SECLK)} \approx 4.3 \pm 0.3$ ms[a]	
Bit1		**Nibble 0**	
SCF0	0	$(2689.5 \pm 192) * \frac{1}{f(SECLK)} \approx 2.15 \pm 0.15$ ms[a]	(r)
	1	$(5378.5 \pm 384) * \frac{1}{f(SECLK)} \approx 4.3 \pm 0.3$ ms[a]	

[1] SECLK: see Control Word 3B on page 20
[a] Filter times derived from system clock configured with f(SECLK[1]) @ 1.25MHz

Control Word 5: I/O stage select for ADC-measurements

Control Word 5 (I/O Stage selection for AD Converter)								**Addr. 0x1B**
								reset entry : 0x00
Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	SELES3	SELES2	SELES1	SELES0

Bit3..0	SELES3	SELES2	SELES1	SELES0	Selection of I/O stage	
SELES3..0	0	0	0	0	I/O stage 1	(r)
	0	0	0	1	I/O stage 2	
	0	0	1	0	I/O stage 3	
	0	0	1	1	I/O stage 4	
	0	1	0	0	I/O stage 5	
	0	1	0	1	I/O stage 6	
	0	1	1	0	I/O stage 7	
	0	1	1	1	I/O stage 8	
	1	0	0	0	I/O stage 9	
	1	0	0	1	I/O stage 10	
	1	0	1	0	I/O stage 11	
	1	0	1	1	I/O stage 12	
	1	1	0	0	I/O stage 13	
	1	1	0	1	I/O stage 14	
	1	1	1	0	I/O stage 15	
	1	1	1	1	I/O stage 16	

Control Word 6: ADC settings

Control Word 6 (ADC settings)								**Addr. 0x1C**
								reset entry : 0x00
Bit	7	6	5	4	3	2	1	0
Name	-	-	SVREF	EW	EME	SELAD2	SELAD1	SELAD0

Bit2..0 SELAD2..0	SELAD2	SELAD1	SELAD0	Settings for ADC measurements	
	0	0	0	A/D-Converter disabled	(r)
	0	0	1	Current measurement IO[1]	
	0	1	0	Voltage measurement high at IO[1]	
	0	1	1	Overall voltage measurement range at IO[1]	
	1	0	0	Voltage measurement low at IO [1]	
	1	0	1	VBy voltage measurement (y:1..4)[2]	
	1	1	0	VBG voltage measurement	
	1	1	1	Temperature measurement	
Bit3 EME	0	Measurement range extension "OFF" (for voltages up to 0.6V)			(r)
	1	Measurement range extension "ON" (for voltages up to 5V) For voltage measurements with SELAD = 0x2 and 0x4, the range extension can be either "ON" or "OFF".			
Bit4 EW	0	A/D converter "OFF"			(r)
	1	Start A/D conversion Bit automatically resets to ’0’ after conversion is completed.			
Bit5 SVREF	0	Internal reference voltage V(Vrefad) is used by ADC (see Elec. Char. 747)			(r)
	1	External reference voltage at Pin VREF is used by ADC			

[1] The corresponding I/O stage is selected via SELES(3:0) of Control Word 5 (P. 22).
[2] VBy (y=1..4) is selected via SELES(3:0) of Control Word 5 :
- VB1 measurements apply to SELES(3:0) = 0x0...0x3,
- VB2 measurements apply to SELES(3:0) = 0x4...0x7,
- VB3 measurements apply to SELES(3:0) = 0x8...0xB and
- VB4 measurements apply to SELES(3:0) = 0xC...0xF.

Output configuration: high side driver

For I/O stages with output function: OUTx switches the high-side driver for IOx.

Output-Register A for I/O stages with output function								**Addr. 0x0C**
								reset entry: 0x00
Bit	7	6	5	4	3	2	1	0
Name	OUT8	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1

Bit7...0	0	High-side driver "OFF"	(r)
OUT8...1	1	High-side driver "ON", i.e. normally, IOx = 1	

Output-Register B for I/O stages with output function								**Addr. 0x0D**
								reset entry: 0x00
Bit	7	6	5	4	3	2	1	0
Name	OUT16	OUT15	OUT14	OUT13	OUT12	OUT11	OUT10	OUT9

Bit7...0	0	High-side driver "OFF"	(r)
OUT16...9	1	High-side driver "ON", i.e. normally, IOx = 1	

Output configuration: flash pulse enable

For I/O stages with output function: PENx enables the flash pulse for IOx. For the flash pulse to be visible at the output also OUTx has to be enabled.

Flash Pulse Enable A for I/O stages with output function								**Addr. 0x0E**
								reset entry: 0x00
Bit	7	6	5	4	3	2	1	0
Name	PEN8	PEN7	PEN6	PEN5	PEN4	PEN3	PEN2	PEN1

Bit7...0	0	Flash pulse "DISABLED"	(r)
PEN8...1	1	Flash pulse "ENABLED"	

Flash Pulse Enable B for I/O stages with output function								**Addr. 0x0F**
								reset entry: 0x00
Bit	7	6	5	4	3	2	1	0
Name	PEN16	PEN15	PEN14	PEN13	PEN12	PEN11	PEN10	PEN9

Bit7...0	0	Flash pulse "DISABLED"	(r)
PEN16...9	1	Flash pulse "ENABLED"	

Pin Status: logic level change (interrupt)

A read access to one of the registers Interrupt Status Register A/B, Overcurrent Message A/B or Change-of-input Message A/B while an interrupt message is active (DCHI, ISCI, IET1, IET2, IEOC, ISD, IUSD or IUSA) locks all of these registers against further changes: the registers are re-enabled only when reset via EOI (see P. 21). Any interrupt such as a successive logic level change interrupt message which occurs during the read-out phase and before a reset with EOI is trapped by an interrupt pipeline. If this happens, the message at NINT resp. D1/SOC or D2/SOB cannot be deleted by EOI, i.e. NINT remains low resp. D1/SOC or D2/SOB constantly remain on high. In this instance, EOI fills the overcurrent message from the pipeline.

If enabled with IENx (see P. 28) the following registers are used to indicate a state change at input IOx.
The DCHx bits may be erased selectable by re-enabling IENx after disable.

Change-of-input Message A (read only) for I/O stages in input mode								**Addr. 0x02** reset entry: 0x00
Bit	7	6	5	4	3	2	1	0
Name	DCH8	DCH7	DCH6	DCH5	DCH4	DCH3	DCH2	DCH1

Bit7...0 DCH8...1	0 1	No change of state at the input IOx or no interrupt enable Input IOx has had a change of state enabled for interrupt messages	(r)

Change-of-input Message B (read only) for I/O stages in input mode								**Addr. 0x03** reset entry: 0x00
Bit	7	6	5	4	3	2	1	0
Name	DCH16	DCH15	DCH14	DCH13	DCH12	DCH11	DCH10	DCH9

Bit7...0 DCH16...9	0 1	No change of state at the input IOx or no interrupt enable Input IOx has had a change of state enabled for interrupt messages	(r)

Pin Status: logic level (status)

INx indicates the state for IOx (via I/O filter or bypass) and does not generate any interrupts.

Input Register A (read only) reading of inputs / output feedback								**Addr. 0x00** reset entry: 0x00
Bit	7	6	5	4	3	2	1	0
Name	IN8	IN7	IN6	IN5	IN4	IN3	IN2	IN1

Bit7...0 IN8...1	0 1	Input/Output IOx read '0' Input/Output IOx read '1'	(r)

Input Register B (read only) reading of inputs / output feedback								**Addr. 0x01** reset entry: 0x00
Bit	7	6	5	4	3	2	1	0
Name	IN16	IN15	IN14	IN13	IN12	IN11	IN10	IN9

Bit7...0 IN16...9	0 1	Input/Output IOx read '0' Input/Output IOx read '1'	(r)

Pin Status: overcurrent (interrupt)

A read access to one of the registers Interrupt Status Register A/B, Overcurrent Message A/B or Change-of-input Message A/B while an interrupt message is active (DCHI, ISCI, IET1, IET2, IEOC, ISD, IUSD or IUSA) locks all of these registers against further changes: the registers are re-enabled only when reset via EOI (see P. 21). Any interrupt such as a successive overcurrent interrupt message which occurs during the read-out phase and before a reset with EOI is trapped by an interrupt pipeline. If this happens, the message at NINT resp. D1/SOC or D2/SOB cannot be deleted by EOI, i.e. NINT remains low resp. D1/SOC or D2/SOB constantly remain on high. In this instance, EOI fills the overcurrent message from the pipeline.

If enabled with SCENx (see P. 28) the following registers are used to indicate an overcurrent state at output IOx. For IOx pins in input mode '0' is output. SCIx reports for IOx.
The SCIx bits may be erased selectable by re-enabling SCENx after disable.

Overcurrent Message A (read only)								**Addr. 0x06**
								reset entry: 0x00
Bit	7	6	5	4	3	2	1	0
Name	SCI8	SCI7	SCI6	SCI5	SCI4	SCI3	SCI2	SCI1

Bit7...0	0	No Message	(r)
SCI8...1	1	Output IOx has had an overcurrent state enabled for interrupt messages (short circuit)	

Overcurrent Message B (read only)								**Addr. 0x07**
								reset entry: 0x00
Bit	7	6	5	4	3	2	1	0
Name	SCI16	SCI15	SCI14	SCI13	SCI12	SCI11	SCI10	SCI9

Bit7...0	0	No Message	(r)
SCI16...9	1	Output IOx has had an overcurrent state enabled for interrupt messages (short circuit)	

Pin Status: overcurrent (status)

Overcurrent Status A and B can be used for error analysis and do not generate any interrupts (real time, no register). '0' is output for IOx pins in input mode. SCx reports for IOx.

Overcurrent Status A (read only)								**Addr. 0x08**
								reset entry : 0x00
Bit	7	6	5	4	3	2	1	0
Name	SC8	SC7	SC6	SC5	SC4	SC3	SC2	SC1

Bit7...0	0	No overcurrent	(r)
SC8...1	1	Overcurrent in output IOx, e.g. through a low-side short circuit	

Overcurrent Status B (read only)								**Addr. 0x09**
								reset entry: 0x00
Bit	7	6	5	4	3	2	1	0
Name	SC16	SC15	SC14	SC13	SC12	SC11	SC10	SC9

Bit7...0	0	No overcurrent	(r)
SC16...9	1	Overcurrent in output IOx, e.g. through a low-side short circuit	

A/D converter data

Digitized result of the analog measurement for load current, I/O voltage, driver supply, internal voltage reference or temperature measurement. The type of A/D conversion as well as the reference voltages are configured with Control Word 6 (P. 23).

A/D-Converter Data 1 (read only)								**Addr. 0x0A**
								reset entry: 0x00
Bit	7	6	5	4	3	2	1	0
Name	D9	D8	D7	D6	D5	D4	D3	D2

Bit7...0	0	Bit value is 0	(r)
D9...2	1	Bit value equals $FACTOR_{ADC}$ * 2^n, with n = 9..2	

A/D-Converter Data 2 (read only)								**Addr. 0x0B**
								reset entry: 0x00
Bit	7	6	5	4	3	2	1	0
Name	D1	D0	-	-	-	-	-	-

Bit7...0	0	Bit value is 0	(r)
D1...0	1	Bit value equals $FACTOR_{ADC}$ * 2^n, with n = 1..0	

[a] $FACTOR_{ADC}$ see P. 35

Interrupt Enable: input change

IENx enables the input IOx for interrupt. The outputs IOx can not be enabled for interrupt. The registers can only be modified in input mode.

Change-of-input Interrupt Enable A for I/O stages with input function								**Addr. 0x10**
								reset entry: 0x00
Bit	7	6	5	4	3	2	1	0
Name	IEN8	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1

Bit7...0 IEN8...1	0 1	"DISABLED" for interrupt "ENABLED" for interrupt: A hi → lo or lo → hi change of state at the input IOx triggers an interrupt.	(r)

Change-of-input Interrupt Enable B for I/O stages with input function								**Addr. 0x11**
								reset entry: 0x00
Bit	7	6	5	4	3	2	1	0
Name	IEN16	IEN15	IEN14	IEN13	IEN12	IEN11	IEN10	IEN9

Bit7...0 IEN16...9	0 1	"DISABLED" for interrupt "ENABLED" for interrupt: A hi → lo or lo → hi change of state at the input IOx triggers an interrupt.	(r)

Interrupt Enable: overcurrent

SCENx enables the output IOx for overcurrent interrupt.

Overcurrent Interrupt Enable A								**Addr. 0x12**
								reset entry: 0x00
Bit	7	6	5	4	3	2	1	0
Name	SCEN8	SCEN7	SCEN6	SCEN5	SCEN4	SCEN3	SCEN2	SCEN1

Bit7...0 SCEN8...1	0 1	"DISABLED" for interrupt "ENABLED" for interrupt: a short-circuit at IOx triggers an interrupt.	(r)

Overcurrent Interrupt Enable B								**Addr. 0x13**
								reset entry: 0x00
Bit	7	6	5	4	3	2	1	0
Name	SCEN16	SCEN15	SCEN14	SCEN13	SCEN12	SCEN11	SCEN10	SCEN9

Bit7...0 SCEN16...9	0 1	"DISABLED" for interrupt "ENABLED" for interrupt: a short-circuit at IOx triggers an interrupt.	(r)

Interrupt Messages

A read access to one of the registers Interrupt Status Register A/B, Over Current Message A/B or Input Change Message A/B while an interrupt message is active (DCHI, ISCI, IET1, IET2, IEOC, ISD, IUSD or IUSA) locks all of these registers against further changes: the registers are re-enabled only when reset via EOI (see P. 21). Any successive interrupts which occur at DCHI, IET2, IET1, ISCI, IEOC, ISD, IUSD and IUSA during the read-out phase and before a reset with EOI are trapped by an interrupt pipeline. If this happens, the message at NINT resp. D1/SOC or D2/SOB cannot be deleted by EOI, i.e. NINT remains low resp. D1/SOC or D2/SOB constantly remain high. In this instance, EOI fills the overcurrent message from the pipeline.

Interrupt Status Register A (read only)								**Addr. 0x04**
								reset entry: 0x00
Bit	7	6	5	4	3	2	1	0
Name	DCHI	IET2	IET1	ISCI	-	ET2	ET1	SCS

Interrupts: Change-of-input data, Overtemperature, overcurrent			
Bit7	0	No message	(r)
DCHI	1	Interrupt through change-of input message	
Bit6	0	No message	(r)
IET2	1	Interrupt through excessive temperature level 2	
Bit5	0	No message	(r)
IET1	1	Interrupt through excessive temperature level 1	
Bit4	0	No message	(r)
ISCI	1	Interrupt through overcurrent message	

Real time signals: Excessive temperature status, overcurrent status			
Bit2	0	No error message	(r)
ET2	1	Excessive temperature level 2 (shutdown)	
Bit1	0	No error message	(r)
ET1	1	Excessive temperature level 1 (warning)	
Bit0	0	No error message	(r)
SCS	1	Overcurrent status (e.g. caused by low-side short circuit)	

Interrupt Status Register B (read only)								**Addr. 0x05**
								reset entry: 0x00
Bit	7	6	5	4	3	2	1	0
Name	IEOC	ISD	IUSD	IUSA	-	EOC	USD	USA

Interrupts: A/D-Converter, Bursts, Undervoltage			
Bit7	0	No message	(r)
IEOC	1	Interrupt by the A/D-Converter	
Bit6	0	No message	(r)
ISD	1	Interrupt caused by bursts at VDD	
Bit5	0	No message	(r)
IUSD	1	Interrupt caused by undervoltage at VDD	
Bit4	0	No message	(r)
IUSA	1	Interrupt caused by undervoltage at VCC	

Real time signals: A/D-Converter, Undervoltage			
Bit2	0	No message	(r)
EOC	1	A/D conversion completed (End of Conversion)	
Bit1	0	No message	(r)
USD	1	Undervoltage at VDD	
Bit0	0	No message	(r)
USA	1	Undervoltage at VCC	

Interconnection Error, Device ID

Interconnection Error, Device Identification (read only)								**Addr. 0x1D**
								reset entry : 0x15
Bit Name	7 IBA	6 USVB	5 NRESA	4 DID4	3 DID3	2 DID2	1 DID1	0 DID0

Interconnection Error			
Bit7 IBA	0 1	No message Interconnection error, broken bond wire at GNDA or GNDD	(r)
Bit6 USVB	0 1	No message Undervoltage at VB4, VB3, VB2 or VB1	(r)
Bit5 NRESA	0 1	No message NRES is 0	(r)

Device ID			
Bit4..0 DID4..0		Device ID for iC-JX: 0b10101	(r)

DESCRIPTION OF FUNCTIONS

Overview I/O configuration

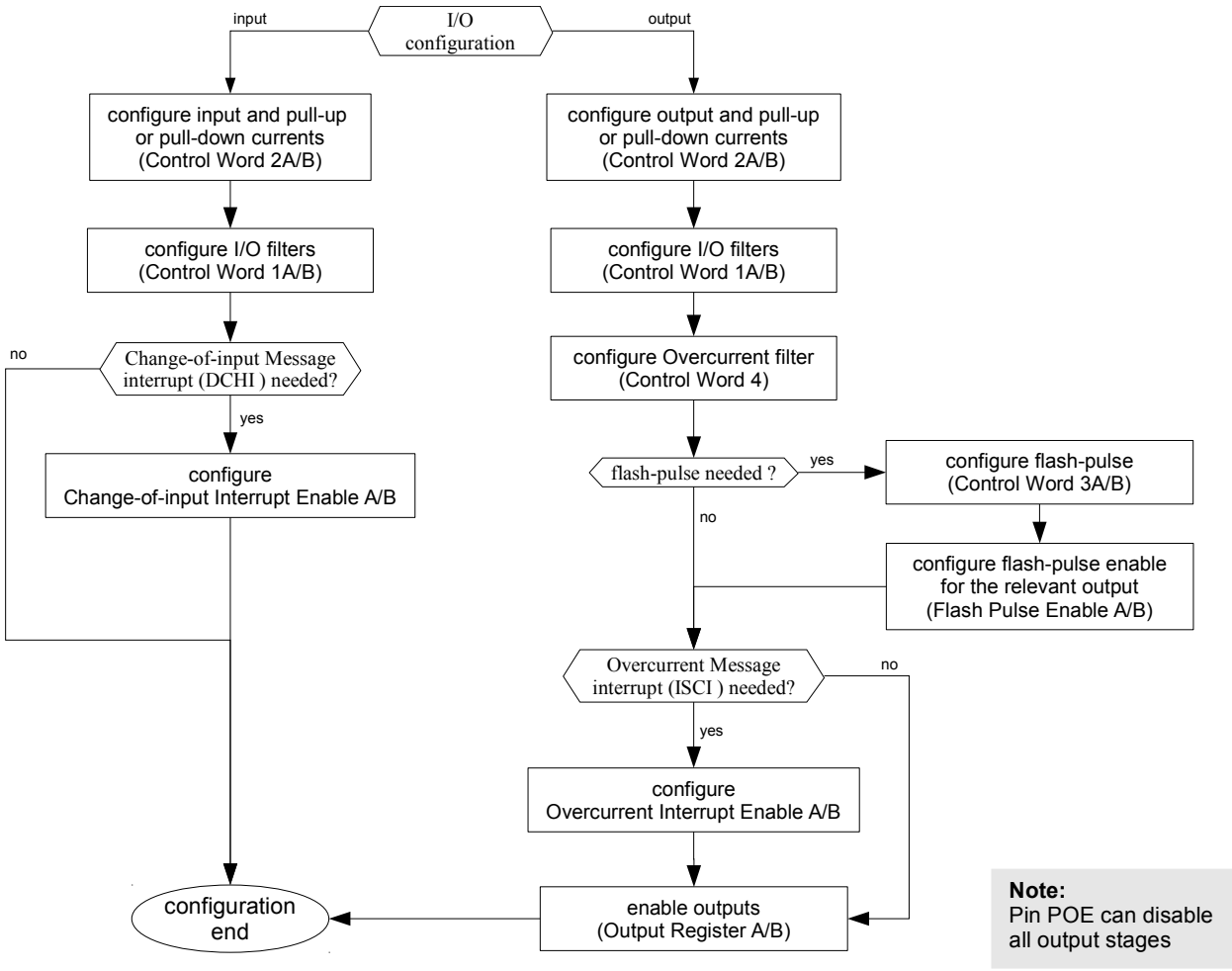


Figure 6: Configuration of a block of four I/O stages

I/O configuration

iC-JX is a bidirectional I/O device with 4x4 high-side driver stages. The input or output function can be separately selected for blocks or nibbles of four I/O stages with Control Word 2 (Addr. 0x16 and 0x17, P. 18).

Each block can also be individually programmed with various filtering options for the debouncing of I/O pin signals (Control Word 1, Addr. 0x14 and 0x15, P. 16) or overcurrent messages (Control Word 4, Addr. 0x1A, P. 21).

I/O stages		
Nibble	Pins	Supply Voltage
0	IO1..4	VB1
1	IO5..8	VB2
2	IO9..12	VB3
3	IO13..16	VB4

Table 2: I/O stage nibbles and corresponding pins/supply voltages

Programmable current sources

The programmable pull-up- resp. pull-down current sources can be set independently of the I/O mode (either input or output mode). In both modes current values of 200 µA, 600 µA or 2 mA are available either as pull-up or pull down. Configuration is done with Control Word 2 (Addr. 0x16 and 0x17, P. 18 f.).

Note:
If the temperature rises above Toff2 the pull-up/down current sources are shut down and are reactivated only if the temperature falls below Ton2 (see P. 37).

Enable outputs

The I/O stages configured as output (Control Word 2 (Addr. 0x16 and 0x17, P. 18) can be enabled individually with Output-Register A/B (Addr. 0x0C, 0x0D, P. 24).

Notes:
Pin POE can disable all output stages (see Tab. 3, P. 32).
If the temperature rises above Toff2 the Output-Registers A/B are reset to disable the output transistors of the I/O stages and thus to minimize power dissipation (see P. 37).

Forced shutdown of output stages

All output stages can be forcibly shut down at input POE (see Tab. 3). This function allows a processor-independent watchdog to lock the outputs in the event of error, for example. An integrated pull-down resistor increases safety.

Forced shutdown of output stages	
Pin POE	output stages
0	disabled
1	enabled (according to Output Register A/B)

Table 3: Forced shutdown of output stages with pin POE

Flash pulse settings

The output stages can be individually set to flash mode with the registers Flash Pulse Enable A/B (Addr. 0x0E, 0x0F, P. 24). The blink or flash frequency can be derived from pin BLFQ or from system clock (SEBLQ: Control Word 3B, Addr. 0x19, P. 20). Note that also the system clock can be applied externally to pin CLK or be generated internally (SECLK: Control Word 3B, Addr. 0x19, P. 20). Different flash frequencies can be set for all four nibbles (Control Word 3A, Addr. 0x18, P.20).

Notes:
The corresponding output has to be enabled in the Output Register (Addr. 0x0C, 0x0D, P. 24) for the flash function to be visible at the output.
If the temperature rises above Toff2 the Flash Pulse Enable A/B registers are reset (see P. 37).

Pin RSET

To set the reference current needed by iC-JX an external resistor of 10 kΩ must be connected from RSET to ground.

External reset

A reset (NRES = 0) sets the register entries to the reset values given in the tables (see chapter REGISTER DETAILS).

Device identification

An identification code has been introduced to enable identification of iC-JX.

DID(4:0)	Addr. 0x1D; bit 4:0
Code	Device ID
0x15	iC-JX

Table 4: Device ID iC-JX

Operation without the external CLK signal

iC-JX can be operated without an external clock at pin CLK. Using Control Word 3B (Addr. 0x19, P. 20) the device can be set to an internally generated clock frequency; In this instance all filter functions remain fully available.

Via SECLK in Control Word 3B the clocked filtering for the I/O signals and overcurrent messaging can also be deactivated. The same behavior can be obtained by setting BYP0, BYP1, BYP2 and BYP3 in Control Word 1 (Addr. 0x14 and 0x15, see P. 16) together with BYPSCF in Control Word 4 (Addr. 0x1A, see P. 21); all filters are avoided by way of a bypass circuit.

Note:
When the filtering of the I/O messages and the overcurrent messages is deactivated with SECLK or BYPO..3 interferences in the line can lead to the unwanted display of interrupts.

ADC measurements

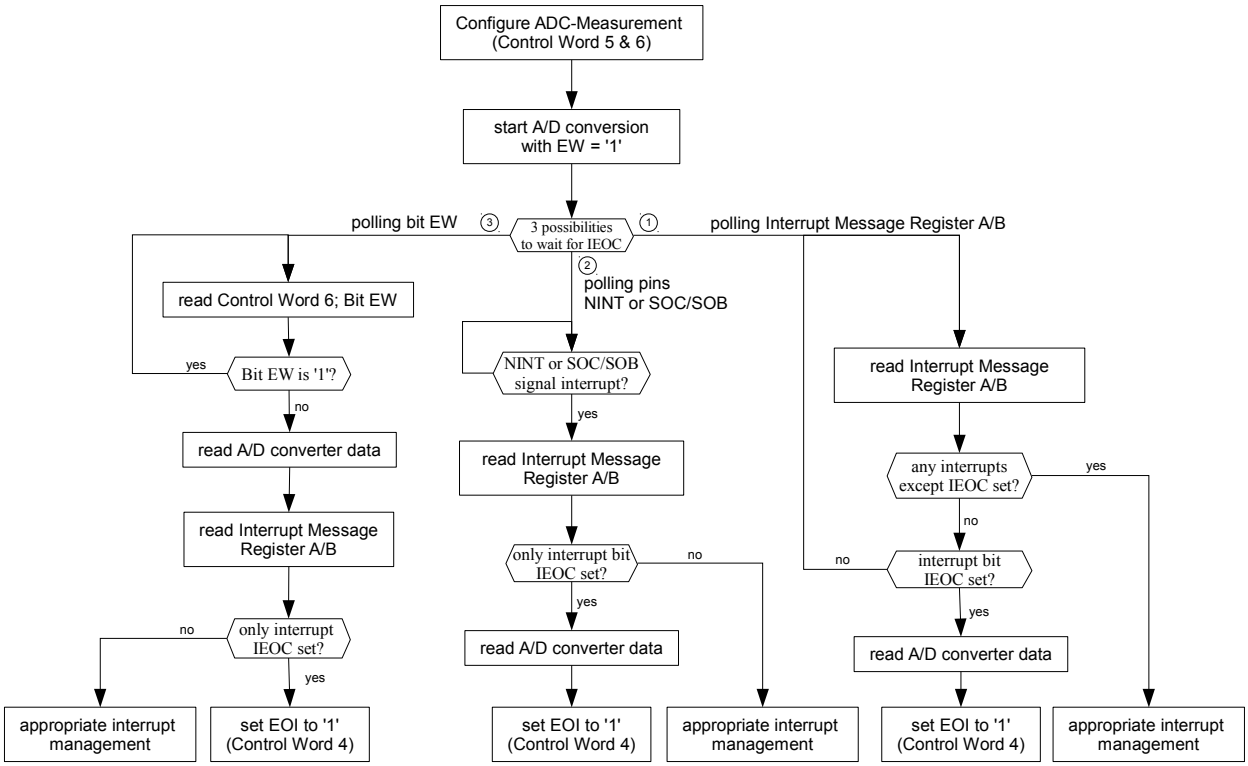


Figure 7: ADC measurement

In the following the various ADC measurement features are described which can be configured using Control Word 6 (Addr. 0x1C, P. 23). An A/D conversion is started by setting bit EW to 1. The end of A/D conversion is reported via EOC resp. IEOC (Interrupt Status Register, Addr. 0x05, P. 29), by a low signal '0' at NINT resp. '1' at D1/SOC or D2/SOB. The result of the conversion is stored as a 10 bit digital value in the registers A/D converter data (see P. 35).

ADC measurements: measuring current

With SELAD = 0x1 the current in each output stage can be measured. The output stage is selected via SELES in Control Word 5 (Addr. 0x1B, P. 22).

The saturation voltage from an internal reference transistor is used for comparison. Each output stage has its own reference transistor in order to guarantee a precise value. The reference voltage is equivalent to the saturation voltage of the output stage transistor with a nominal current of 150 mA; the output digital value thus corresponds to the current intensity in the output stage.

To evaluate current variations in the output stage the controller must perform an initial measurement with a known reference current. Based on this value a monitoring of the load current can then be performed; e.g. failed valves and faulty or wrongly implemented indicator lamps connected to IOx can be verified in this way.

ADC measurements: measuring voltage

The iC-JX measures voltages at the I/O stages in different ranges summarized in Tab. 5

SELAD[1] = 0x2: Voltage measurement high at IO	
EME	Voltage range
0	VR1 = (VBy – 0.6 V) to VBy
1	VR2 = (VBy – 5 V) to VBy
SELAD = 0x4: Voltage measurement low at IO	
EME	Voltage range
0	VR3 = 0 to 0.6 V
1	VR4 = 0 to 5 V
SELAD = 0x3: Overall voltage measurement range at IO	
EME	Voltage range
-	VR5[2]
Notes	[1] Control Word 6, Addr. 0x1C [2] voltage of selected I/O stage 1/15 downscaled VBy = VB1..4 VR1..VR5 please refer to Fig. 8

Table 5: ADC measurement: voltage ranges

The selection of the I/O stage is done via Control Word 5 (Addr. 0x1B, P. 22).

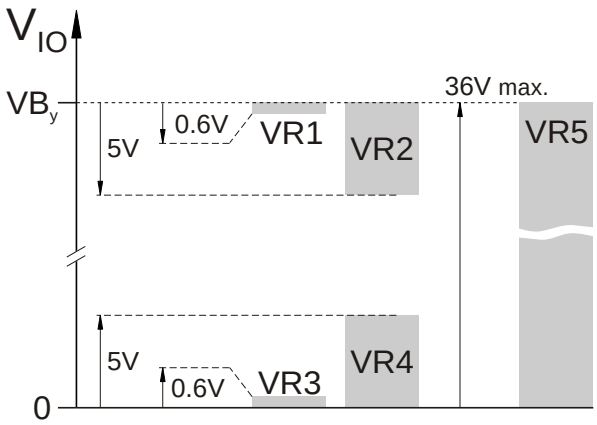


Figure 8: ADC measurement ranges

Note:
For the mode **Overall voltage measurement range at IO** the voltage at the selected I/O stage is downscaled first by a factor of 1/15 using a resistive voltage divider to permit measurement of the full voltage range from rail to rail. The user must be aware of a input current drawn by the voltage divider of approximately V(IO)/200kΩ.

ADC Measurements: VB1..4 and VBG Measurements
The internal reference voltage VBG (SELAD = 0x6) and the external supply voltages VB1 to VB4 (SELAD = 0x5) can also be measured. For VB1 to VB4, the voltage is downscaled first by a factor of 1/15. Selection is done via SELES in Control Word 5 (Addr. 0x1B, P. 22) see Tab. 6.

SELES(3:0)	Addr. 0x1B; bit 3:0
Code	selected supply voltage VB1...VB4
0x0...0x3	VB1
0x4...0x7	VB2
0x8...0xB	VB3
0xC...0xF	VB4

Table 6: ADC measurement: VB1..4 selection

ADC Measurements: Temperature Measurement
With SELAD = 0x7 the internal chip temperature can be determined.

ADC Measurements: Using external VREF
To improve accuracy of the A/D conversion, an external reference voltage at pin VREF can be used by setting the bit SVREF = 1 (see Control Word 6, P. 23). The value of the external voltage reference should be about 2.5V ±0.2%.

SVREF	Addr. 0x1C; bit 5
Code	Reference Voltage
0	V(Vrefad) = 2.75V[1]
1	V(VREF) = 2.5V ±0.2%
Note	[1] Elec. Char. 747

Table 7: Using external VREF

A/D converter data

A 10 bit digital value as a result of A/D conversion is available for output currents and output voltages at a selected I/O stage, for chip temperature and supply voltages VB1..4 and the internal bandgap voltage VBG. Except for the current measurement, the internal voltage V(Vrefad) or an external voltage at pin VREF are used as reference. The reference source is configured using SVREF.

D(9:2) Addr. 0x0A; bit 7:0 **D(1:0)** Addr. 0x0B; bit 7:6	
Code	RESULT
0x000 ... 0xFFF	D(9:0) * $FACTOR_{ADC}$

Table 8: A/D converter data: calculation of ADC result voltage and current measurements

For the the digital representation of the measured voltages and currents please refer to Tab. 9 and 10, for the measured temperature refer to Tab. 11.

SVREF = 0, V(Vrefad) = 2.75V (Elec. Char. 747)	
SELAD[1] = 0x1: Current measurement IO	
EME	$FACTOR_{ADC}$
-	$182.92*10^{-3}$ mA
SELAD = 0x2: Voltage measurement high at IO	
EME	$FACTOR_{ADC}$
0	0.726 mV
1	5,94 mV
SELAD = 0x3: Overall voltage measurement range at IO	
EME	$FACTOR_{ADC}$
-	40.32 mV
SELAD = 0x4: Voltage measurement low at IO	
EME	$FACTOR_{ADC}$
0	0.726 mV
1	5,94 mV
SELAD = 0x5: VB1..4 voltage measurement	
EME	$FACTOR_{ADC}$
-	40.32 mV
SELAD = 0x6: VBG voltage measurement	
EME	$FACTOR_{ADC}$
-	2,688 mV
Notes	[1] Control Word 6, Addr. 0x1C The values are guide values, a reference measurement is recommended. Please take into account Elec. Char. 732- 746.

Table 9: A/D converter data: Voltage/Current Measurements, SVREF = 0

SVREF = 1, V(VREF) = 2.5V ±0.2%	
SELAD[1] = 0x1: Current measurement IO	
EME	$FACTOR_{ADC}$
-	$187.5*10^{-3}$ mA
SELAD = 0x2: Voltage measurement high at IO	
EME	$FACTOR_{ADC}$
0	0.66 mV
1	5.4 mV
SELAD = 0x3: Overall voltage measurement range at IO	
EME	$FACTOR_{ADC}$
-	36,65 mV
SELAD = 0x4: Voltage measurement low at IO	
EME	$FACTOR_{ADC}$
0	0.66 mV
1	5.4 mV
SELAD = 0x5: VB1..4 voltage measurement	
EME	$FACTOR_{ADC}$
-	36,65 mV
SELAD = 0x6: VBG voltage measurement	
EME	$FACTOR_{ADC}$
-	2,443 mV
Notes	[1] Control Word 6, Addr. 0x1C The values are guide values, a reference measurement is recommended. Please take into account Elec. Char. 717- 731.

Table 10: A/D converter data: Voltage/Current Measurements, SVREF = 1

D(9:2) Addr. 0x0A; bit 7:0 **D(1:0)** Addr. 0x0B; bit 7:6	
SVREF = 0, V(Vrefad) = 2.75V (Elec. Char. 747)	
Code	Temperature
563	95°C
...	(774-D(9:0))/2.22[a]
863	-40°C
SVREF = 1, V(VREF) = 2.5V ±0.2%	
Code	Temperature
632	95°C
...	(861-D(9:0))/2.41[b]
957	-40°C
Note	see Elec. char. [a]710, [b]712

Table 11: A/D converter data: Temperature Measurement (SELAD = 0x7)

Interrupts

Interrupt readings at NINT resp. D1/SOC or D2/SOB can be triggered:

- by a change of (filtered) input signal
- by an overcurrent message signaled at an I/O pin (due to a short circuit, for example)
- by undervoltage at VCC or VDD
- by bursts at VDD
- by the end of an A/D conversion
- by exceeding maximum temperature thresholds (2 stages)

Interrupt outputs for each individual I/O stage can be caused:

- by a change of input
- by a short circuit (with stages in output mode)

The relevant interrupt enables determine which messages are stored and which are displayed (Addr. 0x10-0x13, see P. 28).

Note:
The display of interrupt messages caused by excessive temperature, A/D conversion, undervoltage or bursts is not maskable; this particular function is permanently enabled.

When an event occurs which is enabled to produce an interrupt message pin NINT is set to 0. If the device is being operated with a serial interface outputs D1/SOC or D2/SOB are set to 1 when an interrupt occurs if no communication is made via the interface itself and the interrupt messaging is enabled with pin A4 (see Tab. 15, P. 42).

By reading out the Interrupt Status Register (Addr. 0x04 and 0x05, P. 29) the nature of the message can be determined. In case of a change-of-input interrupt or an overcurrent interrupt the I/O stage causing the interrupt can be located. With a change-of-input message the problematic I/O stage is shown in the corresponding Change-of-input Message register (Addr. 0x02 and 0x03, P. 25); with an overcurrent interrupt the Overcurrent Message register (Addr. 0x06 and 0x07, P. 26) pinpoints the I/O stage with a short circuit.

Interrupts are deleted by setting EOI in Control Word 4 (Addr. 0x1A, P. 21). This bit then automatically resets to 0.

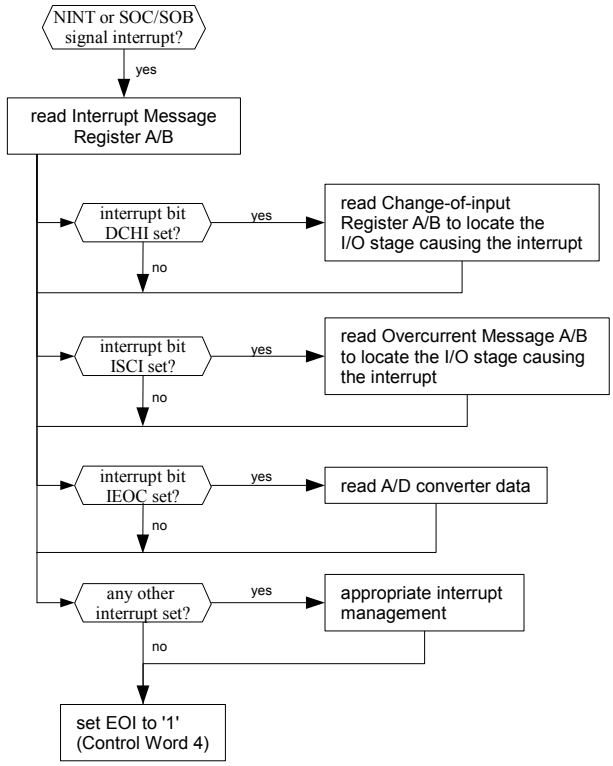


Figure 9: Interrupt management

Note:
To avoid interrupt messages caused by other sources in the time between the readout of a interrupt status register (Interrupt Status Register, Change-of-input Message or Overcurrent Message) and the deletion of the current interrupt being overlooked all interrupt status registers are locked against further changes and successive interrupts are stored in a pipeline. If successive interrupts occur outputs NINT remains at '0' resp. D1/SOC or D2/SOB remain at '1' after the present interrupt has been deleted using EOI. The new interrupt source is displayed in the interrupt status register and in the specific status registers.

I/O stages configured as input: logic level status and Change-of-input Message

Any change to an input signal IOx is accepted via digital filtering only after the selected filter time has expired. The scaling factor for the filter times and the input filter bypass can be programmed separately for all four nibbles (see Control Word 1, Addr. 0x14 and 0x15, P. 16). The clock source for all filters can be programmed with SECLK (see Control Word 3B, Addr. 0x19, P. 20).

Input Registers A/B (Addr. 0x00 and 0x01, P. 25) represent the actual status of the I/O stages. A high at IOx

generates a '1' at bit INx in the Input Register A/B. A low at IOx generates a '0' at bit INx.

Once the Change-of-input Message has been enabled in the Change-of-input Interrupt Enable register (Addr. 0x10 and 0x11, P. 28) a change of level at one of the I/O pins is signaled to the microcontroller. Interrupt pin NINT is set to 0. If the device is operated at the serial interface a change of level is also indicated by a 1 at pin D1/SOC or D2/SOB, depending upon configuration (see SPI interface, Tab. 15, P. 42). The microcontroller can determine which I/O stage has had a change of input by reading out the Change-of-input Message Register A/B (Addr. 0x02 and 0x03, P. 25).

Note:
If during operation an I/O nibble is switched from input to output mode, all Change-of-input Messages of the corresponding I/O nibble are deleted.

I/O stages configured as output: monitor logic level status
As with the reading of inputs the feedback signals of outputs can be output in their filtered or unfiltered state. The microcontroller can determine the actual status of the I/O stages by reading out Input Register A/B (Addr. 0x00 and 0x01, P. 25). A high at IOx generates a '1' at bit INx in the Input Register A/B. A low at IOx generates a '0' at bit INx.

This allows the microcontroller to make a direct check of the switching state and, with the help of the programmable high-side current sources of 200 µA, 600 µA and 2 mA, to monitor the channel for any cable break before an output is switched on with the Output Register (P. 24).

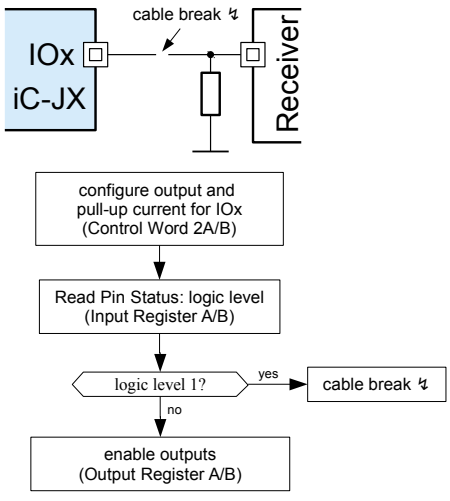


Figure 10: Monitor cable break

Overcurrent messages
If an overload occurs at one of the outputs the current in IOx is limited. In this instance an interrupt message is triggered, providing relevant interrupt enables have been set for overcurrent messages (Addr. 0x12 and 0x13, P. 28) and the filter time set with Control Word 4 (Addr. 0x1A, P. 21) has elapsed. ISCI is then set in the Interrupt Status Register (Addr. 0x04, P. 29) and the relevant bit for the I/O stage causing the problem is set in the Overcurrent Message register (Addr. 0x06 and 0x07, P. 26). Filtering of the overcurrent message can be shut down using a bypass; this bypass can be activated for all I/O stages together using BYPSCF in Control Word 4 (Addr. 0x1A, P. 21).

At addresses 0x08 and 0x09 (see P. 26) the actual, unfiltered overcurrent status of each I/O stage can be read; a global scan of all I/O stages is also possible via bit SCS in the Interrupt Status Register. This shows whether any of the I/O stages have overcurrent at the time of the readout. This short-circuit messaging allows permanent monitoring of the output transistors and clear allocation of error message to affected I/O stages.

Temperature monitoring
iC-JX has a two-stage temperature monitor circuit (see Fig 11).

Stage 1: A warning interrupt IET1 is generated if the first temperature threshold (Toff1 at approx. 132 °C) is exceeded. Suitable measures to decrease the power dissipation of the driver can be implemented using the microcontroller.

Stage 2: If the second temperature threshold is exceeded (Toff2 at approx. 152 °C), a second interrupt IET2 is generated. At the same time the I/O stage pull-up and pull-down current sources are disabled and the registers Output-Register A/B and Flash Pulse Enable A/B are reset to disable the output transistors. Once the temperature has returned to below the level of Ton2 (approx. 132 °C) the pull-up and pull-down current sources are reactivated. Output-Register A/B and Flash Pulse Enable A/B have to be configured anew to reactivate the output stages

Status bits ET1 and ET2 statically indicate when Toff1 and Toff2 are exceeded. Interrupt messages IET1 and IET2 as well as the status bits ET1 and ET2 can be read at Interrupt Status Register A (Addr. 0x04, P. 29).

Stored interrupt message IET1 and IET2 and the display at NINT resp. D1/SOC or D2/SOB can be deleted by setting EOI to 1 in Control Word 4 (Addr. 0x1A, P. 21).

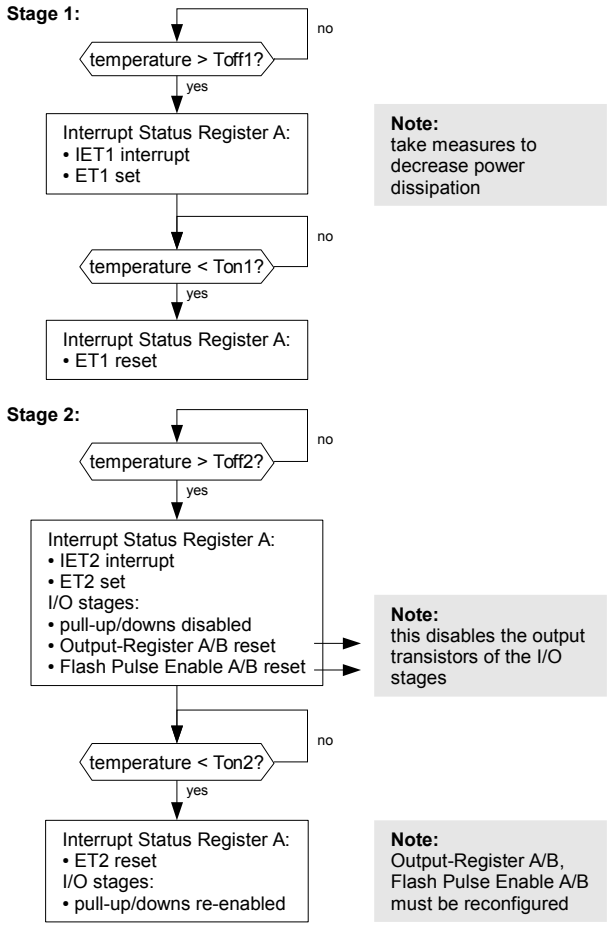


Figure 11: Two-stage temperature monitor circuit (for Toff1/2, Ton1/2 refer to Elec. Char.)

Undervoltage detection: VCC and VDD

When the supply voltage at VCC or VDD is switched on the output transistors of IO1..16 configured as outputs are only enabled by the undervoltage detector after power-on enables VCCon or VDDon (see Elec. Char. 501) have been reached.

Should the supply voltage drop below VCCoff or VDDoff (see Elec. Char. 502) during operation, interrupt bits IUSA (for VCC) or IUSD (for VDD) are set in Interrupt Status Register B (Addr. 0x05, P. 29). The I/O stages are disabled, i.e. the output transistors are turned off. All registers and the Interrupt Status Register A/B except the interrupt bits IUSA, IUSD and ISD are reset. Statusbits USD and USA statically indicate undervoltage at VDD and VCC.

Stored interrupt messages IUSD and IUSA and the display at NINT resp. D1/SOC or D2/SOB can be deleted by setting EOI to 1 in Control Word 4 (Addr. 0x1A, P. 21).

Note:
Should the supply voltage at VCC or VDD rise to VCCon or VDDon after undervoltage detection, all registers of iC-JX except the interrupt bits IUSA, IUSD and ISD in Interrupt Status Register B have been reset.

Undervoltage detection: VB1...4

In order to guarantee the fail-safe operation of connected loads voltages VB1..4 are also monitored.

If one of the voltages VBy (y=1..4) drops below threshold VByoff (see Elec. Char. I02) the output transistors of the corresponding I/O Nibble are disabled. Once voltage VBy again rises above VByon (see Elec. Char. I01) the output transistors of the corresponding I/O Nibble are re-enabled.

Note that neither a device reset nor an interrupt message to the microcontroller are then triggered. The microcontroller can read out the status of the voltages VB1..4 at bit USVB in the Device ID register (Addr. 0x1D, P. 30). In the event of error (one of the voltages VB1..4 < VByoff) this bit is set to 1.

Pin monitoring GNDD and GNDA

iC-JX includes a pin watchdog circuit which monitors the connection between the two ground pins GNDA and GNDD. The microcontroller can detect a possible error, such as a disconnected IC lead, for example, by reading bit IBA in the Interconnection Error register (Addr. 0x1D, P. 30). In the event of error IBA is set to 1.

Note:
If such a case of an error is present (disconnected IC lead), then the potential of the missing ground pin is raised, which can lead to a shift of the trigger levels.

Burst detection at VDD

As in principle bursts at VDD can influence the contents of registers iC-JX monitors spikes in the supply. If any hazard is detected Bit ISD is set to 1 in the Interrupt Status Register B (Addr. 0x05, P. 29). The I/O stages are disabled, i.e. the output transistors are turned off. All registers and the Interrupt Status Register A/B except the interrupt bits IUSA, IUSD and ISD are reset.

Stored interrupt message ISD and the display at NINT resp. D1/SOC or D2/SOB can be deleted by setting EOI to 1 in Control Word 4 (Addr. 0x1A, P. 21).

Note:
After burst detection at VDD the registers of iC-JX are reset except the interrupt bits IUSA, IUSD and ISD in Interrupt Status Register B.

I/O INTERFACES

Interfaces

iC-JX can be operated with either a serial (SPI) or parallel interface. This is set using pin NSP. When this pin is connected to VDD the device works in parallel mode. With NSP connected to ground iC-JX operates in serial mode.

Interface selection	
Pin NSP	selected interface
0	SPI
1	parallel

Table 12: Selection of interface with pin NSP

Parallel interface

The parallel interface in iC-JX consists of:

- 8 data lines: D7 . . . D0
- 5 address lines: A4 . . . A0
- 3 control lines: NCS, NRD, NWR

A circuit diagram of the parallel microcontroller interface is given in Figure 12.

Parallel interface: reading and writing data

The address lines A4 . . . A0 are used to select the registers in iC-JX. Address and data is accepted with the falling edge of chip select signal NCS. Control lines NRD and NWR govern read and write access

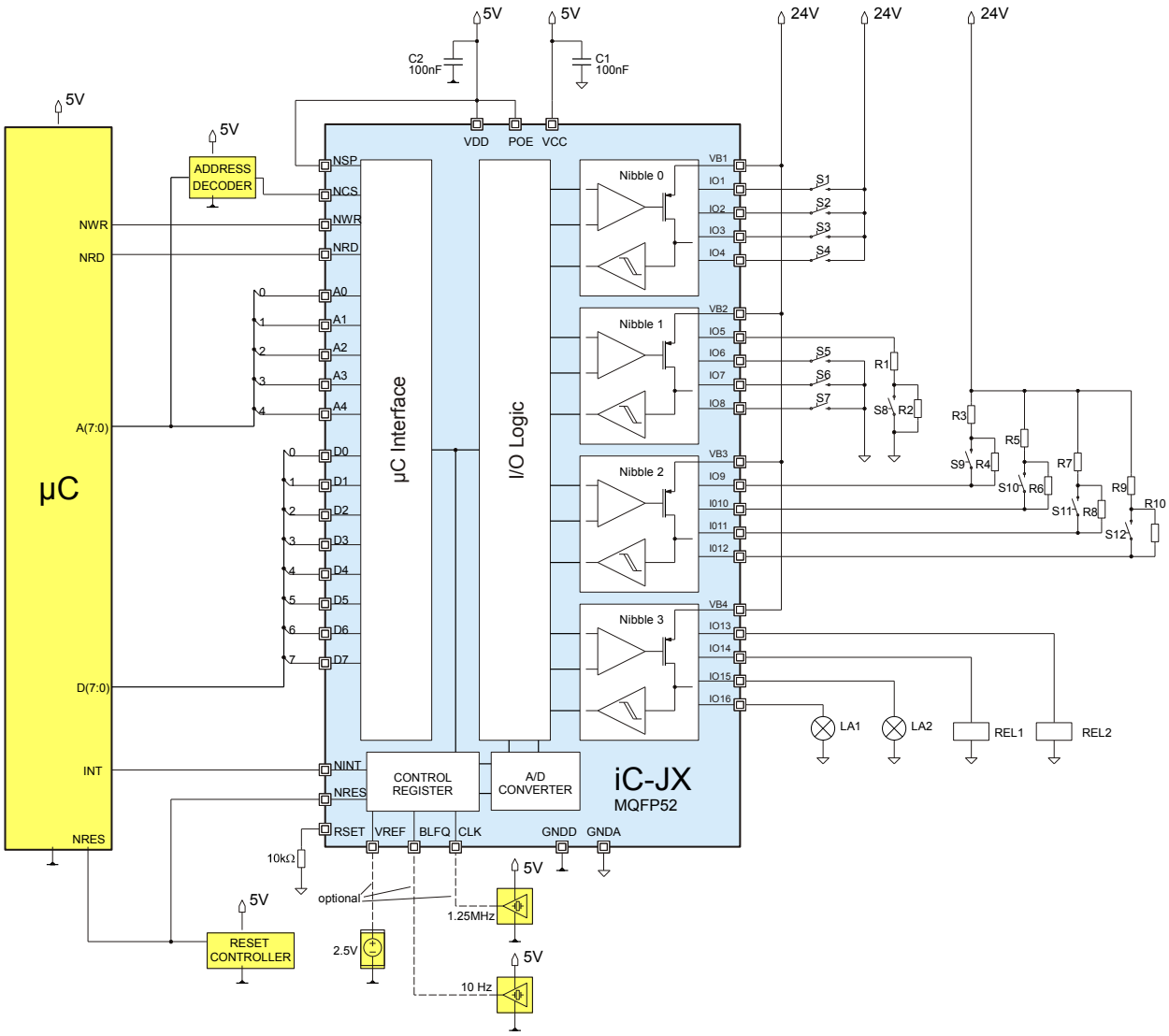


Figure 12: Example application using a parallel interface (pin NSP=1)

SPI interface

To reduce the number of lines running between the microcontroller and iC-JX and thus to economize on the use of optocouplers between the former and either one or several iCs in a unit, for example, an extended serial-peripheral interface (SPI) has been integrated into iC-JX. A possible wiring is shown in Figure 13.

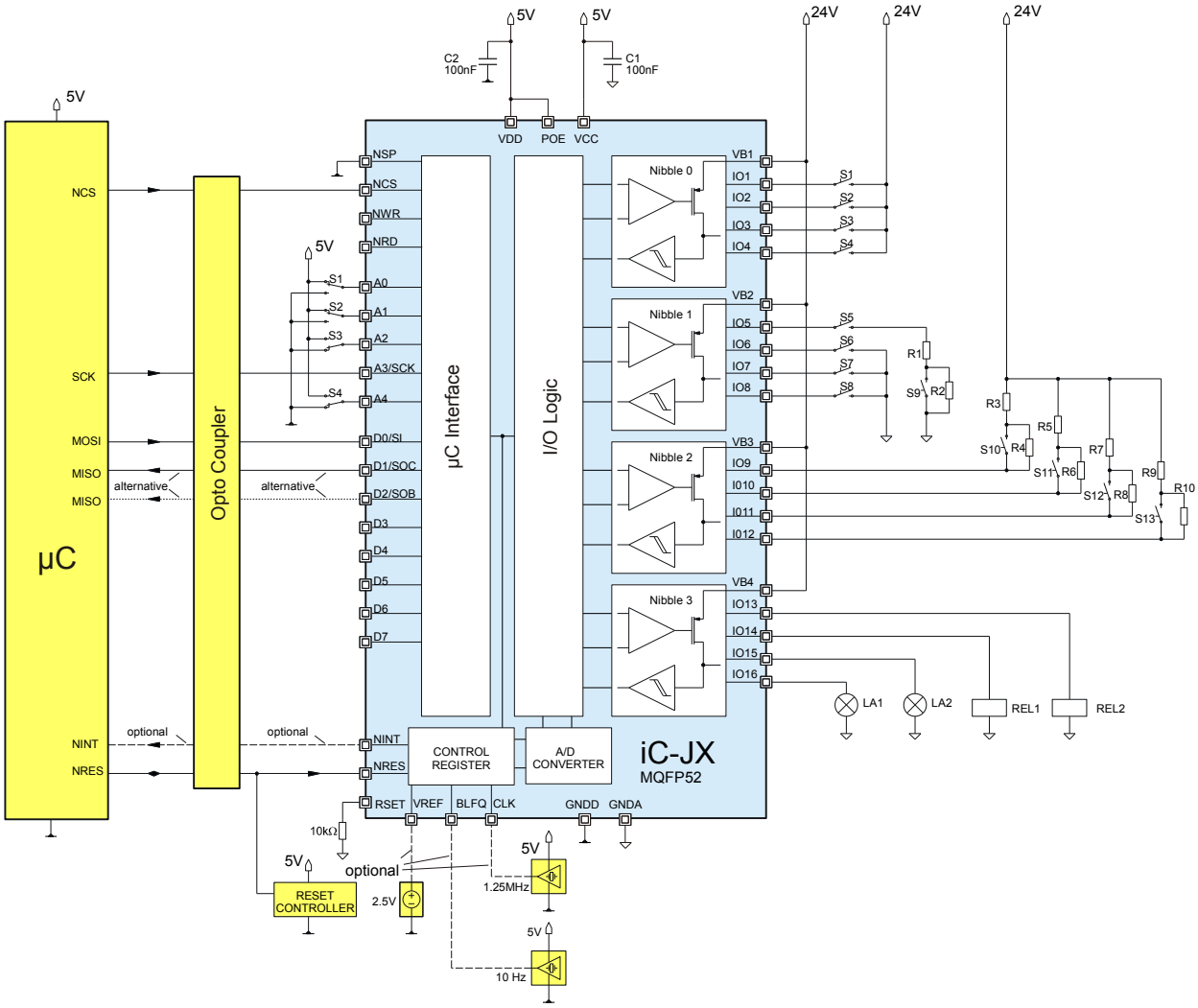


Figure 13: Example application using a serial interface (pin NSP=0)

SPI modes 0 and 3 are supported, i.e. idle level of SCK 0 or 1, acceptance of data on a rising edge. In order to ensure communication between the iC-JX and standard micro controllers, address and data words are both eight bit wide. Data is sent MSB first. The pins used for SPI communication are summarized in Tab. 13.

Pins used in SPI mode	
Pin	Function
A3/SCK	clock input
NCS	chip select input
D0/SI	data input
D1/SOC	data output chain[1]
D2/SOB	data output bus[1]
Note	[1] see Tab. 14

Table 13: Pins used in SPI Mode (NSP = 0)

The configuration (bus or chain) is set using pin A2. If A2 is at 0, the devices are in chain operation; if A2 is at '1', the chips switch to bus configuration.

SPI configuration (bus or chain)		
Pin A2	selected configuration	data output
0	chain	SOC
1	bus	SOB

Table 14: Selection of bus or chain SPI configuration with pin A2

Several iC-JXs can be operated on an SPI (see Fig. 14; SPI daisy chain: max. 4; SPI Bus with shared NCS: max. 4; SPI Bus with individual slaves: no limitation).

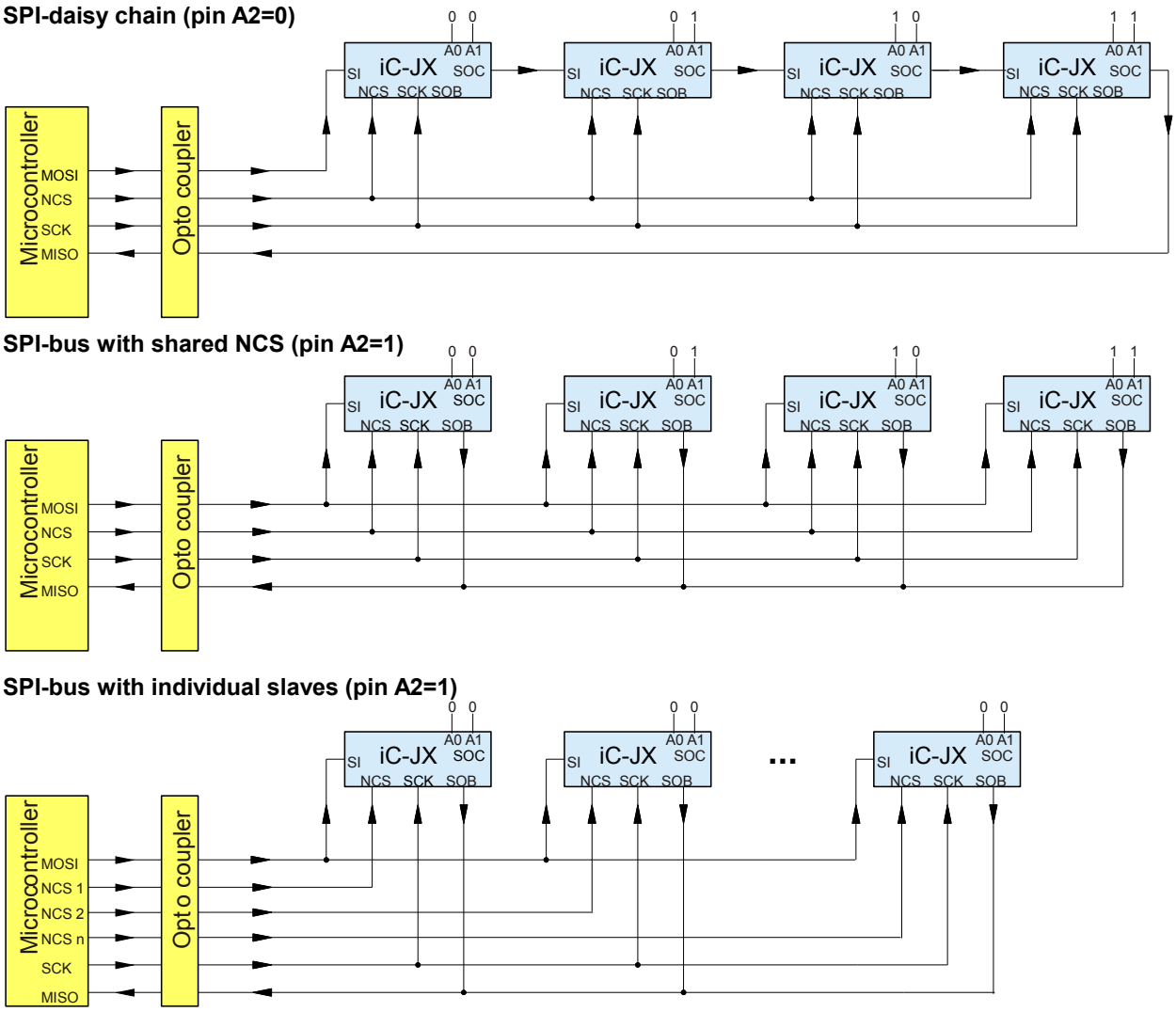


Figure 14: Possible SPI configurations (pin NSP=0)

In chain configuration (see Figure 14, top) output SOC of a device is connected up to the SI data input of the following chip; output SOB is not used. During the ad-

dressing sequence (1 byte of communication) all iC-JXs are switched through transparently so that all devices receive the transmitted address simultaneously. Only the addressed chip then goes into data transfer mode; the others remain transparent so that communication between the controller and addressed iC-JX can take place without delay. It must be noted here that even in transparent mode each iC-JX has a certain transmit time which has an effect on the maximum data frequency of the overall system. The advantage of this configuration lies in the fact that it is possible to read out the values of an address in all devices very quickly.

In bus configuration (see Figure 14, center) all SI inputs and SOB outputs are switched in parallel; the SOC outputs are not used. Addressing the devices ensures that only one of the chips outputs data to SOB; the outputs of the inactive iCs are switched to tristate. This type of configuration differs from chain configuration in that it permits higher clock rates and also allows up to four iC-JXs to be connected up to an SPI bus.

If no communication takes place on the SPI the chips can send interrupts to the controller by switching the master MISO line to 1. To this end all iC-JXs in chain configuration are switched through transparently (see Figure 15). In case of an interrupt message SOC is set to 1. In bus configuration the relevant chip drives a 1 at its SOB output towards the pull-down resistors at the outputs of the other devices.

Using pin A4 settings can be made as to whether interrupts are signaled to the master via the SOB or SOC pin (see Tab. 15).

Note:
The interrupt messaging via SOB must be deactivated in bus configuration if further non iC-JX devices are present on the SPI bus as otherwise data can collide on the bus which is not desirable here.

Interrupt Messaging via SOB/SOC	
Pin A4	interrupt message to pin SOB/SOC
0	disabled
1	enabled *)
Note	*) SOB/SOC = 1 in case of an interrupt

Table 15: Interrupt Messaging via SOB/SOC configuration with pin A4

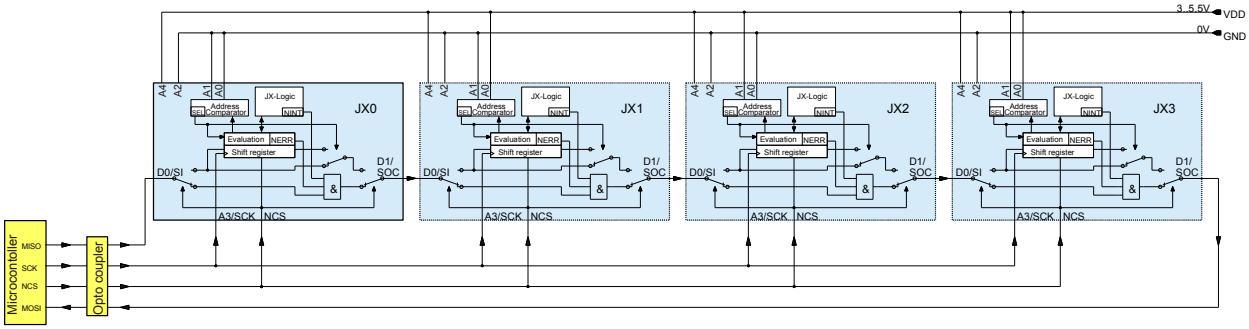


Figure 15: Addressing and interrupt messaging scheme in chain configuration

SPI: Setting address of an iC-JX

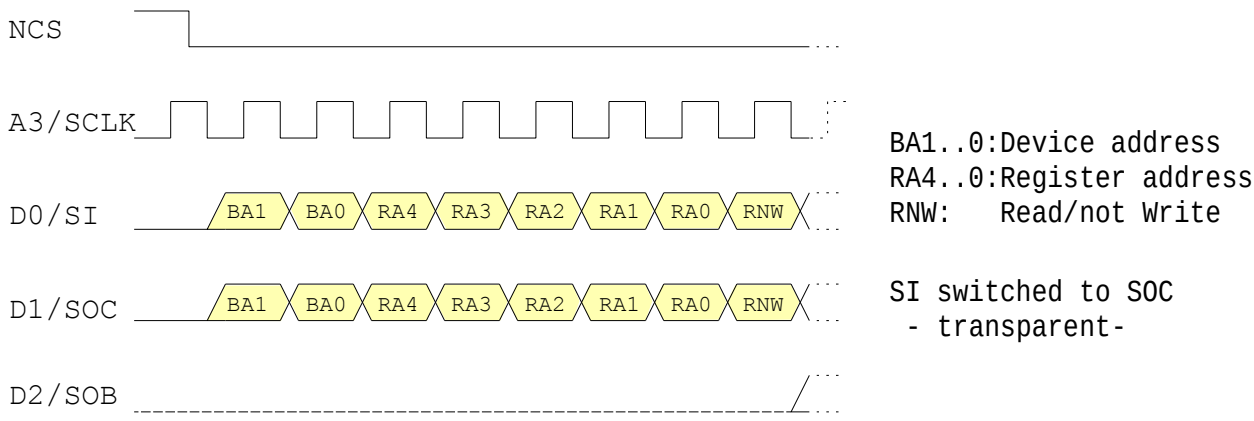


Figure 16: SPI: Addressing sequence

The first byte of communication (see Fig. 16) consists of the 2-bit chip address (BA1:0), the 5-bit register address (RA4:0) and a read-not-write (RNW) bit. The device ID is set for each chip using pins A(1:0). In chain configuration up to four devices can thus be connected to a SPI master.

SPI: Reading single data from an iC-JX

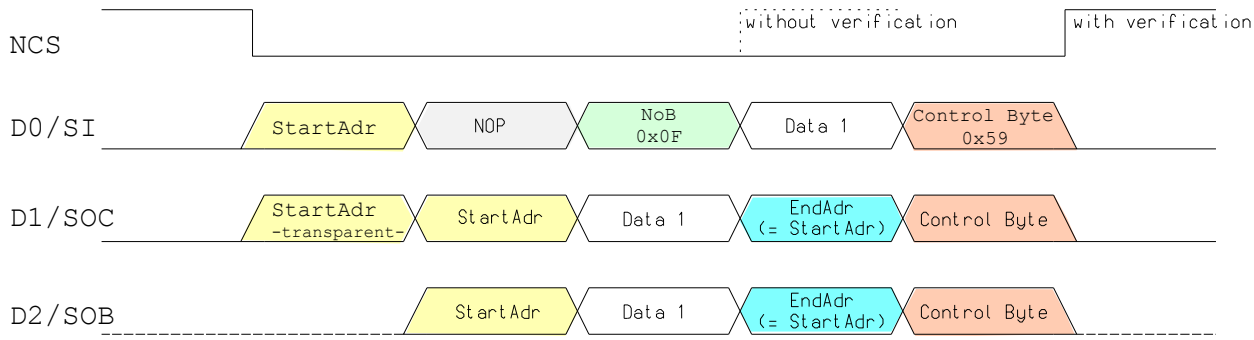


Figure 17: SPI: Reading a single register value

The following describes the SPI data transmission for a single read access (see Fig. 17). The first byte sent by the controller (master) is the address the data is to be read out from (addressing sequence see Fig. 16). The activated iC-JX (slave) sends the address back in the next byte by way of verification while the master sends a NOP (0x00) byte. The slave then sends the required data. The master sends byte NoB which is the number of bytes to be read out minus one. To increase security the number byte NoB is split into two nibbles which are encoded with the original and inverted value (0x0F when reading 1 byte, see Tab. 17).

If the user does not need the verification mechanisms of the master and the slave to validate the sent data, the master may terminate the read cycle at this point. The master otherwise sends the received data back to the slave which then returns the address of the read register (in this instance the start address) by way of verification. If this does not match the one originally sent by the master, the master can then abort communication and repeat if necessary. If the address is correct, in the next stage of the procedure the master transmits the control byte optimized for maximum error recognition (0x59).

For its part the slave checks that the returned data is correct; if this is so, it then also transmits the control byte 0x59. In the event of error an inverted value of 0xA6 is sent. During the transmission of this control byte the slave also checks whether the signals at SI and SOC/SOB are synchronous. If this is not the case (due to a spike occurring at SCK, for example), the slave transmits the inverted control byte as soon as it has detected the error.

The master recognizes a correct transmission by the fact that the control byte was received without error.

Control Byte	Status of transmission
0x59	correct transmission
other values	error during transmission

Table 16: Status of transmission indicated by Control Byte

NoB	Number of bytes	NoB	Number of bytes
0x0F	1	0x87	9
0x1E	2	0x96	10
0x2D	3	0xA5	11
0x3C	4	0xB4	12
0x4B	5	0xC3	13
0x5A	6	0xD2	14
0x69	7	0xE1	15
0x78	8	0xF0	16

Table 17: Setting the number of bytes to send/receive with NoB

SPI: Reading multiple data from an iC-JX

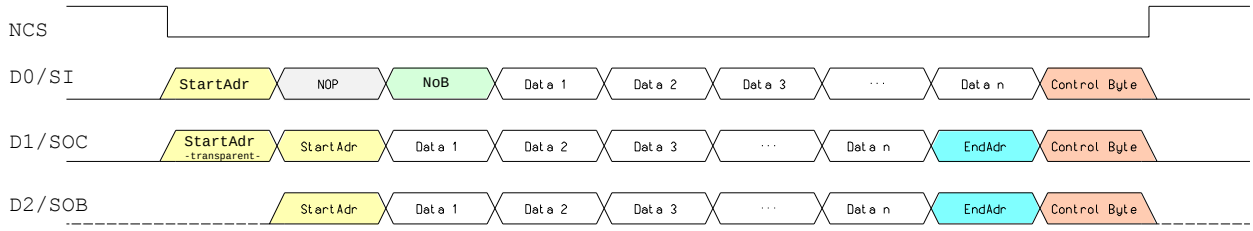


Figure 18: SPI: Reading several values of consecutive register addresses (auto-increment)

If data from several consecutive registers is to be read out (see Figure 18), the auto-increment function enables an abbreviated transmission protocol to be run using iC-JX. As in the reading of a single byte the controller sends the address, a NOP byte and the NoB byte (Number of bytes $\geq$ 2, see Tab. 17).

The addressed iC-JX repeats the start address and then transmits the consecutive register values and after one byte checks the data returned from the master for errors. Once the required number of register values has been sent the slave transmits the address of the last register addressed (EndAdr), followed by the control byte 0x59 with error-free transmission or the inverted value 0xA6 with an error in transmission. During transmission of the control byte the synchronism of the signals at SI and SOC/SOB is again checked; if these are not synchronous, on recognition of this fact the slave then transmits the inverted control byte.

SPI: Writing single/multiple data to an iC-JX

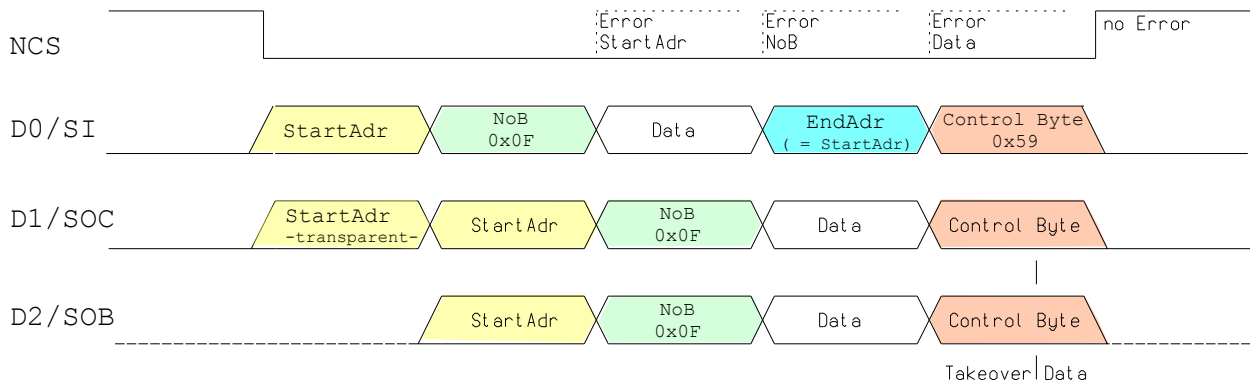


Figure 19: SPI: Writing a single register value

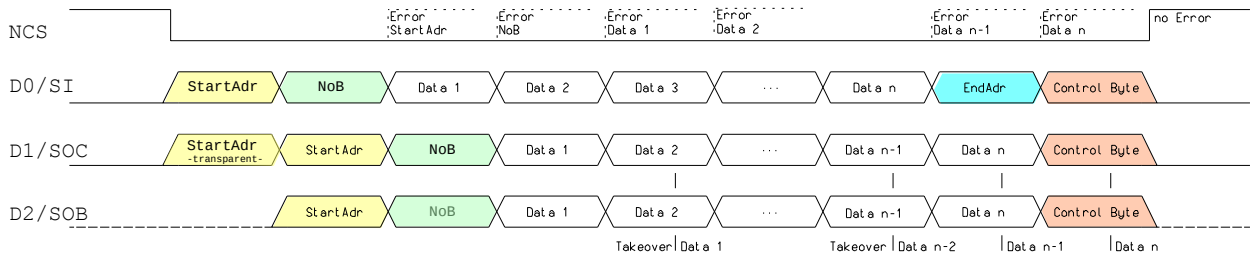


Figure 20: SPI: Writing several register values

In the write process one or several registers can be written during a transmit cycle (see Fig. 19 and 20). To this end the master first sends the start address (addressing sequence see Fig. 16) and the numerical amount of data to be transmitted minus one (NoB, see Tab. 17). As in the read process this value is transmitted as two nibbles (non-inverted and inverted) to increase security. Data from consecutive addresses is then sent by the master. iC-JX returns the master data with a delay of one byte, allowing the master to constantly monitor whether an error has occurred during the addressing sequence or data transmission. If an error is detected, the master can prevent the faulty data being accepted by the slave registers by ending communication.

SPI: Error handling

In order to reduce processing time complex technology, such as CRC, etc., is not used for error handling. The transmitted addresses and data are instead returned by the recipient to the sender where they are compared to the original data transmitted.

Should the master detect an error, it can abort communication in such a way so as to prevent incorrect values being written to the slaves.

If an individually addressed slave determines that the data it has sent has been returned to it incorrectly or that the number of clock pulses is not a multiple of 8 bits, it can signal this error to the master by inverting the closing control byte.

DESIGN REVIEW: Notes On Chip Functions

iC-JX X2 (and previous)		
No.	Function, parameter/code	Description and application notes
1	Leakage current beyond operating conditions (see Elec. Char. 019)	During operation, supply voltages VCC, VDD and VB1..VB4 must already be present and stable to avoid elevated leakage currents at pins IOx (x=1..16)

Table 18: Notes on chip functions regarding iC-JX chip release X2 and previous releases

iC-JX X3 and X3C		
No.	Function, parameter/code	Description and application notes
1	Leakage current beyond operating conditions (see Elec. Char. 019)	Leakage currents < 200 µA

Table 19: Notes on chip functions regarding iC-JX chip releases X3 and X3C

REVISION HISTORY

Rel.	Rel. Date*	Chapter	Modification	Page
C1	2010-02-04	. . .		

Rel.	Rel. Date*	Chapter	Modification	Page
C2	2016-08-12	all chapters	Complete specification revised and corrected. Improved structure, order and presentation of information.	
		REGISTER OVERVIEW	Binary representation A4. . . A0 corrected	15
		I/O INTERFACES	SPI: max. number of slaves corrected. SOB/SOC interrupt message method corrected. References to SPI broadcast deleted (broadcast is no longer possible).	39 ff.
		DESCRIPTION OF FUNCTIONS	Bit and address of undervoltage message VB1. . . 4 corrected in description	38
		DESCRIPTION OF FUNCTIONS	External resistor of 10 kΩ from RSET to ground is mandatory	32
		ABSOLUTE MAXIMUM RATINGS	Item #G001 parameter description corrected	5
		ELECTRICAL CHARACTERISTICS	Item #506 renamed #745 New item #746, #747	10 ff.
		REVISION HISTORY	Document revision history introduced as new chapter.	47

Rel.	Rel. Date*	Chapter	Modification	Page
D1	2023-06-14	ELECTRICAL CHARACTERISTICS	Item 103 changed to 2.3 V (max) Item 104 changed to -0.50 A (max)	6
		OPERATING REQUIREMENTS: Parallel µC Interface	Conditions: logic high level changed from 2.2V to 2.0 V	12
		OPERATING REQUIREMENTS: Serial µC Interface (SPI)	Conditions: logic high level changed from 2.2V to 2.0V Items 104, 105 changed to 165 ns (min) Items 107, 108 changed to 145 ns (max)	13

* Release Date format: *YYYY-MM-DD*

ORDERING INFORMATION

Type	Package	Order Designation
iC-JX	MQFP52	iC-JX MQFP52
Evaluation Board	-	iC-JX EVAL JX2D

Please send your purchase orders to our order handling team:

Fax: +49 (0) 61 35 - 92 92 - 692
E-Mail: dispo@ichaus.com

For technical support, information about prices and terms of delivery please contact:

iC-Haus GmbH
Am Kuemmerling 18
D-55294 Bodenheim
GERMANY

Tel.: +49 (0) 61 35 - 92 92 - 0
Fax: +49 (0) 61 35 - 92 92 - 192
Web: https://www.ichaus.com
E-Mail: sales@ichaus.com

Appointed local distributors: https://www.ichaus.com/sales_partners