iC-PR Series
REFLECTIVE OPTO ENCODERS

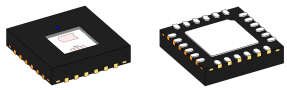
FEATURES

- Lensless, reflective opto-encoder iCs, compact, high-resolution, incremental
- Suitable reflective code discs of ∅ 4, ∅ 14, ∅ 26 and ∅ 43 mm and linear scales with 256 µm period length
- Monolithic *HD Phased Array* with excellent signal matching
- Integrated blue LED with power control, *EncoderBlue*®
- Low-noise signal amplifiers with high EMI tolerance
- Pin-selectable modes of operation: Digital A/B/Z (x1, x2, x4, x8, x16 interpolated), analog COS/SIN with analog or digital Z
- Pin-selectable index gating: Ungated (1 T), B-gated (0.5 T), AB-gated (0.25 T)
- Pin-selectable minimal edge distance: 80 ns, 1 µs, 10 µs
- Complementary quadrature outputs PA, NA, PB and NB
- Complementary index outputs PZ and NZ
- Analog signal output for ease of alignment and resolution enhancement by external interpolation
- Operating temperature range of -40 °C to +105 °C
- Compact and lensless optoQFN mold package
- Evaluation kits on request

APPLICATIONS

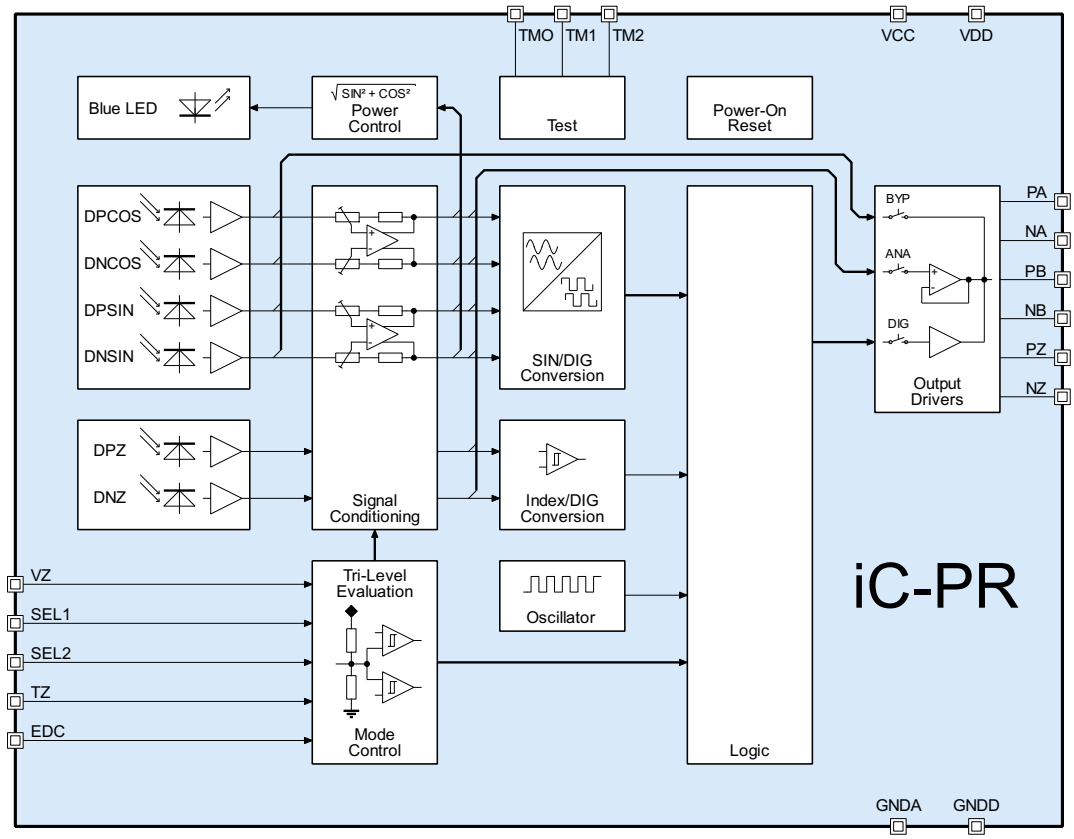
- Incremental encoders
- Miniature motors and actuators
- X-Y and linear stages
- Factory automation robots
- Consumer robots

PACKAGES



optoQFN24-4x4
4 mm x 4 mm x 0.9 mm
RoHS compliant

BLOCK DIAGRAM



DESCRIPTION

The iC-PR series are advanced optical, reflective, lensless encoder iCs featuring integrated HD Phased Array photosensors and a blue LED. They provide high signal quality with relaxed alignment tolerances. Differential digital ABZ outputs with or without interpolation or analog SIN/COS outputs with index are available. Typical applications are incremental encoders for motor control.

Blue-enhanced photosensors are adapted to the short wavelength of the embedded blue LED, and provide low-jitter outputs due to improved signal contrast. The unique assembly technology of the blue LED emitter and sensors results in low optical crosstalk.

Low-noise transimpedance amplifiers, arranged in a paired layout to ensure excellent channel matching, are used to convert the sensor signals into voltages of several hundred millivolts.

Various operation modes are selectable via tri-level inputs SEL1 and SEL2: Digital outputs with native (x1) or interpolated resolution (x2, x4, x8 or x16), analog outputs or mixed analog/digital outputs, where the latter one combines analog COS/SIN signals with a digital index. The amplified analog output signals allow for inspection and monitoring of encoder assembly. Moreover, feeding external interpolation circuits (e.g. iC-NQ, iC-TW8 or iC-TW28) is possible.

Index gating is also pin-selectable via input TZ: The options are ungated (1 T), B-gated (0.5 T) or AB-gated (0.25 T).

Via tri-level input EDC a minimal edge distance of 80 ns, 1 µs or 10 µs can be preset for digital operation modes.

The devices feature a low power consumption. They run at single-sided analog supplies of 4.5 V up to 5.5 V and single-sided digital supplies of 3.0 V up to 5.5 V.

iC-PR4307
Code disc ∅: 43.0 mm
Native CPR: 720

iC-PR26xx
Code disc ∅: 26.0 mm
Native CPR: 250, 256, 360

iC-PR1456
Code disc ∅: 14.0 mm
Native CPR: 250, 256

iC-PR0464
Code disc ∅: 4.0 mm
Native CPR: 64

iC-PR256
Linear scale: 256 µm period length

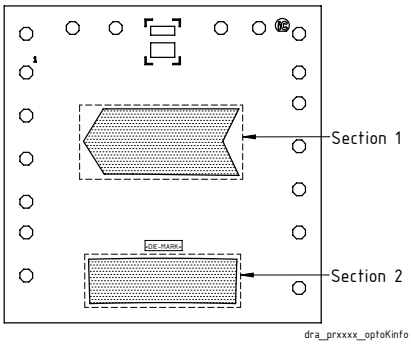
General notice on materials under excessive conditions
Epoxy resins (such as solder resists, IC package and injection molding materials, as well as adhesives) may show discoloration, yellowing, and surface changes in general when exposed longterm to high temperatures, humidity, irradiation, or due to thermal treatments for soldering and other manufacturing processes.

Equally, standard molding materials used for IC packages can show visible changes induced by irradiation, among others when exposed to light of shorter wavelengths, blue light for instance. Such surface effects caused by visible or IR LED light are rated to be of cosmetic nature, without influence to the chip's function, its specifications and reliability.

Note that any other material used in the system (e.g. varnish, glue, code disc) should also be verified for irradiation effects.

PACKAGING INFORMATION

SENSOR LAYOUT

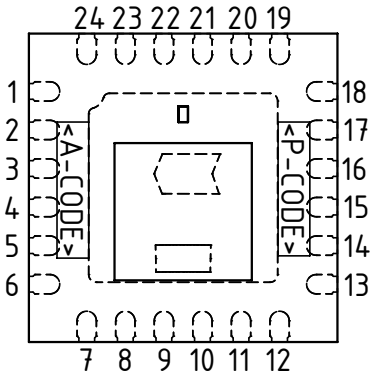


AOI CRITERIA

<Die Mark>	<Section>	<Area Class>[1]
iC PRnnnn	1	A25
	2	A40

[1] Inspection class for the optical inspection of detector areas. Refer to Optical Selection Criteria for further description.

PIN CONFIGURATION
oQFN24-4x4 (4 mm x 4 mm)



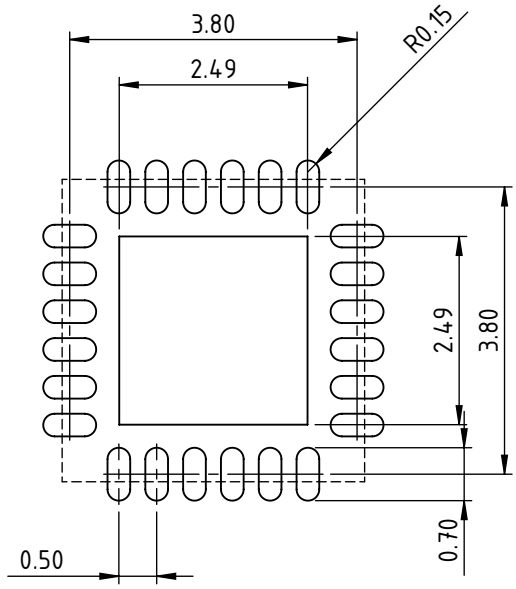
PIN FUNCTIONS

No.	Name	Function
1	VDD	+3.0 V...+5.5 V Digital Supply Voltage
2	SEL1	Mode Selection Input 1
3	SEL2	Mode Selection Input 2
4	TZ	Index Gating Control Input
5	PZ	Index Output Z+
6	NZ	Index Output Z-
13	EDC	Edge Distance Control Input
14	NB	Incr. Output B- / Analog SIN-
15	PB	Incr. Output B+ / Analog SIN+
16	NA	Incr. Output A- / Analog COS-
17	PA	Incr. Output A+ / Analog COS+
18	GNDD	Digital Ground
19	GNDA	Analog Ground
20	TMO	Test Mode Output [2]
21	TM2	Test Mode Input 2 [2]
22	TM1	Test Mode Input 1 [2]
23	VZ	Index Detection Control Input
24	VCC	+4.5 V...+5.5 V Analog Supply Voltage
7..12	n.c.[1]	
	BP	Backside Paddle [3]

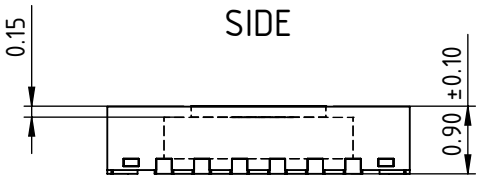
IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes);
1) Pin numbers marked with n.c. are not connected.
2) The test pins may remain unconnected. TM1, TM2, and TMO can be tied to GNDA to increase the noise immunity.
3) The backside paddle has to be connected by a single link to GNDA. A current flow across the paddle is not permissible.

PACKAGE DIMENSIONS

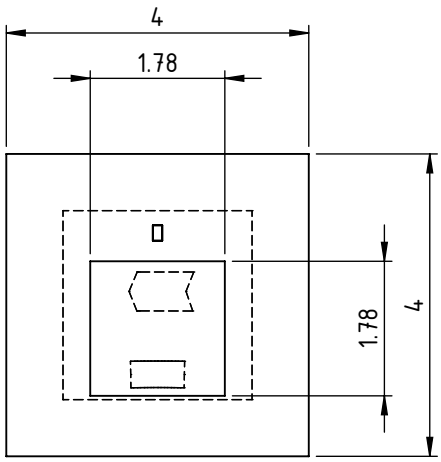
RECOMMENDED PCB-FOOTPRINT



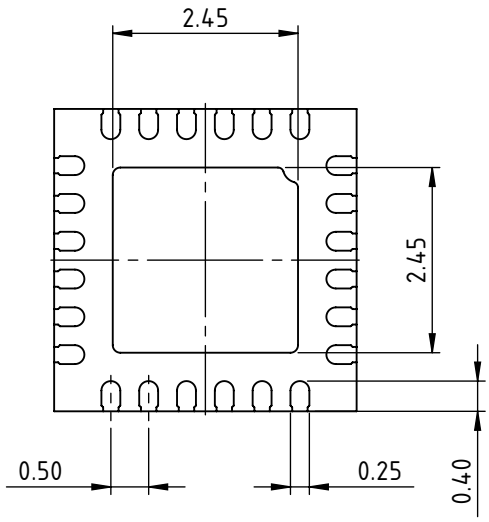
SIDE



TOP



BOTTOM



All dimensions given in mm. Tolerances of form and position according to JEDEC MO-220.
Positional tolerance of sensor pattern: ±70µm / ±1° (with respect to center of backside pad).
Maximum molding excess +20µm / -75µm versus surface of glass/reticle.

dra_prxxxx-oqfn24-1_pack_1, 10:1

ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these ratings device damage may occur.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VCC	Voltage at VCC		-0.3	6	V
G002	I(VCC)	Current in VCC		-20	100	mA
G003	VDD	Voltage at VDD		-0.3	6	V
G004	I(VDD)	Current in VDD		-20	100	mA
G005	I()	Pin Current, all signal outputs		-20	20	mA
G006	Vd()	Electrostatic Discharge	HBM, 100 pF discharged through 1.5 kΩ		2	kV
G007	Tj	Junction Temperature		-40	150	°C
G008	Ts	Chip Storage Temperature		-40	150	°C

[1] JEDEC document JEP 155: 500V HBM allows safe manufacturing with a standard ESD control process

THERMAL DATA

Operating conditions: VCC = 4.5...5.5 V, VDD = 3.0...5.5 V

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range		-40		105	°C
T02	Ts	Permissible Storage Temperature Range		-40		105	°C
T03	Tpk	Soldering Peak Temperature	tpk < 20 s, convection reflow MSL 3 (max. floor life 168 h at 30 °C and 60 % RH); Refer to Handling and Soldering Conditions for details.			245	°C
T04	Rthja	Thermal Resistance Chip to Ambient	package mounted on PCB according to JEDEC standard		50		K/W

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating conditions: VCC = 4.5...5.5 V, VDD = 3.0...5.5 V, Tj = -40...105 °C, unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VCC	Permissible Analog Supply Voltage		4.5		5.5	V
003	VDD	Permissible Digital Supply Voltage	VDD ≤ VCC	3.0		5.5	V
004	I()	Supply Current	I(VCC)+I(VDD), Photocurrent Amplifiers within op. range, fout() <250 kHz, no load refer to Table 5 for details		20		mA
Photocurrent Amplifiers							
101	Z()	Equivalent Transimpedance Gain	Z() = Vout()/Iph(), Tj = 27 °C for PA, NA, PB, NB for PZ, NZ		 4 6		 MΩ MΩ
102	fc()hi	Cut-off Frequency (-3 dB)		200			kHz
Analog Outputs PA, NA, PB, NB, PZ, NZ							
201	Vout()ac	AC Signal Amplitude	Mode AAMP Mode A250 Mode A500DZ		250 250 500		mV mV mV
204	Vout()mx	Permissible Maximum Output Voltage	Mode AAMP refer to Table 5 for typical values			2.2	V
206	Vout()d	Dark Signal Level	Mode AAMP voltage at NZ voltage at PA, NA, PB, NB with no illumination T = -40 °C T = 25 °C T = 125 °C	 870 780 640	 980 880 765	 1140 1060 940	 mV mV mV
207	ΔVout()d	Dark Signal Matching of A, B	Mode AAMP, output vs. output	-2.5		2.5	mV
208	TCVout()d	Temperature Coefficient of Dark Signal Level	Mode AAMP voltage at NZ voltage at PA, NA, PB, NB with no illumination		-1.4		mV/K
209	VREF	Reference Voltage	Mode A250, A500DZ	48	50	52	%VCC
210	V()act	Signal Level at PZ-activation	V(PZ)act = V(NZ) -V(PZ) at activation see also Figure 1 refer to Table 5 for details		180 .. 290		mV mV
211	I()mx	Permissible Load Current	Mode A250, A500DZ Mode AAMP	-1000 -100		1000 10	µA µA
212	C()mx	Permissible Capacitive Load				20	pF
Digital Outputs PA, NA, PB, NB, PZ, NZ							
401	fout()	Maximum Frequency per Output	Mode DX1, EDC low Mode DX2, EDC low Mode DX4, EDC low Mode DX8, EDC low Mode DX16, EDC low	0.2 0.4 0.8 1.6 1.85			MHz MHz MHz MHz MHz
402	AArel	AB Duty Cycle Variation	Mode DX1 Modes DX2, DX4, DX8, DX16 see also Figure 2	-5 -10		5 10	% %
403	HysD	Digital Hysteresis of Interpolator	Hysteresis with respect to one cycle of sine/cosine		5.6		°
404	Vs()lo	Saturation Voltage low	I() = 4 mA see also Figure 3			0.4	V
405	Isc()lo	Short-Circuit Current low	V() = VDD	7		110	mA
406	Vs()hi	Saturation Voltage high	Vs()hi = VDD - V(), I() = -4 mA see also Figure 3			0.4	V
407	Isc()hi	Short-Circuit Current high	V() = 0 V	-110		-7	mA
408	Tedc()	Edge Distance Control Time	EDC low EDC high EDC open	45 6600 640	80 10000 1000	135 14900 1520	ns ns ns

ELECTRICAL CHARACTERISTICS

Operating conditions: VCC = 4.5...5.5 V, VDD = 3.0...5.5 V, Tj = -40...105 °C, unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Tri-Level Programming Inputs SEL1, SEL2, EDC, TZ, VZ							
601	Vt()lo	Tri-Level Threshold Voltage low		10			%VCC
602	Vt()hi	Tri-Level Threshold Voltage high				90	%VCC
603	Vt()mid	Tri-Level Threshold Voltage mid		30		70	%VCC
604	V0()	Pin-Open Voltage		45	50	55	%VCC
605	Rpd()	Pull-Down Resistor	V() = VCC	65		140	kΩ
606	Rpu()	Pull-Up Resistor	V() = GNDA	65		140	kΩ
LED Power Control							
901	Iop()	Permissible LED Current		0.5		20	mA
902	Ictrl()	Controlled LED Output Current	refer to Table 5 for details		5 ..10		mA
Power-On Reset							
A01	VCCon	Turn-on Threshold VCC (power-on release)	increasing voltage at VCC VDD >VDDon, LED Current and Photocurrent Amplifiers within op. range			3.95	V
A02	VCCoff	Turn-off Threshold VCC (power-down reset)	decreasing voltage at VCC VDD >VDDon, LED Current and Photocurrent Amplifiers within op. range	3.00			V
A03	VCChys	Threshold Hysteresis VCC	VCChys = VCCon - VCCoff	200	300	400	mV
A04	VDDon	Turn-on Threshold VDD (power-on release)	increasing voltage at VDD VCC >VCCon, LED Current and Photocurrent Amplifiers within op. range			2.95	V
A05	VDDoff	Turn-off Threshold VDD (power-down reset)	decreasing voltage at VDD VCC >VCCon, LED Current and Photocurrent Amplifiers within op. range	2.3			V
A06	VDDhys	Threshold Hysteresis VDD	VDDhys = VDDon - VDDoff	180	240	300	mV

ELECTRICAL CHARACTERISTICS: Diagrams

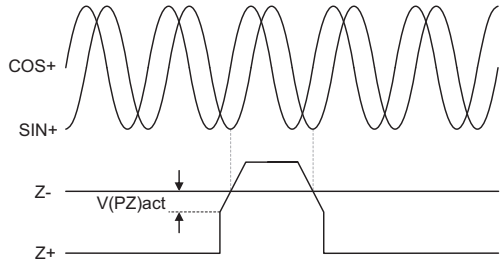


Figure 1: Z-signal level definition.

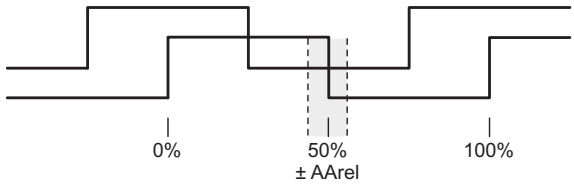


Figure 2: Definition of AB duty cycle variation.

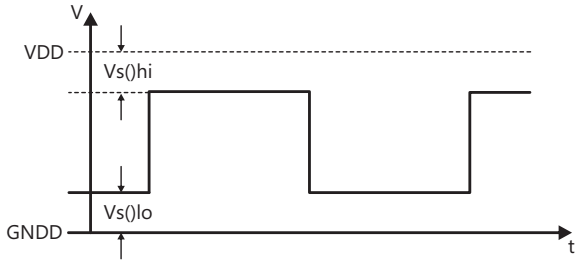


Figure 3: Digital Signal Levels.

SIGNAL DEFINITIONS

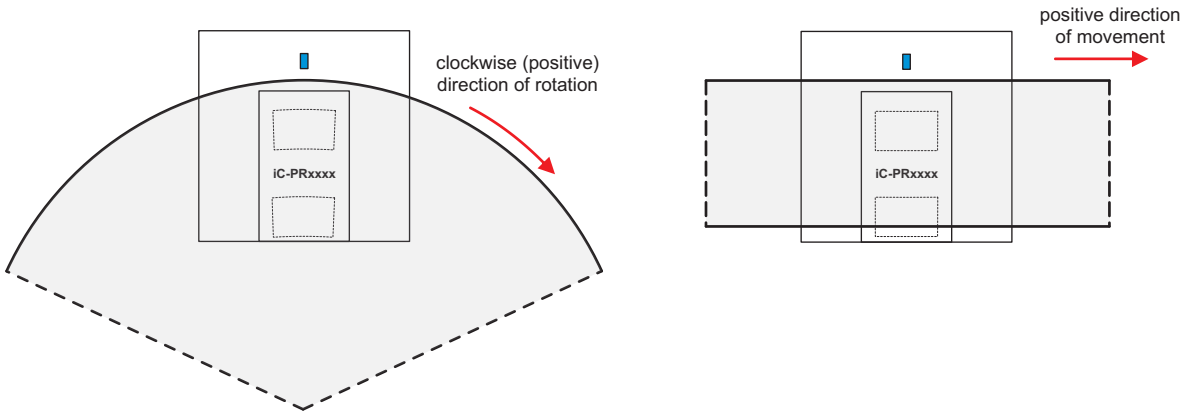


Figure 4: Definition of clockwise rotation / positive direction of movement.

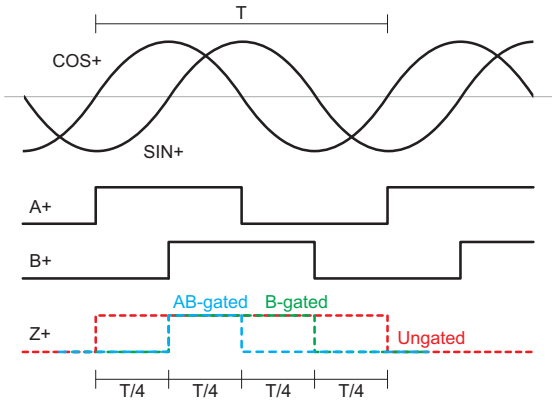


Figure 5: Signal definitions for clockwise rotation / positive direction of movement.

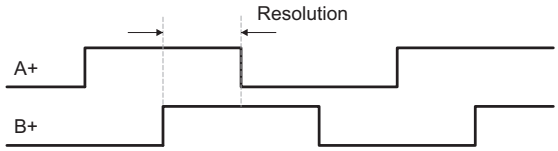


Figure 6: Definition of resolution for linear series.

VOLTAGE DOMAINS

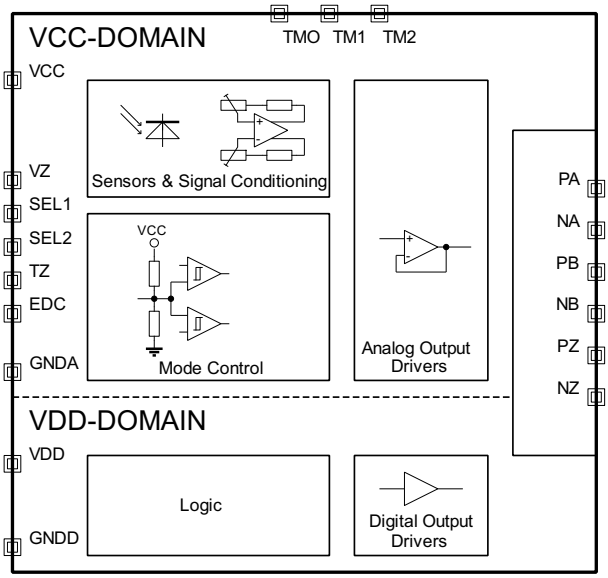


Figure 7: Analog and digital voltage domains

In iC-PR, the analog and the digital supply voltages are applied at different pins. On the one hand, this improves the quality of the analog signals, on the other hand, the digital signal output levels can be chosen to match subsequent circuitry. The internal voltage domains are shown in Fig. 7.

Please note:

- Permissible voltage ranges for VCC, VDD specified in Electrical Characteristics, parameters No. 001 and No. 003, respectively
- VDD $\leq$ VCC
- reference voltage / high level for mode pins is VCC
- GNDA and GNDD must be at the same potential but should be connected with separate lines from a star point on the PCB

OPERATION MODES

The iC-PR series features 8 principle operation modes, which are selectable by the voltages applied to the pins SEL1 and SEL2, as summarized in Table 1.

These tri-level inputs might be connected to a voltage below Vt()lo (low, see 601), a voltage above Vt()hi (high, see 602) or a voltage between the specified values of Vt()mid (open, see 603). For other voltages the function is undefined.

The open configuration can be easily obtained by an external voltage divider. Alternatively, when the pin is left unconnected, the iC itself biases the input at 50% VCC (see 604).

Note: Static pin voltages at SEL1 and SEL2 are required during operation. If changing the setting of SEL1 and SEL2 pins during operation, power-on reset of iC-PR is required.

SEL1	SEL2	Mode	Description
low	high	DX1	digital A/B/Z (x1 interpolation)
high	low	DX2	digital A/B/Z (x2 interpolation)
low	open	DX4	digital A/B/Z (x4 interpolation)
high	high	DX8	digital A/B/Z (x8 interpolation)
high	open	DX16	digital A/B/Z (x16 interpolation)
open	low	A250	analog COS/SIN (VREF $\pm$ 250 mV), analog Z, see Figure 8
open	high	AAMP	analog COS/SIN (transimpedance amps. $\pm$ 250 mV), analog Z, see Figure 8
open	open	A500DZ	analog COS/SIN (VREF $\pm$ 500 mV), digital Z (ungated), see Figure 8

Table 1: Operation modes selectable by pins SEL1/2.

ANALOG / MIXED OPERATION MODES

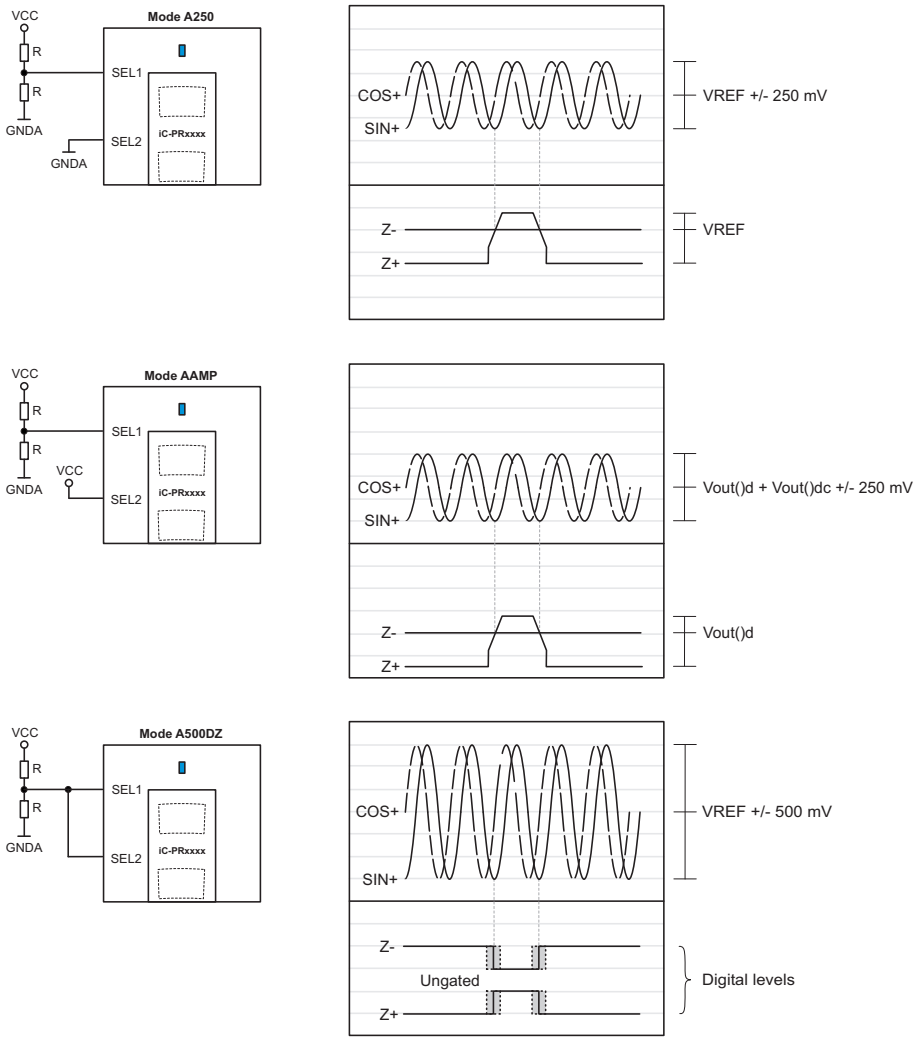


Figure 8: Analog / mixed operation modes. Complementary signals COS- and SIN- not shown.

- Vout()d is the dark signal level of the analog signals. It is independent of illumination but proportional to temperature.
- Vout()dc is the dc-level of the analog signals with respect to the dark signal level. It is proportional to illumination but independent of temperature.
- The permissible load current for the analog outputs is specified as parameter 211 in the Electrical Characteristics.
- For correct functionality of the Z-index, programming pin VZ has to be set to a proper value as described in section INDEX DETECTION THRESHOLD.

DIGITAL OPERATION MODES

INTERPOLATION FACTOR AND INDEX GATING

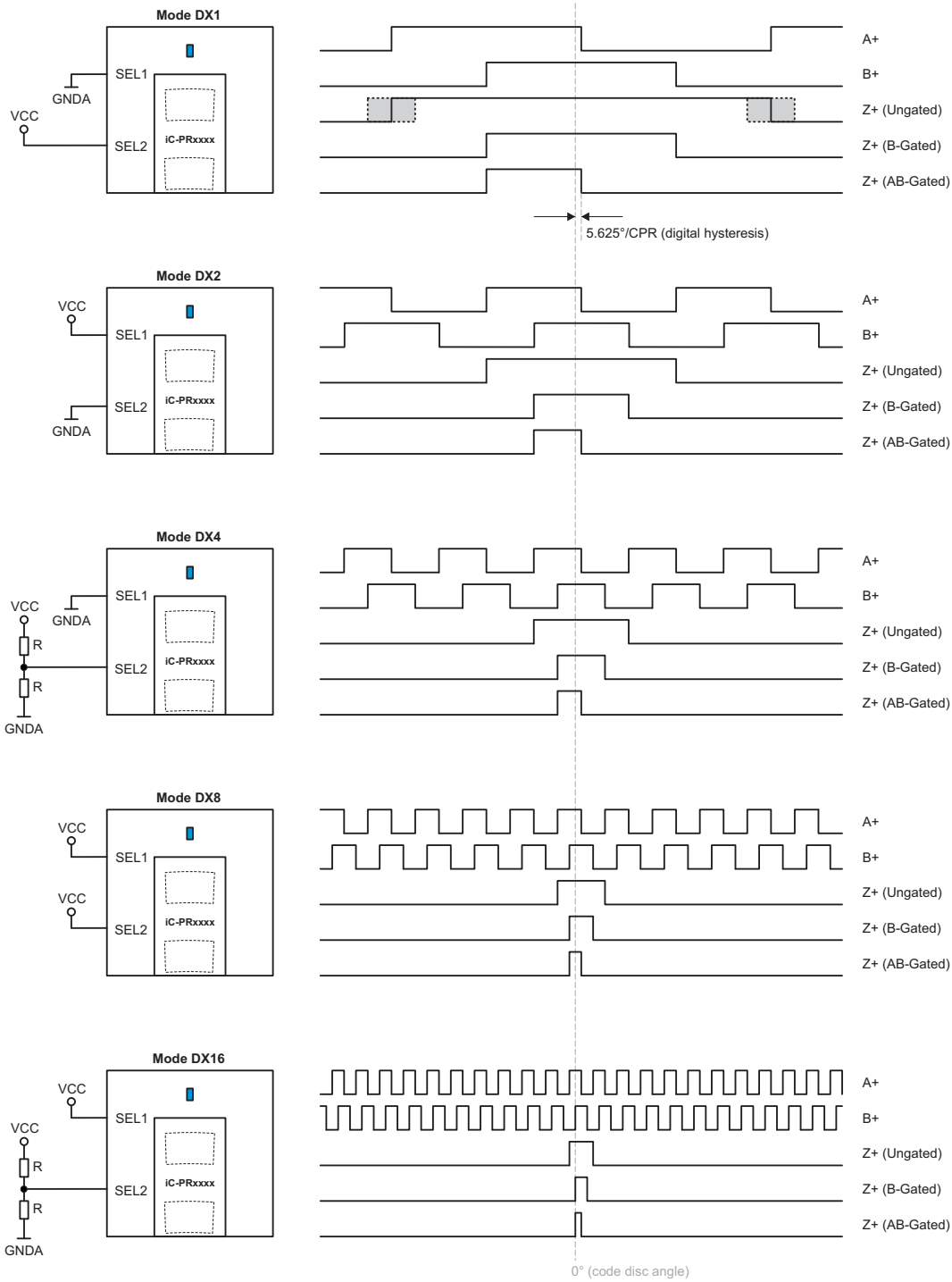


Figure 9: Digital operation modes (interpolation and index gating). Complementary signals A-, B- and Z- not shown.

An overview of the digital modes (interpolation and index gating) is depicted in Figure 9. The index gating can be controlled via tri-level pin TZ, as defined by Table 2.

Note: Static pin voltage at TZ is required during operation.

TZ	Description
low	B-gated index (180°)
high	Ungated index (360°)
open	AB-gated index (90°)

Table 2: Index gating controlled by pin TZ.

For correct functionality of the Z-index, programming pin VZ has to be set to a proper value as described in section INDEX DETECTION THRESHOLD.

DIGITAL HYSTERESIS

In all interpolation modes the iC-PR series features a digital angular hysteresis of $\frac{360°}{64 \cdot CPR}$, i.e. 1 LSB of the angular resolution in mode DX16. As illustrated in Figure 10, the digital hysteresis corresponds to a slip existing between the two rotating directions. In this way multiple switching of the incremental signals at the reversing point of a changing direction of rotation is prevented.

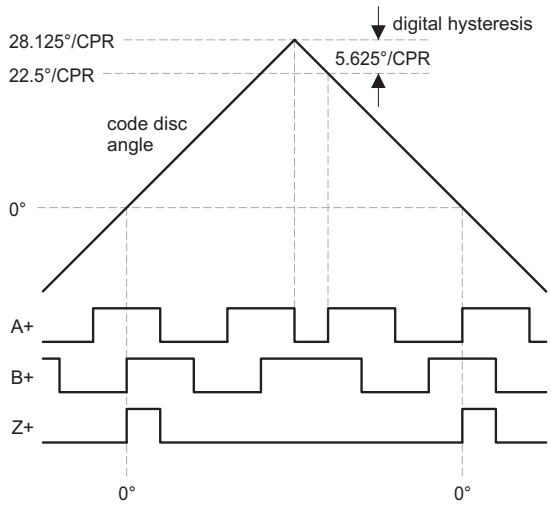


Figure 10: Digital hysteresis in mode DX16 with AB-gated index.

EDGE DISTANCE CONTROL

The edge distance is defined as the time between two consecutive AB edges, as depicted in Figure 11.

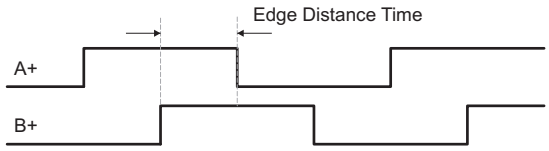


Figure 11: Definition of the edge distance time.

With the tri-level input pin EDC a minimal edge distance of 80 ns, 1 µs or 10 µs (typical values) can be configured to suit the system on hand (cable length, external counter). It is recommended to set EDC low.

Note: Static pin voltage at EDC is required during operation.

EDC	Description
low	80 ns minimal edge distance
high	10 µs minimal edge distance
open	1 µs minimal edge distance

Table 3: Minimal edge distance controlled by pin EDC.

STARTUP BEHAVIOR

When iC-PR is powered on, the digital outputs are held in a defined state:

PA = NA = PB = NB = low
PZ = NZ = high

This specific combination of output signal levels is invalid during normal operation, hence signalizing that the iC is in the startup phase. Once the logic has found and verified the code disc position, valid A/B/Z signals are then output henceforth.

Note: iC-PR will also enter or remain in the startup state, when the regulated LED current exceeds a specific value, e.g. due to code disc misalignment. Once the LED current returns to a valid range, the logic will again search for the code disc position and output valid A/B/Z signals afterwards.

INDEX DETECTION THRESHOLD

Via tri-level pin VZ an internal threshold for the index detection can be controlled, as described in Table 4. Setting VZ low (maximal threshold), a safe detection of the index pulse requires stronger illumination of the respective photodiodes, which also results in a stronger interference resistance against extraneous or stray light. On the other hand, with VZ high (minimal threshold) less illumination of the index photodiodes is required for a safe detection. However, in this case the interference resistance is reduced respectively. With VZ open the threshold lies in between the other two options.

For air gap above 1.5 mm (IC to code disc), the recommended value for VZ is shown in Table 5. For smaller air gaps, it may be necessary to decrease the index detection threshold.

Note: VZ affects all operation modes, no matter if the index signal is analog or digital.

VZ	Description
low	Maximal threshold
high	Minimal threshold
open	Medium threshold

Table 4: Index detection controlled by pin VZ.

POWER CONTROL

iC-PR devices regulate the current through the integrated blue LED, keeping the optical power constant regardless of aging effects, varying temperature or changes in air gap (iC to code disc).

In case of strong code disc misalignment or in the absence of any code disc, a maximum current is sent through the LED, which corresponds to an overall supply current of typ. 80 mA.

When code disc and iC-PR are properly aligned, the LED current is significantly reduced and mainly depends on the code disc type and the actual air gap (see Table 5 for typ. supply current values).

SAFETY ADVICE

Depending on the mode of operation, these devices emit highly concentrated visible blue light which can be hazardous to the human eye.

Products which incorporate these devices have to follow the safety precautions given in IEC 60825-1 and IEC 62471.

HANDLING ADVICE

Because of the specific housing materials and geometries used, these LED devices are sensitive to rough handling or assembly and can thus be easily damaged or may fail in regard to their electro-optical operation. Excessive mechanical stress or load on the LED surface or to the glass windows must be avoided.

DEVICE OVERVIEW

Device	CPR	Code Disc		Supply Current / mA		Max. RPM		VZ	V(PZ)act	Vout()mx
	native	P/O Code	Type	1.5mm [1]	2.0mm [1]	DX1..8/Ax	DX16	≥1.5 mm [1]	/ mV	/ V
⌀ 43 Series										
iC-PR4307	720	PR28S	P	21	27	16 000	9 000	low	290	1.70
⌀ 26 Series										
iC-PR2604	360	PR24S	P	21	26	32 000	18 000	low	290	1.55
iC-PR2656	256	PR25S	P	16	18	45 000	25 000	open	280	1.55
iC-PR2656	250	PR30S	P	16	18	45 000	25 000	open	280	1.55
⌀ 14 Series										
iC-PR1456	256	PR27S	P	21	27	45 000	25 000	high	180	1.80
iC-PR1456	250	PR29S	P	21	27	45 000	25 000	high	180	1.80
⌀ 04 Series										
iC-PR0464	64	PR06S	M	21	27	180 000	100 000	high	200	1.65

Device	Res.	Code Disc		Supply Current / mA		Max. Speed / m/s		VZ	V(PZ)act	Vout()mx
	DX16	P/O Code	Type	1.5 mm [1]	2.0 mm [1]	DX1..8/Ax	DX16	≥1.5 mm [1]	mV	V
Linear Series										
iC-PR256	4 µm	PR01L	F	16	18	50	28	low	290	1.55

Type M = Metal
Type P = Polycarbonate
Type F = Film
Type [ ] = Glass

Definition of resolution for linear series see Figure 6.

Device availability on request.

Table 5: Device overview

[1] Air gap (iC vs. code disc)

DESIGN REVIEW: Notes On Chip Functions

PRnnnn	Chip release Y	
No.	Function, Parameter/Code	Description and Application Hints
		No fiducials to align IC to reference structures on PCB.

Table 6: Design review

PRnnnn	Chip release X, X1, W	
No.	Function, Parameter/Code	Description and Application Hints
		None at time of printing.

Table 7: Design review

APPLICATION NOTES

Application notes for iC-PR-series devices are shown separately.

REVISION HISTORY

Rel.	Rel. Date[1]	Chapter	Modification	Page
A1	2015-11-23		Initial Release	all

Rel.	Rel. Date[1]	Chapter	Modification	Page
A2	2016-03-31	BLOCK DIAGRAM	Block diagram updated.	1
		ELECTRICAL CHARACTERISTICS	204, 212: Moved value from "min." to "max." as defined as "permissible"	6
		SIGNAL DEFINITIONS	Figure for definition of resolution in linear series added.	9
		OPERATION MODES	Description of analog modes in Table 1 updated.	9
		DIGITAL OPERATION MODES	Recommended EDC configuration added.	12
		INDEX DETECTION THRESHOLD	Updated description.	13
		DEVICE OVERVIEW	Device overview table extended and updated. Changed recommendation for VZ.	14

Rel.	Rel. Date[1]	Chapter	Modification	Page
A3	2017-02-20	DESCRIPTION	Added "General notice on materials under excessive conditions"	2
		PACKAGING INFORMATION	Changed footnote for TM1, TM2, TMO	3
		ABSOLUTE MAXIMUM RATINGS	G002, G004: Changed max. values	5
		THERMAL DATA	T02: Permissible Storage Temperature Range added T04: Corrected unit	5
		ELECTRICAL CHARACTERISTICS	405/407: Max./Min. value changed 605/606: Added max. value	6,7
		SIGNAL DEFINITIONS	Added definition of positive direction of movement for linear series	9
		VOLTAGE DOMAINS	Added section	10
		ANALOG / MIXED OPERATION MODES	Added note on VZ Changed figure	11
		DIGITAL OPERATION MODES	Added note on VZ	13
		INDEX DETECTION THRESHOLD	Added Note	14
		POWER CONTROL	Description of power control added	14
		DEVICE OVERVIEW	Changed Code Disc P/O Code, Type	19

Rel.	Rel. Date[1]	Chapter	Modification	Page
A4	2020-06-08	PACKAGING INFORMATION	AOI criteria added	3
		ELECTRICAL CHARACTERISTICS	Added figure for Vs()low and Vs()hi	8
		DIGITAL OPERATION MODES	Description of minimal edge distance updated.	13
		SAFETY ADVICE	Added section	14
		HANDLING ADVICE	Added section	14
		DEVICE OVERVIEW	Added Vout()mx	15

Rel.	Rel. Date[1]	Chapter	Modification	Page
B1	2023-03-08	ABSOLUTE MAXIMUM RATINGS	ESD description	5
		THERMAL DATA	MSL changed	5
		DESIGN REVIEW: Notes On Chip Functions	Chapter added	16
		ORDERING INFORMATION	Detailed description	20

Rel.	Rel. Date[1]	Chapter	Modification	Page
B2	2023-08-01	PACKAGING INFORMATION	AOI CRITERIA updated	3

[1] Release Date format: *YYYY-MM-DD*

ORDERING INFORMATION

Type	Package	Options	Order Designation
iC-PRnnnn	24-pin optoQFN, 4 mm x 4 mm, 0.9 mm thickness RoHS compliant	nnnn = device version	iC-PRnnnn oQFN24-4x4
Evaluation kit	iC-PR0464 oQFN24-4x4, PR1M (61mm x 64 mm), Code Disc PR06PS		iC-PR0464 EVAL PR1M
	iC-PR1456 oQN24-4x4, PR1M (61mm x 64 mm), Code Disc PR27PS+PR29PS		iC-PR1456 EVAL PR1M
	iC-PR2604 oQFN24-4x4, PR1M (61mm x 64 mm), Code Disc PR24PS		iC-PR2604 EVAL PR1M
	iC-PR2656 oQFN24-4x4, PR1M (61mm x 64 mm), Code Disc PR25PS+PR30PS		iC-PR2656 EVAL PR1M
	iC-PR4307 oQFN24-4x4, PR1M (61mm x 64 mm), Code Disc PR28PS		iC-PR4307 EVAL PR1M
	iC-PR256 oQFN24-4x4, PR1M (61mm x 64 mm), Linear Scale PR01FL		iC-PR256 EVAL PR1M
Mother board	Adapter PCB PR2M (80 mm x 110 mm)	incl. ribbon cable	iC-PR EVAL PR2M

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