iC-TW39

preliminary

24-BIT MAGNETIC ON-AXIS ANGLE SENSOR

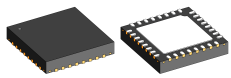
FEATURES

- TMR-based absolute angle sensor over 360 °
- High operating distance and axial play tolerance
- Automatic signal error correction
- Rotation speed up to 360,000 rpm
- FlexCount® ABZ output from 1 up to 65536 AB cycles
- Adjustable zero position and length
- AB output frequency up to 12.5 MHz
- Outstanding AB jitter performance (e.g. ±2 % at 2500 cpr)
- UVW output at 1 up to 32 cpr, adjustable rotor angle
- Bidirectional open-source BiSS Interface, profile compatible
- High angle resolution (24-bit ST)
- 24-bit revolution counting
- High accuracy (INL ±0.15°) and repeatability (0.04°)
- Ultra-low output lag of 1.5 µs
- Configurable status monitoring for alarm output
- 20 MHz SPI interface
- Internal EEPROM
- Single 3.3 V supply, low power consumption (typ. 30 mA)
- Operating temperature range of –40 to +125 °C

APPLICATIONS

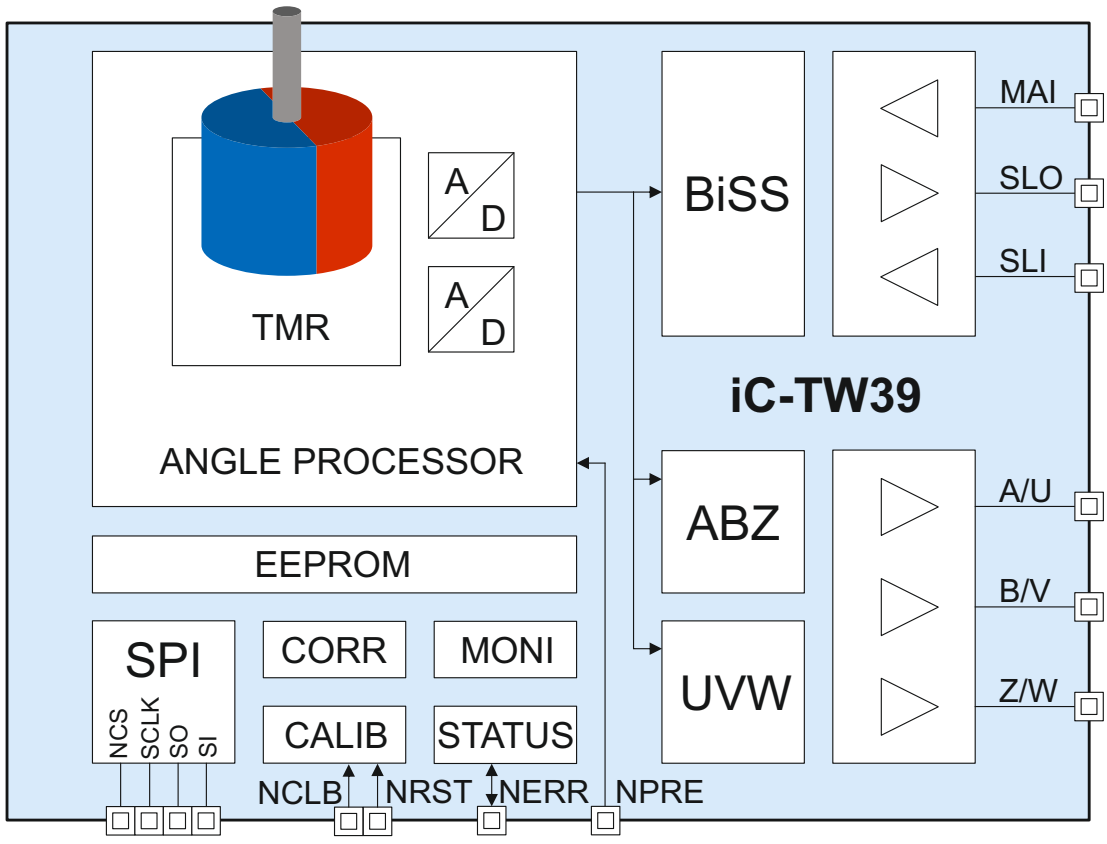
- High-resolution angle sensing
- Brushless motor commutation (2...64 poles)
- Servo motor control
- Incremental or absolute rotary encoders

PACKAGES



32-pin QFN
5 mm x 5 mm
RoHS compliant

BLOCK DIAGRAM



DESCRIPTION

The iC-TW39 is a very compact TMR-based system-on-chip solution for 360-degree absolute angle sensing in the end-of-shaft position. The sensor tracks the magnetic field direction only in the X-Y chip plane, with reasonable placement tolerances of the IC, especially for the operating distance to the diametrical magnet. Therefore, an axial play of the motor shaft can be tolerated without significant impact on angular accuracy.

The sensor signal is resolved by a high-resolution interpolator, featuring resolution-enhancing digital filtering and automatic signal error correction. The device ensures minimal angular error, excellent position jitter even at low speeds, and unmatched position noise at standstill.

The fast data processing refreshes the absolute angle position every 20 ns for immediate output via BiSS, SSI or SPI.

Additionally, incremental ABZ quadrature signals are provided with FlexCount® resolution of 1 up to 65536 cycles per revolution, with an adjustable Z position and length. The incremental outputs can also provide UVW commutation signals for 1 to 32 pole-pair motors, alternatively.

The iC-TW39 can be configured via SPI or the bidirectional BiSS Interface, which supports encoder profiles 3 and 3S, simplifying BiSS master connection.

Extensive status and signal quality monitoring capabilities allow detection and notification of poor operating conditions, as well as drive monitoring for predictive maintenance.

The iC-TW39 requires minimal external components for operation. An EEPROM for storage of configuration and calibration data is already integrated on-chip.

Adding external RS-422 line drivers/receivers allows extended cabling for BiSS and incremental applications with encoder quadrature outputs.

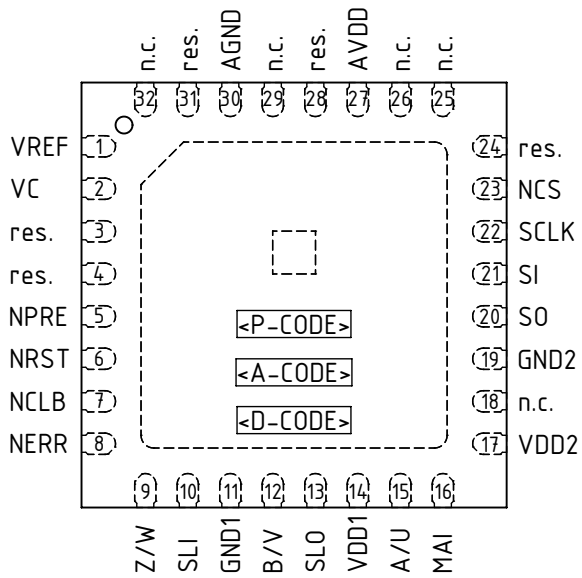
General notice on application-specific programming
Parameters defined in the datasheet represent supplier's attentive tests and validations, but - by principle - do not imply any warranty or guarantee as to their accuracy, completeness or correctness under all application conditions. In particular, setup conditions, register settings and power-up have to be thoroughly validated by the user within his specific application environment and requirements (system responsibility).

The chip's performance in application is impacted by system conditions like the quality of the magnetic target, field strength and stray fields, temperature and mechanical stress, sensor alignment and initial calibration.

CONTENTS

PACKAGING INFORMATION

PIN CONFIGURATION
QFN32 5 mm x 5 mm (top view)



PIN FUNCTIONS

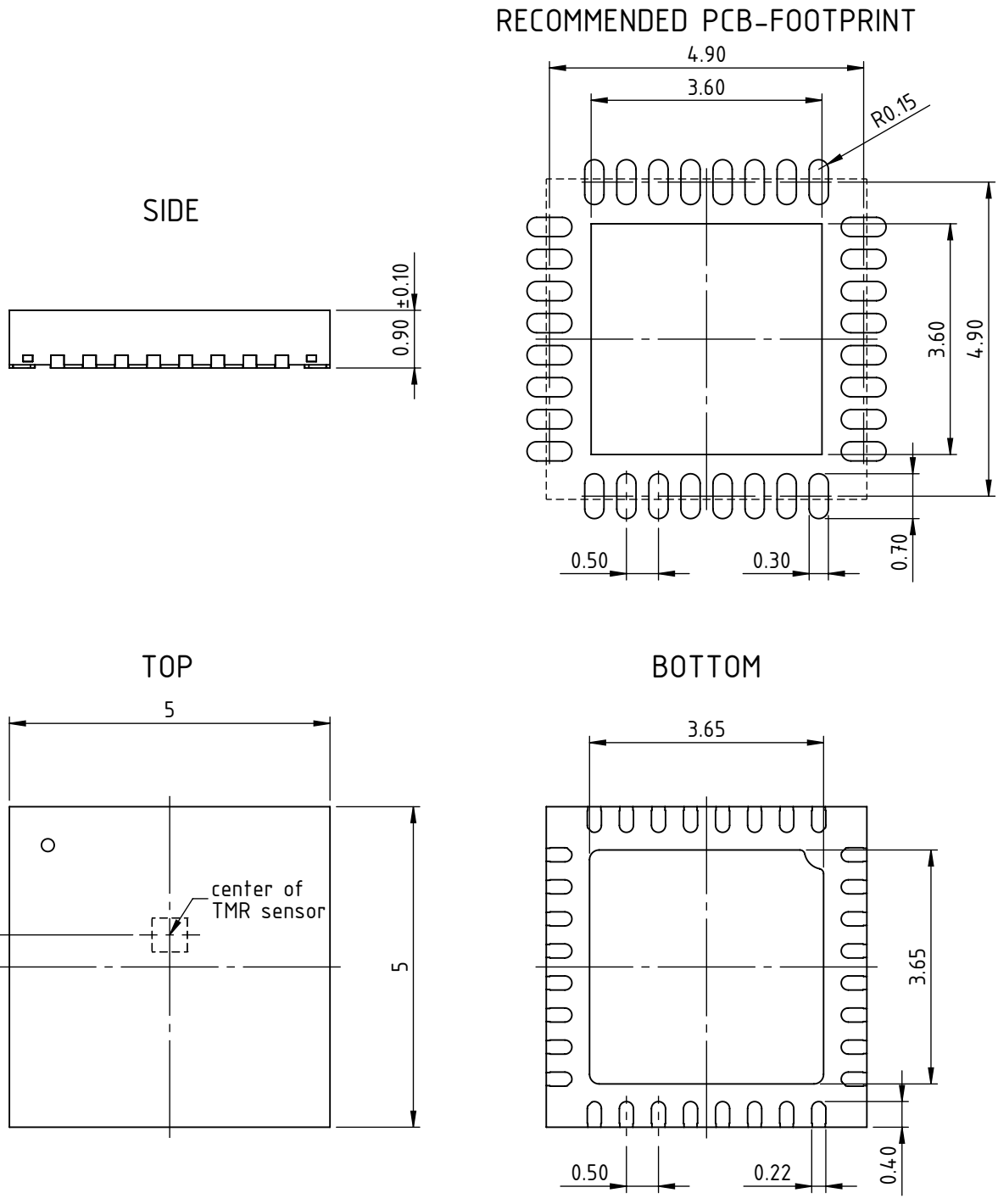
No.	Name	Function
1	VREF [1]	ADC Reference Output
2	VC [1]	Bias Output (VDD/2)
3	reserved [3]	
4	reserved [3]	
5	NPRE [4]	BiSS Position Preset Input
6	NRST [4]	Reset Input (low active)
7	NCLB [4]	Auto-Calib. Input (low active)
8	NERR [4]	Error Output (low active)

PIN FUNCTIONS

No.	Name	Function
9	Z/W	Incremental Output
10	SLI	BiSS Interface, Data Input
11	GND1	Digital Ground
12	B/V	Incremental Output, or MTDAT
13	SLO	BiSS Interface, Data Output
14	VDD1	+3.3 V Digital Supply Input
15	A/U	Incremental Output, or MTCLK
16	MAI	BiSS Interface, Clock Input
17	VDD2	+3.3 V Digital Supply Input
18	n.c. [2]	
19	GND2	Digital Ground
20	SO [5]	SPI Slave Output (Master Input)
21	SI [5]	SPI Slave Input (Master Output)
22	SCLK [5]	SPI Clock Input
23	NCS [4]	SPI Slave Select Input (low active)
24	reserved [6]	
25	n.c.	
26	n.c.	
27	AVDD	+3.3 V Analog Supply Input
28	reserved [7]	
29	n.c.	
30	AGND	Analog Ground
31	reserved [7]	
32	n.c.	
	BP [8]	Backside Paddle

IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes), <D-CODE> = date code (subject to changes);
[1] Pin must be decoupled with 100 nF to AGND. Do not inject noise.
[2] n.c. – pin is not connected.
[3] Pin must be connected to ground.
[4] Connect to +3.3 V via 10 kΩ resistor if not used. Do not allow to float.
[5] Connect to ground via 10 kΩ resistor if not used. Do not allow to float.
[6] Pin must be connected to +3.3 V.
[7] Do not wire this pin.
[8] Must be connected to a ground plane at AGND potential. Can also be used to connect GND1 and GND2.

PACKAGE DIMENSIONS QFN32 5 mm x 5 mm



All dimensions given in mm.
General tolerances of form and position according to JEDEC MO-220.
Tolerance of sensor pattern: ±0.10mm / ±1° (with respect to center of backside pad).

drb_qfn32-5x5-6_tw39_pack_1, 10:1

The magnet must be centered over the TMR sensor element, which is offset by 0.5 mm from the geometric center of the chip (see drawing above).

ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these values damage may occur.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	xVDD	Voltage at AVDD, VDD1, and VDD2	Referenced to xGND (AGND, GND1, and GND2 respectively)	–0.3	4.1	V
G002	Vpin	Pin Voltage at any pin	Referenced to xGND	–0.3	AVDD + 0.3	V
G003	Iin()	Input Current into any pin		–2	2	mA
G004	Iout()	Output Current	Single output pin loaded	–10	10	mA
G005	Bmax	Magnetic Flux Density			180	mT
G006	Vesd1	ESD Susceptibility	HBM, 100 pF discharged through 1.5 kΩ		2	kV
G007	Tj	Junction Temperature		–40	125	°C

THERMAL DATA

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range		–40		125	°C
T02	Rthja	Thermal Resistance Chip to Ambient	QFN32-5x5 surface mounted to PCB according to JEDEC 51		40		K/W
T03	Ts	Storage Temperature		–40		125	°C

All voltages are referenced to pin AGND unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating conditions: xVDD = 3.1...3.6 V, Tj = –40...+125 °C, reference point AGND unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	xVDD	Permissible Supply Voltage	(all supply pins linked)	3.1		3.6	V
002	I_{xVDD}	Total Supply Current	xVDD = 3.3 V, outputs unloaded		30	42	mA
003	I_{RST}	Reset Current	NRST pulled low after xVDD ramp up		250		µA
004	VDDon	Power-On/Off Threshold	NRST tied to DVDD	2.5	2.7	3.0	V
005	VDDoff	Undervoltage Reset Threshold	Decreasing voltage xVDD; NRST tied to DVDD	2.5		3.0	V
006	tstart	Startup Time	EEPROM configuration valid			10	ms
Magnetic Input							
101	Bext	Magnetic Flux Density	Field direction coplanar to chip (x-y plane) Recommended Tolerated maximum	30	60	80 160	mT mT mT
102	Dmag	Recommended Diameter of Magnet	Magnet thickness 2.5 mm	6			mm
103	zdis	Operating Distance of Magnet to Top of Package	for angle accuracy ≥ 10 bit; magnet ⌀ 9 mm magnet ⌀ 14 mm		0.5 1.0		mm mm
104	xdis	Permissible Lateral Displacement of Magnet Axis to Center of Sensor	for angle accuracy ≥ 10 bit; magnet ⌀ 9 mm magnet ⌀ 14 mm		 0.25 0.5		 mm mm
105	xpac	Sensor Placement vs. Center of Package		-0.2		0.2	mm
106	ϕpac	Zero Angle vs. Package Axis	Shipping state, uncalibrated	-2		2	DEG
107	fin()	Magnet Field Rotation Frequency		0		6	kHz
Converter Performance							
201	INL	Integral Nonlinearity	Refer to Figure 1, magnetic input according to 101 cf; settled error correction On power up, with OEM calibration		± 0.15	 ± 0.5	° °
202	DNL	Differential Nonlinearity	Refer to Figure 1; at 10,000 AB pulses		± 0.002		°
204	RESnf	Noise-free Resolution	deviation ±3σ, bandwidth 100 kHz		13.2		bit
205	Nrms	Angle Noise	deviation ±1σ		0.006		°
Incremental Outputs: A/U, B/V, Z/W							
301	Vs()hi	Saturation Voltage Hi	Vs()hi = VDD1 - V(); I() = -4 mA			0.7	V
302	Vs()lo	Saturation Voltage Lo	I() = 4 mA			0.7	V
303	Isc()hi	Short-Circuit Current Hi	Pin shorted to GND1	–30			mA
304	Isc()lo	Short-Circuit Current Lo	Pin shorted to VDD1			30	mA
305	tr()	Rise Time	xVDD = 3.3 V, CL = 50 pF, 10% → 90% VDD			20	ns
306	tf()	Fall Time	xVDD = 3.3 V, CL = 50 pF, 10% → 90% VDD			20	ns
307	t_{AB}	Output Phase A vs. B	Refer to Figure 2		25		%
308	t_{whi}	Duty Cycle at Output A, B	Refer to Figure 2		50		%
309	AArel	Relative Angle Accuracy	Refer to Figure 2, at up to 2500 cpr		2		%
310	t_{MTD}	Minimum Edge Distance A to B	Refer to Figure 2; ABLIMIT = 0 ABLIMIT = 24	1/fosc	 20 500		ns ns ns
311	fc()	Clock Frequency at MTCLK	Multiturn function enabled: A/U = MTCLK		150		kHz
BiSS Interface: MAI, SLO, SLI							
401	Vt()hi	Input Threshold Hi at MAI, SLI				1.9	V
402	Vt()lo	Input Threshold Lo at MAI, SLI		0.8			V
403	Vs()hi	Saturation Voltage Hi at SLO	Vs()hi = VDD1 - V(); I() = -4 mA			0.7	V
404	Vs()lo	Saturation Voltage Lo at SLO	I() = 4 mA			0.7	V
405	Isc()hi	Short-Circuit Current Hi at SLO	Pin shorted to GND1	–30			mA
406	Isc()lo	Short-Circuit Current Lo at SLO	Pin shorted to VDD1			30	mA
407	tr()	Rise Time at SLO	xVDD = 3.3 V, CL = 50 pF, 10% → 90% VDD			20	ns
408	tf()	Fall Time st SLO	xVDD = 3.3 V, CL = 50 pF, 10% → 90% VDD			20	ns

ELECTRICAL CHARACTERISTICS

Operating conditions: xVDD = 3.1...3.6 V, Tj = –40...+125 °C, reference point AGND unless otherwise stated.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
409	fclk()	Permissible Clock Frequency at MAI	BiSS SSI SSI after request time t_{RQ}			10 1 4	MHz MHz MHz
410	t_{RQ}	Request Time at MAI	Only for SSI output, see Fig.3		24 / fosc		
411	t_{out}()	Slave Timeout at SLO	See Figure 5; BiSS_CFG0.at = 0 (fixed) BiSS_CFG0.at = 1 (adaptive)	 8 / fosc	1024 / fosc t_{init} + 4 / fosc	 1024 / fosc	
SPI Interface: SI, SCLK, NCS, SO							
501	Vt()hi	Input Logic Threshold Hi at SI, SCLK, NCS				1.9	V
502	Vt()lo	Input Logic Threshold Lo at SI, SCLK, NCS		0.8			V
503	Ilk()	Input Leakage Current at SI, SCLK, NCS				±50	nA
504	f(SCLK)	Permissible SPI Clock Frequency at SCLK				20	MHz
505	Vs()hi	Saturation Voltage Hi at SO	Vs()hi = VDD1 - V(); I() = -4 mA			0.7	V
506	Vs()lo	Saturation Voltage Lo at SO	I() = 4 mA			0.7	V
507	tr()	Rise Time at SO	xVDD = 3.3 V, CL = 50 pF, 10% → 90% VDD			20	ns
508	tf()	Fall Time at SO	xVDD = 3.3 V, CL = 50 pF, 10% → 90% VDD			20	ns
Error Input/Output: NERR							
601	Vt()hi	Input Threshold Hi				1.9	V
602	Vt()lo	Input Threshold Lo		0.8			V
603	Vs()lo	Saturation Voltage Lo	I() = 4 mA (open drain)			0.7	V
604	Isc()lo	Short-Circuit Current Lo	NERR pulls low, short to VDD1			30	mA
Control Inputs: NRST, NPRE, NCLB							
701	Vt()hi	Input Logic Threshold Hi				1.9	V
702	Vt()lo	Input Logic Threshold Lo		0.8			V
703	Ilk()	Input Leakage Current			±50		nA
Bias Outputs: VC, VREF							
801	VC	Bias Voltage VC	I(VC) = 0		50		%AVDD
802	dVREF	ADC Reference Output VREF	dVREF = V(VREF) - V(VC); I(VREF) = 0	–1.1	–1	–0.9	V
Internal Oscillator							
A01	fosc	Oscillator Frequency	Tj = 27 °C		50		MHz
A02	TCf	Temperature Coefficient			225		ppm/K
Temperature Sensor							
B01	Tacc	Temperature Sensor Accuracy	Tj = 100 °C		±2		°C
Internal EEPROM							
C01	Nwrite	Permissible Number of Write Cycles	Tj = –40 °C...85 °C	1000			
C02	Tjw	Write Temperature Range		–40		85	°C
C03	Tjr	Read Temperature Range		–40		125	°C
C04	DRTraw	Raw Data Retention Time		10			years
C05	DRTact	Actual Data Retention Time (with error correction)	Tj = 85 °C	50			years

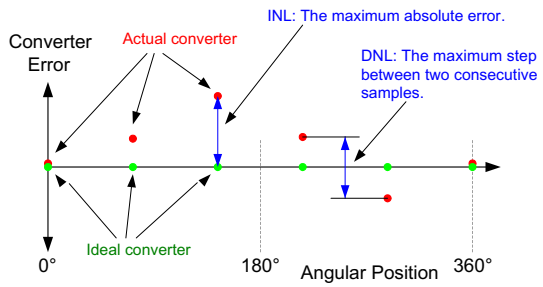


Figure 1: Definition of absolute converter error (INL) and differential nonlinearity error (DNL)

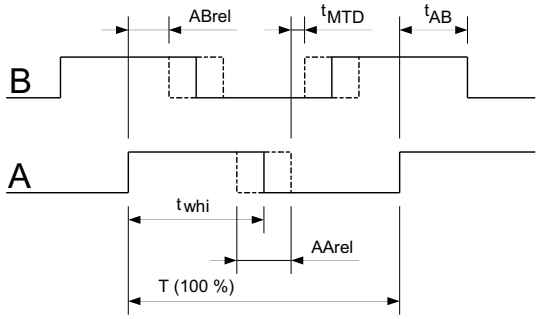


Figure 2: Description of AB output signals

OPERATING REQUIREMENTS: BiSS Interface

Operating conditions: xVDD = +3.1...+3.6 V, xGND = 0 V, Tj = –40...125 °C

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
SSI protocol						
I001	t_C	Permissible Clock Period	With t_{RQ} according to I004	250		ns
I002	t_{L1}	Clock Signal Hi-Level Duration		125	t_{out}	ns
I003	t_{L2}	Clock Signal Lo-Level Duration		125	t_{out}	ns
I004	t_{RQ}	Request Time	Clock low-level at MAI due to 410	500		ns
I005	t_{P3}	Output Propagation Delay			50	ns
I006	t_{out}	Slave Timeout		see Elec. Char. 411		
I007	t_{frame}	Permissible Frame Repetition		*	indefinite	
BiSS C protocol						
I008	t_C	Permissible Clock Period		100		ns
I009	t_{L1}	Clock Signal Hi-Level Duration		50	t_{out}	ns
I010	t_{L2}	Clock Signal Lo-Level Duration		50	t_{out}	ns
I011	t_{busy}	Minimum Data Output Delay		2 t_C		
I012	t_{busy}	Maximum Data Output Delay			400	ns
I013	t_{P3}	Output Propagation Delay			50	ns
I014	t_{out}	Slave Timeout		see Elec. Char. 411		
I015	t_{S1}	Setup Time: SLI stable before MA hi → lo		25		ns
I016	t_{H1}	Hold Time: SLI stable after MAI hi → lo		10		ns
I017	t_{frame}	Permissible Frame Repetition		*	indefinite	

Note: * Allow t_{out} to elapse.

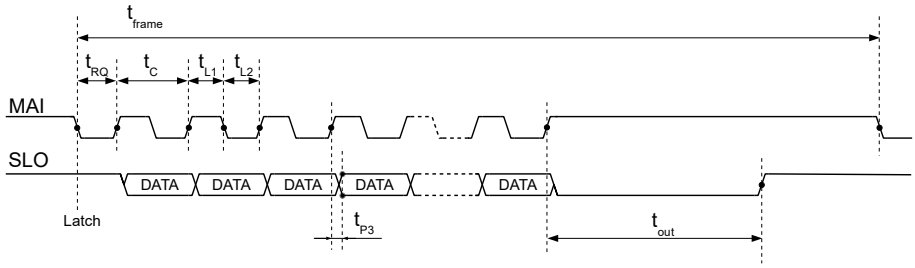


Figure 3: SSI protocol timing

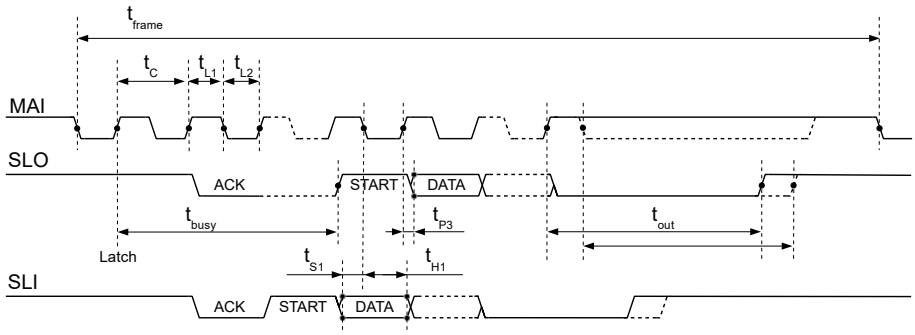


Figure 4: BiSS protocol timing

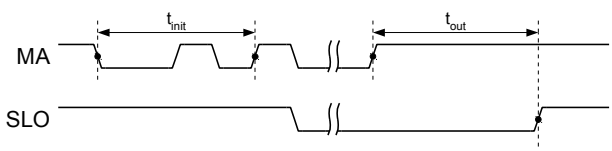


Figure 5: BiSS slave timeout

OPERATING REQUIREMENTS: ADI Interface

Operating conditions: AVDD = DVDD = IOVDD = +3.1...+3.6 V, AVSS = DVSS = IOVSS = 0 V, Tj = –40...125 °C

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
BiSS Protocol (ADI_CFG.biss = 1)						
I101	t_C	Clock Period	ADI_CFG.freq = 0 ADI_CFG.freq = 1	5.9 0.59	7.7 0.77	µs µs
I102	t_{L1}, t_{L2}	Clock Signal Hi/Lo Level Duration		50		% t_C
I103	t_{busy}	Permissible Processing Time	relative to clock period		∞	% t_C
I104	t_{P0}	Permissible Propagation Delay (Line Delay Compensation)	not supported (data is captured on next rising clock edge)	0		ns
I105	Δt_P	Permissible Propagation Delay Variance	not supported (refer to t_S and t_H)			% t_C
I106	t_S	Setup Time: Data stable before clock edge lo → hi	without line delay compensation (t_{P0} = 0)	100		ns
I107	t_H	Hold Time: Data stable after clock edge lo → hi	without line delay compensation (t_{P0} = 0)	0		ns
I108	t_{out}	Permissible Slave Timeout		t_C		µs
I109	t_{frame}	Clock Frame Repetition	Note: This value can vary during operation.	1	3	ms
SSI Protocol (ADI_CFG.biss = 0)						
I110	t_C	Clock Period	ADI_CFG.freq = 0 ADI_CFG.freq = 1	5.9 0.59	7.7 0.77	µs µs
I111	t_{L1}, t_{L2}	Clock Signal Hi/Lo Level Duration		50		% t_C
I112	t_S	Setup Time: Data stable before clock edge lo → hi		100		ns
I113	t_H	Hold Time: Data stable after clock edge lo → hi		0		ns
I114	t_{out}	Permissible Slave Timeout		t_C		µs
I115	t_{frame}	Clock Frame Repetition	Note: This value can vary unpredictably during operation.	1	3	ms

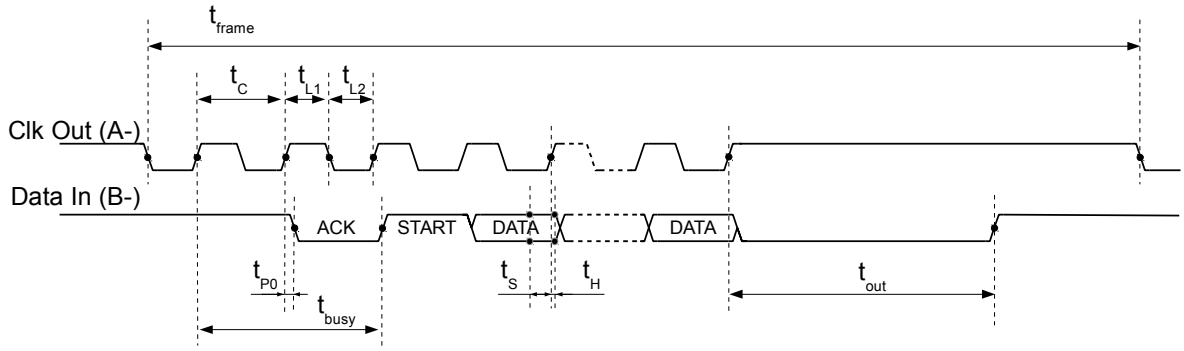


Figure 6: ADI timing with BiSS protocol

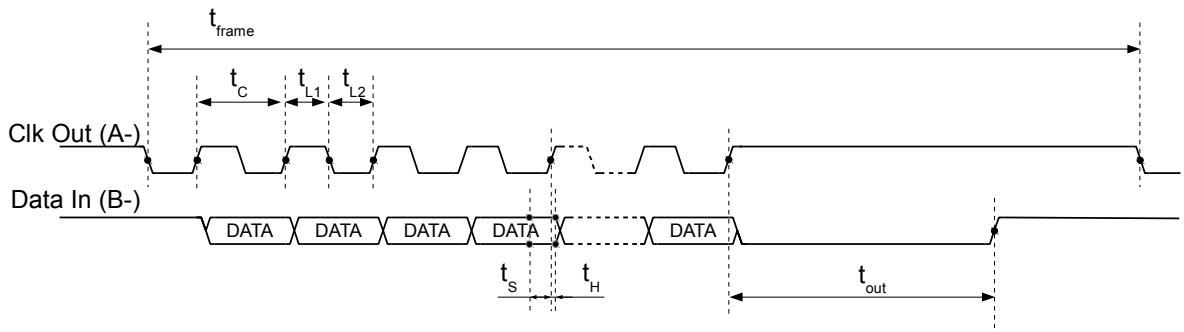


Figure 7: ADI timing with SSI protocol

OPERATING REQUIREMENTS: SPI Interface

Operating conditions: xVDD = +3.1...+3.6 V, xGND = 0 V, Tj = –40...125 °C

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
SPI Interface Timing						
I201	t_{C1}	Permissible Clock Cycle Time	Clock frequency according to 504	50		ns
I202	t_{D1}	Clock Signal Lo Level Duration		15		ns
I203	t_{D2}	Clock Signal Hi Level Duration		15		ns
I204	t_{S1}	Setup Time: NCS lo before SCLK lo → hi		80		ns
I205	t_{H1}	Hold Time: NCS lo after SCLK hi → lo		50		ns
I206	t_{W1}	Wait Time: between NCS lo → hi and NCS hi → lo		200		ns
I207	t_{S2}	Setup Time: SI stable before SCLK lo → hi		5		ns
I208	t_{H2}	Hold Time: SI stable after SCLK lo → hi		10		ns
I209	t_{P1}	Propagation Delay: SO stable after NCS hi → lo			60	ns
I210	t_{P2}	Propagation Delay: SO high impedance after NCS lo → hi			25	ns
I211	t_{P3}	Propagation Delay: SO stable after SCLK hi → lo			20	ns

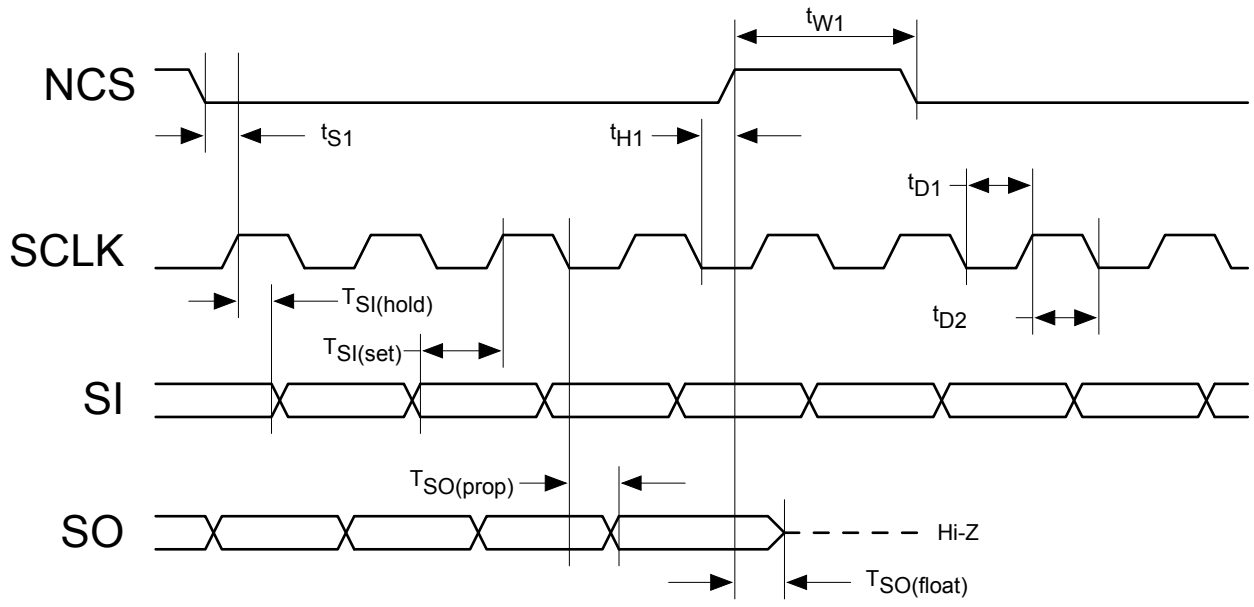


Figure 8: SPI Timing

ELECTRICAL CONNECTIONS

The basic electrical connections for an absolute single-turn stand-alone application using BiSS are shown in Figure 9. An external RS422-compatible driver/receiver, such as the iC-HF, and a 5 V-to-3.3 V level shifter, such as the TXS0104E, are required.

See the iC-HF data sheet for more information.

Alternatively, resistive voltage dividers can be used instead of an explicit level shifter chip. In this case, values of 470 Ω and 560 Ω are recommended to drive MAI and SLI. This will add 15 mA of current consumption.

Note: The input voltages must not exceed the chip's supply voltage (3.3 V).

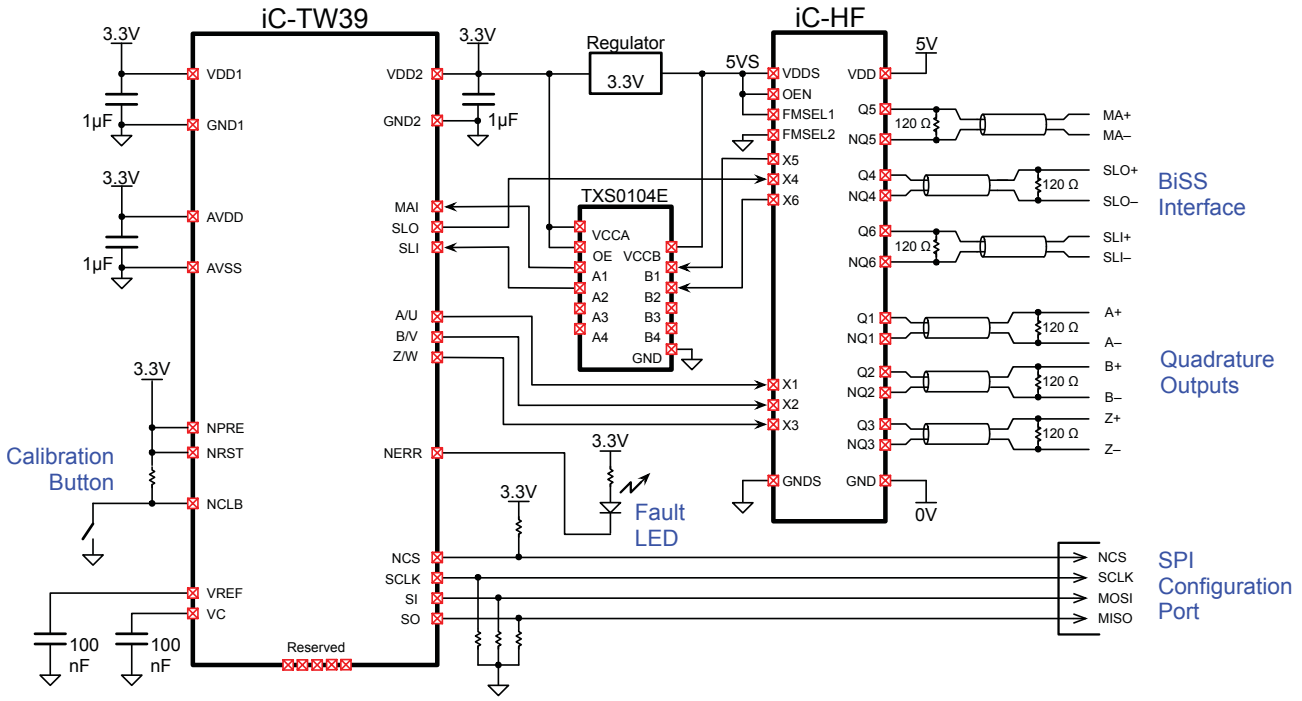


Figure 9: Typical Electrical Connections for Absolute BiSS Stand-Alone Application featuring additional incremental quadrature outputs.
Note: The circuit diagram is a basic application example only. Other components may be necessary, but are omitted for clarity. Please refer to the component specific data sheets.

Power and Ground

It is sufficient to connect all three supply pins to the same low-impedance power source, preferably an on-board voltage regulator. Likewise, the three ground pins can usually be connected to the same solid ground plane on the PC board. In all cases, each power pin should have a dedicated 1 µF decoupling capacitor placed as close to the iC-TW39 as possible.

Reference Outputs

The reference outputs VREF and VC must each be decoupled to ground with separate 100 nF capacitors placed as close to the iC-TW39 as possible. Do not apply any load to these pins.

NCLB Input

The active-low NCLB input is used to activate the auto-calibration feature of the iC-TW39. A push-button and pull-up resistor can be connected to this input as shown for easy manual calibration. If push-button calibration is not required, NCLB should be connected to 3.3 V to avoid spurious calibration.

NRST Input

The iC-TW39 contains a built-in power-on-reset (POR) circuit that controls the safe startup of the device. In most applications, no external components are required and NRST can be connected directly to 3.3 V.

However, to extend the device reset in case of slow-rising supplies, it is recommended to provide an RC network on the PC board (see Figure 10) and only populate the capacitor if required.

To reduce the power consumption in battery-powered applications, the NRST input is best controlled by the host. The following MCU controlled sequence should be followed:
1. Set NRST = 0 and ramp up xVDD.
2. Set NRST = 1 for at least 10 µs.
3. Set NRST = 0 to enter low power mode.

Refer to Elec. Char. 003, page 8, for current consumption. The restart after NRST = 1 takes up to 10 ms, see Elec. Char. 006.

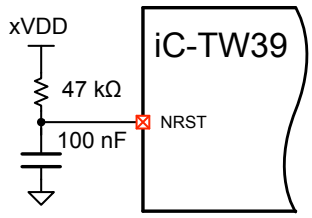


Figure 10: NRST Connection

NPRE Input
The NPRE input enables a pin-triggered zeroing for the BiSS/SSI interface data output. Refer to section Position Preset for further information.

To prevent input floating, NPRE may be wired to either ground or 3.3 V when the pin function is not required and disabled by programming.

NERR
The open-drain NERR pin functions as an active-low fault output. It can be used to directly drive an LED with an appropriate current-limiting resistor for fault indication.

SPI Port
The iC-TW39 provides a standard SPI (Serial Peripheral Interface) slave port that can be used for device configuration and communication with a host processor. Refer to the Programmer's Reference for information. Connect the SPI port pins to the host processor as shown in Figure 11.

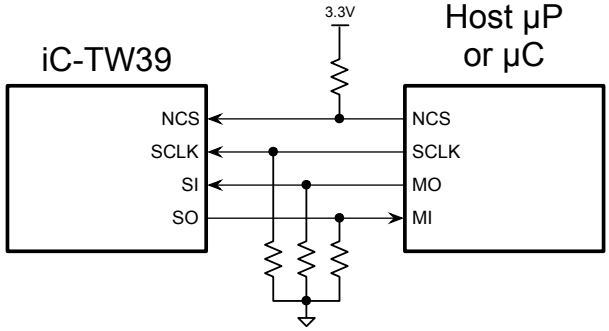


Figure 11: SPI Port Connection

If the host processor or microcontroller can be disconnected, the SPI port pins must be pulled up or down as shown in Figure 11. Do not allow any of the SPI port pins to float.

Reserved Pins
Each reserved pin must be wired to either ground or VDD according to the pin configuration description (see page 5).

DEVICE FUNCTIONS

The advanced iC-TW39 angle sensor utilizes Tunnel Magneto Resistor bridges along with digital signal processing for interpolation, filtering, error correction, and monitoring operation.

The chip's permanent Auto adaption maintains optimal offset, amplitude balance, and phase compensation values for the TMR's sin/cos signals during operation to ensure maximum interpolation accuracy and lowest jitter under all operating conditions.

Traditional encoder quadrature ABZ signals are available as single-ended outputs. The ABZ output resolution (edges or AB cycles per revolution) is programmable independently of the BiSS output resolution.

The ABZ outputs incorporate a programmable AB output frequency limiter that guarantees a minimum separation time between AB edges. This is useful to avoid counting errors with PLCs or counters with input frequency limits less than the 12.5 MHz maximum AB output frequency of the iC-TW39.

When the AB output frequency is being limited, the AB outputs lag behind the input angle. If this condition is temporary or transient, the AB outputs catch up when the limiter is no longer active. If this condition persists, however, a fatal fault is generated and the iC-TW39 stops its angle conversion and tri-states the ABZ/UVW outputs. The AB output frequency limiter can be programmed to activate NERR.

3-phase UVW signals for commutation of brushless motors with up to 64 poles (32 pole pairs) per revolution are also available over the incremental outputs.

The BiSS slave interface provides BiSS C-Mode bidirectional communication of output angle (with independently programmable resolution), revolution count, and configuration data. Encoder Profiles 3 and 3S (Safety) are implemented in the iC-TW39.

Note that the execution of BiSS protocol commands is not featured. In hosted applications, user-defined system commands could be implemented on the microprocessor and called up by the BiSS control data communication.

The SPI port is available for use by an external host processor for initial calibration or general communication.

The iC-TW39 provides comprehensive monitoring functions for status and faults, chip temperature and sin/cos input signal quality.

The status/fault monitor monitors 13 internal conditions, each of which can be individually configured to activate the fault output, pin NERR, as well as BiSS error and warning bits to notify an external system during operation. The active-low NERR output can be used to directly drive an LED. In addition, real-time and latched status information is available over the SPI and BiSS interfaces.

The iC-TW39 incorporates an on-chip temperature sensor. The temperature monitor can provide real-time chip temperature data to a host processor or BiSS master. The temperature monitor can be configured to activate a status bit when the chip temperature exceeds a programmable limit. This condition can also activate NERR.

The sensor amplitude monitor continuously monitors the sensor's sin/cos vector amplitude by calculating the quantity $\sqrt{sin^2 + cos^2}$. If the vector amplitude is outside configured limits, a status bit is activated and the fault output can be activated.

The excessive error monitor continuously calculates the residual offset, balance, and phase error of the corrected sin/cos signals. These residues represent the uncorrected signal error and are typically zero (or near zero) assuming the sensor is properly positioned to the magnet. If any of the error residues exceeds configured limits, a status bit is set and the fault output can be activated.

The excessive adaption monitor continuously compares the current offset, balance, and phase correction parameter values to baseline values stored in the EEPROM during device configuration. If any of the correction values deviate from the base values (due to auto adaption) by more than the configured limits, a status bit is set and the fault output can be activated.

Auto calibration is used at initial device commissioning to automatically determine gain, offset, channel balance, and phase compensation values for the sin/cos signals derived from the TMR angle sensor.

Auto calibration is initiated using the NCLB input pin or via a serial command. Calibrated values are stored in the internal EEPROM for use on subsequent startups.

Device and chip identification is provided in the form of a unique factory-programmed chip serial number as well as a chip ID and revision code. In BiSS applications, user-programmable manufacturer ID, product ID, device serial number, and production date are available.

The iC-TW39 incorporates an internal write-protected EEPROM to store configuration and initial calibration data for use at startup. In addition to a standard checksum on the EEPROM data, sophisticated data encoding allows detection and correction of single-bit errors and detection of two-bit errors for enhanced application security. The EEPROM can be unlocked using the SPI or BiSS interface.

Output Modes

The iC-TW39 features different output modes. All signals are available as single-ended standard CMOS outputs or inputs respectively. Connection of external line drivers/transceivers must be used to achieve 5 V compatibility.

In combination with the BiSS Interface, one of four different output modes can be selected as shown in Table 1. If using SSI, refer to Table 2.

BiSS Output Modes							
MAIN_CFG .nio	Mode	I/O Pin Signals					
		MAI	SLO	SLI	A/U	B/V	Z/W
0	BiSS Only	MAI	SLO	SLI	Hi-Z	Hi-Z	Hi-Z
1	BiSS/ABZ	MAI	SLO	SLI	A+	B+	Z+
2	BiSS/UVW	MAI	SLO	SLI	U+	V+	W+
(3 - optional)	(BiSS/ADI)	MAI	SLO	SLI	Clk Out	Data In	I/O

Table 1: BiSS Output Modes

SSI Output Modes							
MAIN_CFG .nio	Mode	I/O Pin Signals					
		MAI	SLO	SLI	A/U	B/V	Z/W
0	SSI Only	CLK	Data	Hi-Z	Hi-Z	Hi-Z	Low
1	SSI/ABZ	CLK	Data	Hi-Z	A+	B+	Z+
2	SSI/UVW	CLK	Data	Hi-Z	U+	V+	W+
(3 - optional)	(SSI/ADI)	CLK	Data	Hi-Z	Clk Out	Data In	I/O

Table 2: SSI Output Modes

All **ABZ output modes** require additional configuration for output polarity, direction, startup, etc. as explained in ABZ OUTPUT on page 20.

All **UVW output modes** require additional configuration for output polarity, direction, etc. as explained in UVW OUTPUT on page 22.

BiSS output modes use the MAI, SLO, and SLI pin for the BiSS signals, whereas **SSI output modes** use only MAI for Clock In and SLO for Data Out. The SLI pin has no function in this case. The signals should be connected to a suitable RS422-compatible driver/receiver as shown in Figure 9.

All BiSS and SSI output modes require additional configuration as explained in BISS/SSI INTERFACE on page 24.

ANGLE PROCESSOR

Parameter	Default	Description	Comments
START.wait	0	Startup Wait Time (default = 0 ms)	
	1...6	1 ms, 3 ms, 10 ms, 30 ms, 100 ms, 300 ms	Optional, e.g. when using the ADI.
Counter			
GB_CFG.rclen	0	Revolution Counter Length = 0 bits	
	2	Revolution Counter Length = 8 bits	
	3	Revolution Counter Length = 12 bits	
	4	Revolution Counter Length = 16 bits	
	6	Revolution Counter Length = 24 bits	Allowed maximum.
Hysteresis			
HYST	43	Hysteresis, recommended minimum (7164 interpolated angle increments)	0.0384° = 140" ensures flicker-free AB output.
range	0...71	Minimum (zero) ... allowed maximum (4.92°)	

Table 3: <Angle Processor> Parameters

GB_CFG.rclen determines the length (number of bits) of the revolution counter.

The actual number of bits used for the revolution counter, *rcbits*, is calculated as

$$rcbits = 4 \cdot \text{GB\_CFG.rclen}$$

HYST determines the hysteresis of the interpolated angle. Its register value is semi-logarithmic to provide a wide range of values for different applications. The actual hysteresis in output degrees, *hyst*, is calculated as

$$hyst[^\circ] = \pm\frac{360^\circ}{2^{26}} \cdot (\text{HYST}[1:0] + 4) \cdot 2^{\text{HYST}[6:2]} - 4$$

The equivalent hysteresis in output AB edges, UVW edges, or BiSS LSBs is a function of the output resolution as determined by ABZ_RES, UVW_CFG.pairs, and BISS_RES registers respectively.

Startup

The startup sequence (see Figure 12) is initiated when power is applied to the iC-TW39. A POR circuit monitors the supply voltage and waits until it has reached 2.7...2.9 V. The iC-TW39 then reads the configuration data from its EEPROM and halts for a programmable wait time configured by **START.wait**.

Note that the chip's VDD supply must be above the specified minimum (see Elec. Char. item 001) at the end of the startup wait time. If any faults are detected during the startup cycle, the iC-TW39 does not enable any outputs but goes into an idle state with NERR asserted.

The startup sequence can also be initiated by external hardware connected to the NRST input, or by a command via the BiSS or SPI interfaces.

During a normal startup and no active faults, **STAT_START** activates in order as each startup state is completed. Thus, a successful startup is finally indicated by STAT_START = 0x000F (see Table 4 for overview).

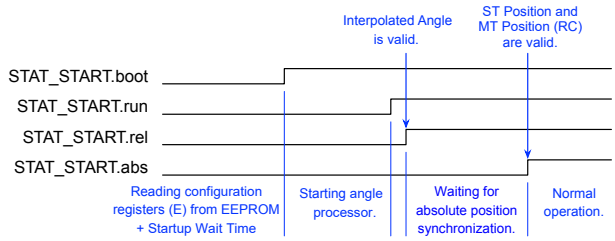


Figure 12: Normal Startup with No Active Faults.

STAT_START.boot = 1 when the iC-TW39 has completed its bootup state and is ready for communication via the BiSS or SPI interfaces. During the bootup state (STAT_START.boot = 0), the NERR pin is active (low), and the iC-TW39 attempts to read its configuration parameters and correction values from the internal EEPROM.

When this is complete and there are no fatal faults (STAT_FATAL = 0), STAT_START.boot changes to 1, and the NERR pin is deactivated. STAT_START.boot also changes to 1 at the end of bootup even when fatal faults come active, but the startup sequence does not advance to the run state and the NERR pin remains active (low).

During the run state of the startup sequence, STAT_START.run = 0, the iC-TW39 starts the angle

processing and interpolation. When this is complete, STAT_START.run changes to 1.

If the optional absolute data interface (ADI) is not in use to process MT data, STAT_START.abs = 1 is reached simultaneously with STAT_START.rel = 1, and the ABZ or UVW outputs are enabled.

If the optional ADI is used, STAT_START.rel = 1 as soon as the Interpolated Angle is valid, i.e. when the "relative" position has been established. This happens almost simultaneously with STAT_START.run = 1. After the first valid absolute position read over the ADI occurs, STAT_START.abs = 1 is reached and the ABZ or UVW outputs are enabled.

Parameter	Value	Description	Comments
STAT_START		Startup Status Register	
	0b 0001	Bootup complete	STAT_START.boot = 1
	0b 0011	Angle processor running	STAT_START.run = 1
	0b 0111	Interpolated angle (IA) valid	STAT_START.rel = 1
	0b 1111	Absolute position (IA, RC) valid	STAT_START.abs = 1

Table 4: <Startup> . Startup sequence on power up and after releasing NRST to high.

ABZ OUTPUT

Parameter	Default	Description	Comments
ABZ Resolution			
ABZ_RES range	4 096 4...262 144	1 024 AB cycles per revolution	Factory default. Up to 65 536 AB cycles per rev.
AB_LIMIT range	1 0...1023	AB Output Frequency Limit = 6.25 MHz	 Up to 12.5 MHz maximum (edge rate 20 ns)
ABZ_CFG.zwidth	0 1 2	Z Output Width = 1 AB incr. (90° of an AB cycle) Z Output Width = 2 AB incr. (180° of an AB cycle) Z Output Width = 4 AB incr. (1 AB cycle)	Factory default.
ABZ_PH range	0 0...65535	ABZ Phase Shift = 0°	 Example: 32 768 = 180°
ABZ Output Configuration			
MAIN_CFG.nio	1	Function of Outputs: A/U, B/V, Z/W	1 = ABZ.
ABZ_CFG.apol ABZ_CFG.bpol ABZ_CFG.zpol ABZ_CFG.dir range	0 0 0 0 0, 1	Invert A polarity Invert B polarity Invert Z polarity Reverse counting direction 0 = normal, 1 = inverted / reversed	

Table 5: <ABZ> Parameters

ABZ Output Configuration
The ABZ outputs must be configured for resolution, polarity, direction of rotation, etc. to match the application requirements. Note that the configuration of ABZ_CFG is only effective in ABZ output mode (MAIN_CFG.nio = 1), otherwise it is ignored.

ABZ_RES determines the resolution of the AB outputs in edges (increments) per revolution. Any resolution between 4 and 262 144 (2^{18}) edges per revolution may be specified regardless of the resolution of the BiSS Interface. The AB output resolution in cycles per revolution is ABZ_RES/4.

AB_LIMIT is used to set the level of the AB output frequency limiter.

The actual AB output frequency limit, *fab*, is calculated as

$$fab\,[\mathrm{MHz}] = \frac{12.5\,\mathrm{MHz}}{(\mathrm{AB\_LIMIT} + 1)}$$

The equivalent minimum time between AB edges, *tedge*, is calculated as

$$tedge\,[\mathrm{ns}] = 20 \cdot (\mathrm{AB\_LIMIT} + 1)$$

The magnetic field input frequency, *finput*, that corresponds to the AB frequency limit is calculated as

$$finput\,[\mathrm{kHz}] = \frac{50\,000}{\mathrm{ABZ\_RES} \cdot (\mathrm{AB\_LIMIT} + 1)}$$

For example, if ABZ_RES = 40 000, and AB_LIMIT = 24,

$$fab\,[\mathrm{MHz}] = \frac{12.5\,\mathrm{MHz}}{(24 + 1)} = 0.5\,\mathrm{MHz}$$

and

$$finput\,[\mathrm{kHz}] = \frac{50\,000}{40\,000 \cdot (24 + 1)} = 0.05\,\mathrm{kHz}$$

In this case the maximum input speed calculates to 3,000 rpm (60 x 50 Hz). When the speed exceeds *finput*, the AB output position can no longer keep up with the sensor position and STAT_VAL.vlim = 1. In this case, the iC-TW39 keeps generating output pulses at the maximum AB frequency.

If this condition is temporary or transient, the AB outputs catch up when the input speed decreases. If this condition persists and the AB output position falls behind the input angle by 180°, the AB outputs are no longer valid (unexpected direction reversal) and a fatal fault is generated (STAT_VAL.lagfatl = 1).

ABZ_CFG.zwidth determines the width of the Z output.

ABZ_PH determines the position of the Z output relative to the magnetic field angle. The actual ABZ phase, *abzph*, in degrees is calculated as

$$abzph[^\circ] = \mathrm{ABZ\_PH} \cdot \frac{360^\circ}{65\,536}$$

If ABZ_PH is kept zeroed, the Z output signal appears when the orientation of the magnet field to the package of iC-TW39 is as shown in Figure 13.

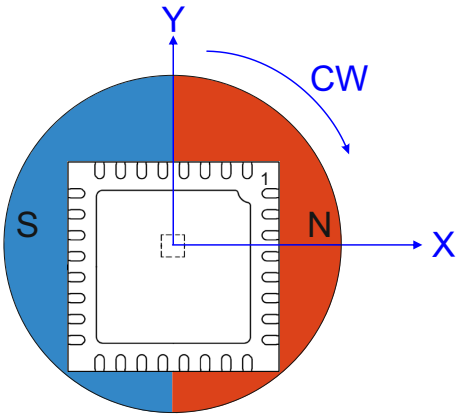


Figure 13: On-axis view (through IC backside) with magnet orientation for zero angle and Z output (ABZ_PH = 0). The interpolated angle increases with CW rotation.

ABZ_CFG.apol determines whether the polarity of the A output is normal or inverted. ABZ_CFG.apol also determines the state of the A output when the Z output is active.

ABZ_CFG.bpol determines whether the polarity of the B output is normal or inverted. ABZ_CFG.bpol also determines the state of the B output when the Z output is active.

ABZ_CFG.dir determines the counting direction of the AB outputs.

Note that setting ABZ_CFG.apol or ABZ_CFG.bpol (but not both) also reverses the counting direction of the AB outputs. In this case, invert ABZ_CFG.dir to restore the original AB counting direction. Setting both ABZ_CFG.apol and ABZ_CFG.bpol does not change the AB output counting direction.

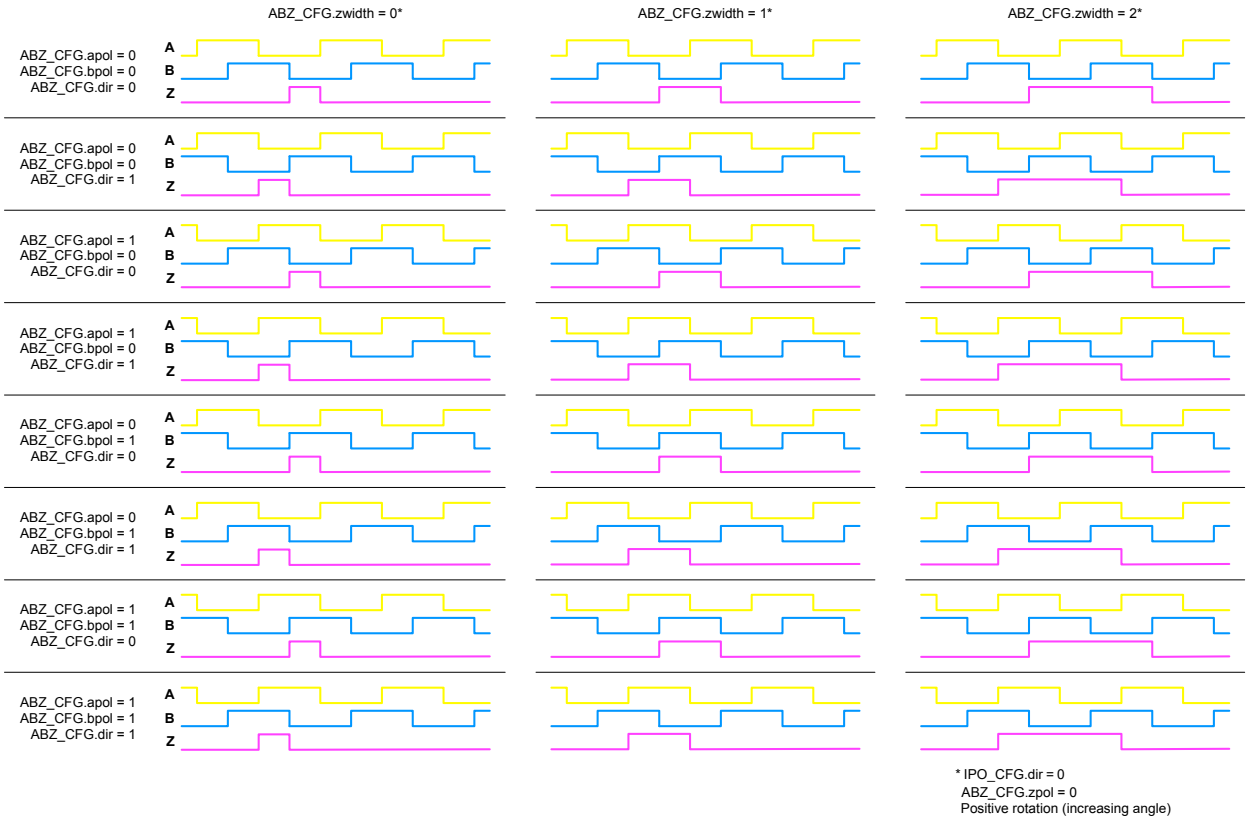


Figure 14: AB Output Polarity and Z Width

UVW OUTPUT

Parameter	Default	Description	Comments
UVW Resolution			
UVW_CFG.pairs range	1 0...31	UVW Pole Pairs = 1 UVW cycle per revolution	 0 = 32 cycles (maximum)
UVW_PH range	0 0...65535	UVW Phase Shift = 0 deg	 Example: 32 768 = 180°
UVW Output Configuration			
MAIN_CFG.nio	2	Function of Outputs: A/U, B/V, Z/W	2 = UVW.
UVW_CFG.pol UVW_CFG.dir range	0 0 0, 1	Invert UVW polarity UVW Rotation Direction = normal UVW sequence 0 = normal, 1 = inverted / reversed	

Table 6: <UVW> Parameters

UVW Output Configuration

The UVW outputs must be configured for resolution, polarity, direction of rotation, etc. to match the application requirements. The state of the UVW signals at a given position within a revolution is always the same after every startup.

UVW_CFG is used to set the polarity, direction, and resolution of the UVW outputs. It is only effective in UVW output mode (MAIN_CFG.nio = 2), otherwise it is ignored.

UVW_CFG.pairs determines the number of UVW cycles per revolution. It must be equal to the number of magnetic pole pairs of the motor being controlled.

UVW_PH determines the phase shift between the magnetic field angle (FA) and the start of the UVW cycle. The actual UVW phase, *uvwph*, in degrees is calculated as

$$uvwph[^\circ] = \text{UVW\_PH} \cdot \frac{360^\circ}{65\,536}$$

If UVW_PH is zero, the U output edge appears when the orientation of the magnet field to the package of iC-TW39 is as shown in Figure 13.

UVW_CFG.pol determines whether the polarity of the UVW outputs is normal or inverted. Note that setting UVW_CFG.pol shifts the phase of the UVW outputs by 180°.

UVW_CFG.dir determines the rotation direction (phase sequence) of the UVW outputs.

The effect of the UVW_CFG.dir and UVW_CFG.pol with positive magnetic field rotation (i.e. CCW in Figure 13) is shown in Figures 15 and 16.

Note: Always restart the interpolator (command 0x04) after any change to UVW_CFG or UVW_PH to ensure proper UVW output synchronization.

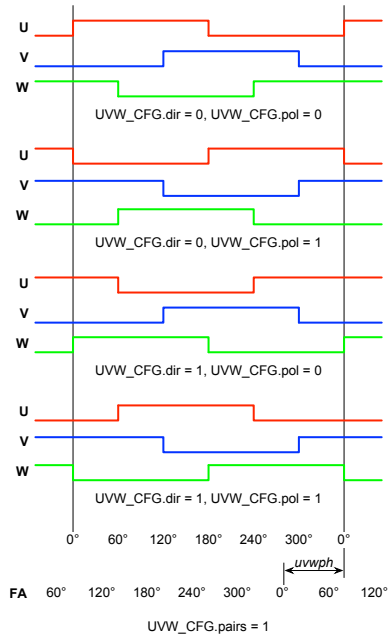


Figure 15: UVW Operation (2 Pole Motor)

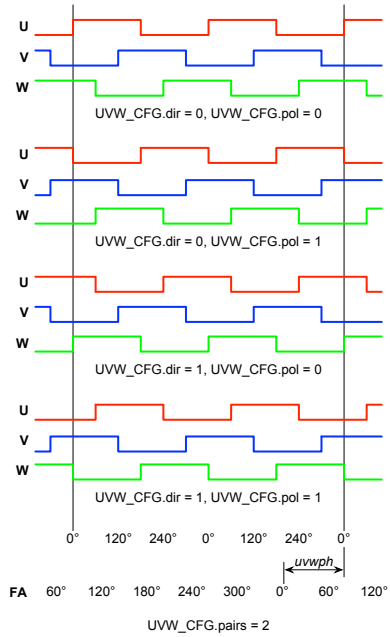


Figure 16: UVW Operation (4 Pole Motor)

ABZ + UVW OUTPUT

By pulling pin 24 low, the BiSS Interface can be disabled and switched to output incremental signals instead. This enables the output of ABZ signals together with UVW signals. In this case, the iC-TW39 must be configured via SPI.

Parameter	Default	Description	Comments
ABZ Output Configuration			
Pin 24 = Low		BiSS Interface disabled for ABZ output.	MAI = A, SLO = B, SLI = Z.
UVW Output Configuration			
MAIN_CFG.nio	2	Function of Outputs: A/U, B/V, Z/W	2 = UVW
ABZ and UVW Configuration			
Refer to Tables 5 and 6.			

Table 7: Configuration of Pure Incremental ABZ + UVW Output

BiSS/SSI INTERFACE

The BiSS/SSI slave interface in the iC-TW39 allows BiSS C-mode communication with a BiSS master for transmission of absolute position and control data, or SSI communication with an SSI master for transmission of absolute position data.

An external RS422-compatible line driver/receiver is generally required to provide differential signals as shown in Figure 9.

BiSS Communication

The iC-TW39 provides one channel of single-cycle sensor data (SCDS) in the SCD frame. This data consists of multiturn and singleturn position at programmable resolution with up to 50 bits maximum, two feedback bits, and a CRC value of 6 or 16 bits as specified by the BiSS Profile ID.

The multiturn position represents the counted revolutions and the singleturn position the interpolated angle.

The BiSS warning (nW) and error (nE) bits can be configured to activate in response to any selection of the iC-TW39's internal status conditions. The nE and nW bits can also be configured to automatically clear, in which case they are active for only one BiSS SCD frame. Finally, any fatal status condition automatically activates both bits.

Direct access to frequently used iC-TW39 registers and indirect access to all other registers is provided in the BiSS control data frame.

Note: iC-TW39 does not support BiSS protocol commands.

SSI Communication

The iC-TW39 provides one channel of single-cycle sensor data per frame. This data consists of multiturn and singleturn position at programmable resolution with up to 50 bits maximum. The multiturn position represents the counted revolutions and the singleturn position the interpolated angle. Error or CRC bits are not available.

Note: Blind register write capability is available in SSI mode to provide BiSS recovery.

Note: An active error mapped to the BiSS error bit by means of STAT_BE.xxx causes the data output SLO (B+) to show high permanently in SSI mode until the error is removed.

Interface Configuration

The registers used by the BiSS/SSI Interface are shown in Table 8.

Parameter	Value	Description	Comments
BiSS General			
BISS_CFG0.ssi	0, 1	Protocol: 0 = BiSS, 1 = SSI	
BISS_CFG0.at	0, 1	BiSS Timeout: 0 = fixed (20 µs), 1 = adaptive	
BiSS_CFG0.dir	0, 1	BiSS SCDS Count Direction 0 = same direction, 1 = opposite direction	
BiSS Data			
BISS_CFG0.mtlen	0	BiSS/SSI Multiturn Bits = 0 bit MT data	
	1...5	BiSS/SSI Multiturn Bits = 4, 8, 12, 16, 20 bit	
	6	BiSS/SSI Multiturn Bits = 24 bit MT data	Allowed maximum MT output resolution.
BISS_RES	4 096	Singleturn BiSS SCDS Resolution = 12 bit	Binary numbers from 4 upwards only.
	16 384	Singleturn BiSS SCDS Resolution = 14 bit	
	65 536	Singleturn BiSS SCDS Resolution = 16 bit	
	131 072	Singleturn BiSS SCDS Resolution = 17 bit	
	2 097 152	Singleturn BiSS SCDS Resolution = 21 bit	
	16 777 216	Singleturn BiSS SCDS Resolution = 24 bit	Allowed maximum ST output resolution.
BiSS_DLEN	25	BiSS SCDS Data Length (bit count = DLEN + 1)	Read only (calculated by iC-TW39).
BiSS Profile			
BISS_CFG1.bp	0	BiSS Profile BP3 (Standard Encoder Profile)	with nE, nW, 6-bit CRC (polynomial 0x43, start value 0)
	1	BiSS Profile BP3s (Safety Encoder Profile)	with nE, nW, 6-bit Sign-of-Life, 16-bit CRC (polynomial 0x190D9, start value 0).
PROFILE	0x1A62	BiSS Encoder Profile ID	As calculated by iC-TW39.
BiSS Position Preset			
BISS_NRPPH	0	BiSS Interpolated Angle Preset Phase Shift	These values will be calculated by iC-TW39 if triggered by command or input NPRE.
BISS_RCPPH	0	BiSS Revolution Count Preset Phase Shift	
CALIB_CFG.gppre	0	Position Preset Input NPRE = disabled	
	1	Position Preset Input NPRE = enabled	

Table 8: <BiSS> Parameters

BISS_CFG0 is used to configure the BiSS/SSI Interface for protocol (BiSS or SSI), direction of rotation, multiturn bit length, adaptive timeout, and startup mode.

BISS_CFG0.ssi determines the protocol used by the BiSS/SSI Interface.

BISS_CFG0.at determines whether the BiSS timeout is fixed (20 µs) or adaptive. For more information on the adaptive timeout, see BiSS AN23 at www.biss-interface.com.

BISS_CFG0.dir determines the count (rotation) direction of the BiSS/SSI position data.

BISS_CFG0.mtlen determines the number of bits of the revolution counter that are used for the BiSS/SSI multiturn count.
The number of BiSS multiturn bits must not be greater that the length of the revolution counter (GB_CFG.rclen).

BISS_RES determines the resolution of the singleturn position in the BiSS single-cycle sensor data (SCDS) in increments per revolution. Binary resolutions between 4 and 16 777 216 (2^{24}) increments per revolution may be specified. The BiSS resolution can be configured fully independently of ABZ or UVW resolution.

Note that the number of singleturn plus multiturn bits is limited to a maximum of 50 bits.

BISS_DLEN is a read-only register indicating the length (number of bits) of the BiSS single-cycle sensor data (SCDS) without CRC. This value is calculated automatically by the iC-TW39 and includes error and warning bits, as well as the optional sign-of-life counter.

BISS_CFG1.bp configures iC-TW39 according to the BiSS Encoder Profiles 3 (BP3) or 3 Safety (BP3S). See www.biss-interface.com for more information on the BiSS protocol and BiSS encoder profiles. The available frame formats are shown in Figure 17.

PROFILE contains the BiSS Encoder Profile ID that is generated automatically by iC-TW39 depending on the user's configuration. Restart the interpolator (command 0x04) after any change to ensure proper BiSS operation. See www.biss-interface.com for more information on BiSS encoder profiles.

Note: Always restart the interpolator (command 0x04) after any changes of settings to ensure proper BiSS operation.

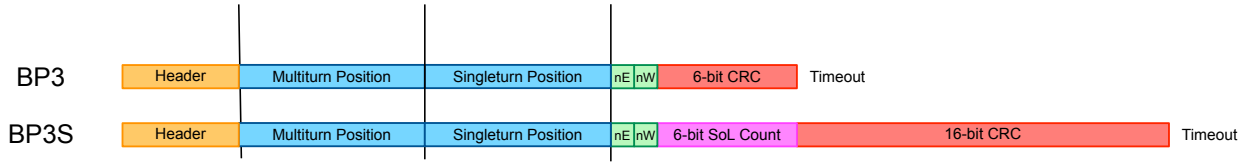


Figure 17: BiSS SCD Frame Formats

Position Preset

BISS_NRPPH is the preset phase shift which is added to the interpolated angle for read-out of ST data using the BiSS/SSI Interface.

BISS_RCPPH is the preset phase shift which is added to the revolution count for read-out of MT data using the BiSS/SSI Interface.

Both these values are set automatically by the iC-TW39 when a position preset is performed to define the zero angle. The position preset for the BiSS/SSI Interface does not change the UVW or the ABZ output phase.

The BiSS/SSI position preset function can be initiated either by writing command 0x05 to the COMMAND register at address 0x60, or using the NPRE input. If input NPRE is enabled for preset (**CALIB_CFG.gppre** = 1), the preset phase shifts are determined and stored to the EEPROM when input NPRE changes back from low to high level.

BiSS Control Data Channel

The BiSS control data communication can directly access the BiSS Direct Access registers the iC-TW39 provides at 0x40 up to 0x7F, e.g. to read the BiSS Profile ID, status, etc.

Furthermore, an indirect access to all internal iC-TW39 registers is supported by exchange registers (on 0x5C to 0x5F) as shown in Table 9.

iC-TW39 Register Address and Data
Indirect read/write access to all iC-TW39 registers is available to the BiSS Interface via slave register addresses 0x5C...0x5F when BiSS register access is allowed (BISS_KEY = 0xB4). To read an iC-TW39 register via the BiSS Interface, use the following sequence:

1. Write the LSB of the iC-TW39 register address to BiSS slave register address 0x5C.
2. Write the MSB of the iC-TW39 register address to BiSS slave register address 0x5D.
3. Read the LSB of the iC-TW39 register data from BiSS slave register address 0x5E.
4. Read the MSB of the iC-TW39 register data from BiSS slave register address 0x5F.

It is important to read the LSB register (0x5C) first to ensure that the returned 16-bit register data is consistent (both LSB and MSB sampled at the same time).

To write to an iC-TW39 register via the BiSS Interface, use the following sequence:

1. Write the LSB of the iC-TW39 register address to BiSS slave register address 0x5C.
2. Write the MSB of the iC-TW39 register address to BiSS slave register address 0x5D.
3. Write the LSB of the iC-TW39 register data to BiSS slave register address 0x5E.
4. Write the MSB of the iC-TW39 register data to BiSS slave register address 0x5F.

It is important to write the LSB register (0x5C) first to ensure that both the MSB and LSB of the 16-bit register data are written to the iC-TW39. If the MSB of the data (0x5D) is written first, the LSB (0x5C) will not be written to the iC-TW39.

Non-Implemented Registers and Features
BiSS slave register addresses 0x64...0x77 are not implemented in the iC-TW39. Accesses to these registers are rejected and the W-bit in the CDS frame is inverted. BiSS passthrough mode allows a host processor connected to the iC-TW39's SPI interface to handle these accesses if desired.

BiSS Slave Registers							
BiSS Slave Register					iC-TW39 Register		
Address	BiSS Parameter	Description	Mode	Value	Address	Bits	Name
0x00...0x3F	See Table	EDS SE [1]	–	–	–	–	–
0x40	BSEL(7:0)	Bank Select [1]	Read/Write		–	–	–
0x41	EDS_BANK(7:0)	EDS Bank Pointer [1]	Read-only	0x01	–	–	–
0x42 0x43	BiSS_BP_ID(15:8) BiSS_BP_ID(7:0)	BiSS Profile ID	Read-only		0x4094	7:0 15:8	PROFILE
0x44 0x45 0x46 0x47	BiSS_DEV_SN(31:24) BiSS_DEV_SN(23:16) BiSS_DEV_SN(15:8) BiSS_DEV_SN(7:0)	BiSS Device Serial Number	Read-only		0x4096	7:0 15:8	DEV_SN[15:0]
					0x4098	7:0 15:8	DEV_SN[31:16]
0x48 0x49		Chip ID	Read-only	0x1D 0x00	0xE000	7:0 15:8	CHIP_ID
0x4A 0x4B		Chip Revision	Read-only	0x41 0x90	0xE002	7:0 15:8	CHIP_REV
0x4C 0x4D		Status	Read-only		0x010E	7:0 15:8	STAT_VAL
0x4E 0x4F		Latched Status	Read-only		0x0110	7:0 15:8	STAT_LATCH
0x50 0x51		Fatal Faults	Read-only		0x0112	7:0 15:8	STAT_FATAL
0x52 0x53		Chip Temperature	Read-only		0x4068	7:0 15:8	T_NOW
0x54 0x55		Synchronization Offset	Read-only		0x0038	7:0 15:8	BISS_JO[15:0]
0x56 0x57					0x003A	7:0 15:8	BISS_JO[31:16]
0x58 0x59					0x003C	7:0 15:8	BISS_JO[47:32]
0x5A 0x5B					0x003E	7:0 15:8	BISS_JO[49:48]
0x5C 0x5D		iC-TW39 Register Address	Read/Write [2]			7:0 15:8	
0x5E 0x5F		iC-TW39 Register Data	Read/Write [2]			7:0 15:8	
0x60		iC-TW39 Command Register	Read/Write		0x4000	7:0	COMMAND
0x61		Register Protection Key	Read/Write		0x0042	7:0	BISS_KEY
0x62		General-Purpose Inputs	Read-only		0x005A	7:0	GPIN
0x63		General-Purpose Outputs	Read/Write [2]		0x0002	7:0	GPOUT
0x64...0x77		Not Implemented	–	–	–	–	–
0x78 0x79 0x7A 0x7B 0x7C 0x7D	BiSS_DEV_ID(47:40) BiSS_DEV_ID(39:32) BiSS_DEV_ID(31:24) BiSS_DEV_ID(23:16) BiSS_DEV_ID(15:8) BiSS_DEV_ID(7:0)	BiSS Device ID	Read-only		0x409A	7:0 15:0	DEV_ID[15:0]
					0x409C	7:0 15:0	DEV_ID[31:16]
					0x409E	7:0 15:0	DEV_ID[47:32]
0x7E 0x7F	BiSS_MFR_ID(15:8) BiSS_MFR_ID(7:0)	BiSS Manufacturer ID	Read-only		0x40A0	7:0 15:0	MFR_ID
Notes	This table is not relevant in BiSS Passthrough Mode (BISS_CFG2.passmode =2). [1] Only if BISS_CFG1.eds = 1. [2] These registers are only writeable if BISS_KEY[7:0] = 0xB4.						

Table 9: BiSS Slave Registers

iC-TW39 Status, Fault, and Command Registers
The iC-TW39's STAT_VAL, STAT_LATCH, and STAT_FATAL, registers are available to the BiSS Interface at slave register addresses 0x4C...0x51.

The iC-TW39's COMMAND register is available at slave register address 0x60. When BiSS register access is protected (BISS_KEY ≠ 0xB4), only commands 0x04...0x06 can be executed via the BiSS Interface. See COMMAND REGISTER on page 36 for more information on these commands.

User Data Registers
Six user data registers allow for storage of a user-defined product serial number (**DEV_SN** at 0x44...0x47), device ID (**DEV_ID** at 0x78...0x7D), and manufacturer ID (**MFR_ID** at 0x7E...0x7F) in the internal EEPROM.

The BiSS manufacturer ID is assigned to each BiSS licensee by iC-Haus (support@biss-interface.com). The combination of serial number, device ID and manufacturer ID must be unique to allow the BiSS master to properly assign device addresses.

Register Write Protection
The **BISS_KEY** at 0x61 is used to allow or deny BiSS write access to iC-TW39 registers and commands.

If BISS_KEY[7:0] = 0xB4, the BiSS master can write to any iC-TW39 register. If BISS_KEY[7:0] ≠ 0xB4, the BiSS master can only write to the iC-TW39 COMMAND register, and only certain commands can be executed. See THE COMMAND REGISTER on page 36 for more information. The BiSS master can read any iC-TW39 register regardless of the BISS_KEY value.

SSI Mode
The SSI protocol is selected when BISS_CFG0.ssi = 1. As for BiSS, SSI communication also requires an external RS422-compatible line driver/receiver to provide differential signals as shown in Figure 9.

SSI configuration is the same as BiSS configuration, except that only the configured singleturn and (counted) multiturn position are returned in the serial data stream. BiSS-specific features such as feedback bits, CRC, control data, etc. are not available in SSI mode and do not need to be configured. The SSI data frame format is shown in Figure 18.

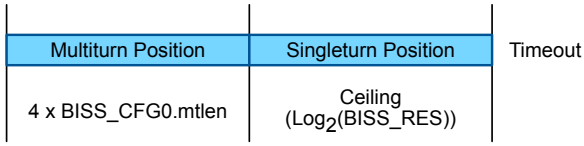


Figure 18: SSI Frame Format

It is possible to write to the iC-TW39 registers in SSI mode using the same procedure as BiSS. However, it is not possible to read any iC-TW39 registers in SSI mode. It should only be necessary to write to the iC-TW39 in SSI mode to enable BiSS mode when SPI communication is not available.

To switch the iC-TW39 from SSI mode to BiSS mode using the SSI interface, use the following sequence:

1. Write 0xB4 to slave register address 0x61.
2. Write 0x18 to slave register address 0x5C.
3. Write 0x00 to slave register address 0x5D.
4. Write 0x00 to slave register address 0x5E.
5. Write 0x00 to slave register address 0x5F.

This writes 0xB4 to BISS_KEY to allow register access, and 0x0000 to BISS_CFG0, which disables SSI mode and enables BiSS mode. It also resets all other BISS_CFG bits which must then be restored to the desired configuration via the BiSS Interface.

BiSS ELECTRONIC DATA SHEET

The BiSS interface can be configured to implement BiSS Standard Encoder Electronic Data Sheet EDS SE. This allows the BiSS master to read the device configuration over the BiSS interface at startup. (In hosted applications, the host processor can implement any BiSS EDS.)

If BISS_CFG1.eds = 1 enables the EDS registers, the BiSS bank selection register 0x40 is set to 0x01 and registers 0x00 – 0x3F provide the EDS data according to Table 10. This EDS data is always available regardless of the bank selection value. Refer to the EDS SE data sheet for more information on EDS register entries.

If BISS_CFG1.eds = 0 disables the EDS, the BiSS slave registers 0x00...0x40 are undefined.

EDS Register Entries

EDS_VER_LEN[15:0] contains the version and length of the EDS SE, where iC-TW39 sets EDS_VER_LEN[15:8] to 0x01 after startup because the EDS SE occupies only a single bank. The EDS version on EDS_VER_LEN[7:0] can be configured as required (to 0x10 for EDS SE revision A1).

EDS_MAX_BUSY[7:0] (Maximum BiSS Timeout) is set by the iC-TW39 to 0xAA if BISS_CFG0.at = 0 (fixed timeout) and 1 if BISS_CFG0.at = 1 (adaptive timeout) and should not be changed.

EDS_MAX_BUSY[15:8] (Maximum SCD Processing Time) is set by the iC-TW39 to 0x0004 and should not be changed.

EDS_TC_MTLEN[7:0] (Maximum BiSS Timeout) is set by the iC-TW39 to 0x0000 and should not be changed.

EDS_TC_MTLEN[15:8] (Multiturn Data Length) is calculated by the iC-TW39 based on BISS_CFG0.mtlen and should not be changed.

EDS_STLEN_DIAG[7:0] (Singleturn Data Length) is calculated by the iC-TW39 based on BISS_RES and should not be changed.

EDS_STLEN_DIAG[15:8] (SCD Feedback Length) is calculated by the iC-TW39 based on BISS_CFG1.fb and should not be changed.

EDS_INCOFF (Incremental Offset Address LSB) must be set to 0x0054 for proper operation of EDS SE in the iC-TW39.

EDS_TINTEXT[7:0] must be set to 0xD2 for proper operation of the internal temperature sensor in the iC-TW39. It is recommended to set EDS_TINTEXT[15:8] = 0x00 since the iC-TW39 does not support an external temperature sensor.

Electronic Data Sheet EDS SE						
BiSS Slave Register				iC-TW39 Register		
Address [1]	EDS SE Parameter	Description	Value	Address	Bits	Name
0x00	EDS_VER	EDS Version		0x406A	7:0	EDS_VER_LEN
0x01	EDS_LEN	EDS Length (Banks)	0x01		15:8	
0x02	USR_STA	User Data Start Address	0xFF	0x406C	7:0	EDS_STA_END
0x03	USR_END	User Data End Address	0xFF		15:8	
0x04	TO_MAX	Maximum BiSS Timeout	Calculated	0x406E	7:0	EDS_MAX_BUSY
0x05	TBUSY_S	Maximum SCD Processing Time	4		15:8	
0x06	TCYC	Minimum Cycle Time	0	0x4070	7:0	EDS_TC_MTLEN
0x07	MT_LEN	Multiturn Data Length (Bits)	Calculated		15:8	
0x08	ST_LEN	Singleturn Data Length (Bits)	Calculated	0x4072	7:0	EDS_STLEN_DIAG
0x09	DIAG_LEN	SCD Feedback (Diagnosis) Length	Calculated		15:8	
0x0A	EN_TYP	Encoder Type		0x4074	7:0	EDS_ENTYP_SIP
0x0B	SIP_CNT[23:16]	Signal Periods per Revolution			15:8	
0x0C	SIP_CNT[15:8]			0x4076	7:0	EDS_SIP
0x0D	SIP_CNT[7:0]				15:8	
0x0E	SPD_MAX[15:8]	Maximum Speed		0x4078	7:0	EDS_SPDMAX
0x0F	SPD_MAX[7:0]				15:8	
0x10	INC_OFF	Position Offset Address LSB	Must be 0x54	0x407A	7:0	EDS_INCOFF
0x11	Reserved		0		15:8	
0x12	Reserved		0	0x407C	7:0	EDS_RES0_RES1
0x13	Reserved		0		15:8	
0x14	TLATEN	Typical Position Latency		0x407E	7:0	EDS_TLATEN
0x15	Reserved		0		15:8	
0x16	Reserved		0	0x4080	7:0	EDS_RES2_RES3
0x17	Reserved		0		15:8	
0x18	T_INT	Internal Temperature Start Address	Must be 0xD2	0x4082	7:0	EDS_TINTEXT
0x19	T_EXT	External Temperature Start Address	(0x00)		15:8	
0x1A	Reserved		0	0x4084	7:0	EDS_RES4_RES5
0x1B	Reserved		0		15:8	
0x1C	Reserved		0	0x4086	7:0	EDS_RES6_RES7
0x1D	Reserved		0		15:8	
0x1E	Reserved		0	0x4088	7:0	EDS_RES8_RES9
0x1F	Reserved		0		15:8	
0x20	PDATE[31:24]	Production Date		0x408A	7:0	EDS_PDATE[15:0]
0x21	PDATE[23:16]				15:8	
0x22	PDATE[15:8]			0x408C	7:0	EDS_PDATE[31:16]
0x23	PDATE[7:0]				15:8	
0x24	PID[31:24]	Product ID		0x408E	7:0	EDS_PID[15:0]
0x25	PID[23:16]				15:8	
0x26	PID[15:8]			0x4090	7:0	EDS_PID[31:16]
0x27	PID[7:0]				15:8	
0x28	STATUS_E1	Address of Error Byte 1	0x4C			
0x29	STATUS_E2	Address of Error Byte 2	0x4D			
0x2A	STATUS_E3	Address of Error Byte 3	0x4E			
0x2B	STATUS_E4	Address of Error Byte 4	0x4F			
0x2C	STATUS_W1	Address of Warning Byte 1	0x50			
0x2D	STATUS_W2	Address of Warning Byte 2	0x48			
0x2E	STATUS_W3	Address of Warning Byte 3	0x4A			
0x2F	STATUS_W4	Address of Warning Byte 4	0x4B			
0x30...0x33	CMD0...CMD3		0			
0x34	CMD_ADDR	Address of Command Register	0x60			
0x35	REBOOT	Reconfigure from EEPROM	0xFF			
0x36	RESET	Initialize	0x04			
0x37	PRESET	Execute Preset	0x05			
0x38	SCLEAR	Clear Status	0x06			
0x39...0x3D	Reserved		0			
0x3E	Reserved		0	0x4092	7:0	EDS_CHKSUM
0x3F	CHKSUM	EDS Checksum			15:8	
Notes	[1] Contents available only if BISS_CFG1.eds = 1.					

Table 10: BiSS Slave Registers for EDS SE

BiSS PASSTHROUGH MODE

If a full multi-bank BiSS slave with programmable EDS, extended OEM memory, and additional functionality is required, BiSS register communication can be serviced by a host processor connected to the iC-TW39's SPI port.

Following power up, the host processor can initiate BiSS passthrough mode by setting BISS_CFG2.passmode. The configured passmode selects whether only non-implemented registers or *all* BiSS slave registers are queried from the host processor.

BISS_CFG2.passmode (0x002A Bits 1:0)	
Value	Description
3	Reserved (do not use)
2 1 0	Passthrough for all BiSS registers Passthrough for non-implemented BiSS registers Passthrough disabled (default)
Note	The setting is not stored in the EEPROM. The interpolator must be restarted (command 0x04) after changes.

Table 11: BiSS Passthrough Mode

If BISS_CFG2.passmode = 2, the iC-TW39 passes *all* BiSS slave register accesses to the host processor via the iC-TW39's SPI interface. In this case, the host processor must implement the complete BiSS slave register (addresses 0x00...0x7F) as the iC-TW39 will *not* respond to any BiSS slave register accesses.

In BiSS passthrough mode, when the BiSS master reads or writes a BiSS slave register in the iC-TW39, the request is passed to the host processor via the BISS_PASS register for action. BISS_PASS contains the register address and data of the BiSS slave register access passed through to the SPI interface. The host must respond appropriately to these requests, which are then passed back to the BiSS master via the BISS_PASS register.

BISS_PASS Register (0x002E)		
Bits	Name	Description
15	rd	BiSS read (not write)
14:8	BISS_PASS.addr	BiSS address to read or write
7:0	BISS_PASS.data	BiSS data to read or write
Note	Contents are not defined if passthrough mode is disabled.	

Table 12: BiSS Passthrough Register

BiSS passthrough communication is controlled by the BiSS read/write request (brw) bit in the SPI status byte. The brw bit can also be configured to activate xIRQ to interrupt the host processor. See STATUS/FAULT MONITOR on page 42 for more information.

Figure 19 shows the recommended implementation of a BiSS write to a host processor via the SPI interface in BiSS passthrough mode.

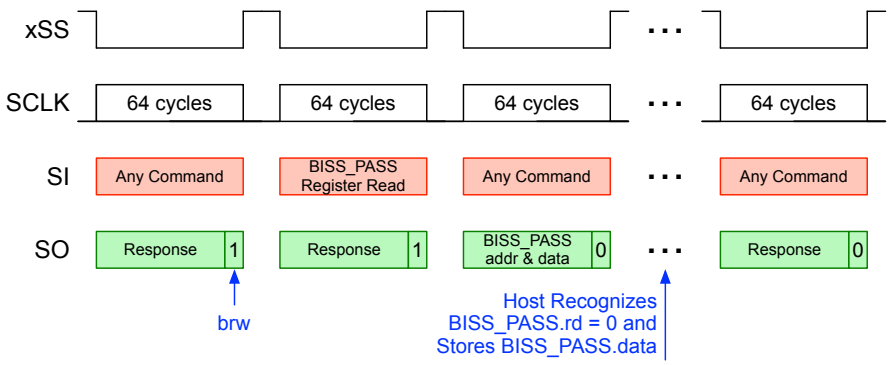


Figure 19: BiSS Passthrough Write

When the host receives a response with brw = 1, it must read the BISS_PASS register. If BISS_PASS.rd = 0, the request is a BiSS passthrough write and BISS_PASS.data contains the data to be written to the BiSS slave register at BISS_ADDR. In this case, reading BISS_PASS resets the brw bit. The host processor must then store BISS_PASS.data for future recall by the BiSS master. For example, if the BiSS master selects bank 7 by writing 0x07 to BiSS slave register 0x40, the host processor must remember this and return bank 7 data when the BiSS master subsequently reads register bank data (BiSS slave register addresses 0x00...0x3F).

Figure 20 shows the recommended implementation of a BiSS read from a host processor via the SPI interface in BiSS passthrough mode.

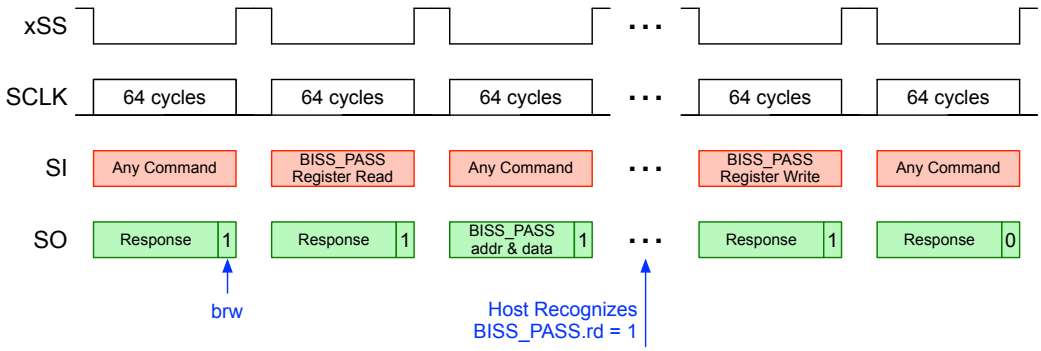


Figure 20: BiSS Passthrough Read

When the host receives a response with brw = 1, it must read the BISS_PASS register. If BISS_PASS.rd = 1, the request is a BiSS passthrough read and the host processor must then write the requested data to BISS_PASS.data. This passes the requested data to the BiSS interface and resets the brw bit. For example, if the BiSS interface requests the EDS bank by reading BiSS slave register 0x41, the host processor reads BISS_PASS = 0xC100 and then must write the bank number of the bank where the EDS starts to BISS_PASS.data.

ABSOLUTE DATA INTERFACE (ADI)

The **ADI** uses the A/U and B/V pins for the ADI Clock Output and Data Input respectively. These signals may need to be connected to a suitable driver/receiver depending on the connected absolute data device.

Using the ADI requires additional configuration as explained in the following.

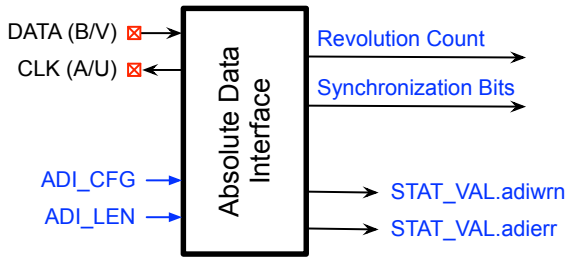


Figure 21: Absolute Data Interface (ADI)

The ADI uses a BiSS/SSI master to read the revolution count from an external multiturn device such as the iC-PVL. The revolution count is used to initialize the absolute position at startup and for verification of proper counting of the iC-TW39 during operation. Synchronization bits ensure that the absolute position synchronization is correct even when the system is moving during synchronization or if there is misalignment of the external revolution counting device.

ADI operation is enabled if **MAIN_CFG.nio = 3**, also changing the functionality of the A/U and B/V outputs (see Figure 21). The ADI must be configured for protocol (BiSS or SSI), clock frequency, number of revolution count bits, number of synchronization bits, etc. The configuration must always be compatible with the external multiturn device (→ MT sensor) for proper operation.

The registers used by the ADI are shown in Table 13.

Parameter	Value	Description	Comments
MAIN_CFG.nio		Function of Outputs	
	3	3 = ADI Interface Mode	Enables the ADI operation.
	0, 1, 2	0 = disabled, 1 = A+, B+, Z+, 2 = U+, V+, W+	
< ADI Setup >			
ADI_CFG.biss	0, 1	ADI Master Protocol: 0 = SSI, 1 = BiSS C	
ADI_CFG.freq	0, 1	ADI Clock Frequency: 0 ≈ 150 kHz, 1 ≈ 1.5 MHz	
ADI_CFG.mode	0	ADI Update Mode = Only after 1st ADI position read	
	(1)	(1 = All ADI reads update the counter)	
ADI_LEN.rc		ADI Revolution Count Bits	The revolution counter length must be configured equally or smaller (→ GB_CFG.rclen)
range	0...6	0 bits, 4 bits, 8 bits, 12 bits, 16 bits, 20 bits, 24 bits	
GB_CFG.syncbits		Revolution Counter Synchronization Bits	Misalignment tolerance of MT vs. ST angle:
range	0...3	0 = 4 bits, 1...3 = 1...3 bits	±168.75°, ±90°, ±135°, ±157.5°
ADI_LEN.sgap		ADI Synchronization Gap Bits	Bits to be ignored if the MT sensor
range	0...15	none ... 15 bits maximum	provides more than 4 syncbits.
ADI_LEN.fbk		ADI Error And Warning Bits	
range	0...2	0 = none, 1 = 1 bit (error), 2 = 2 bits (error + warning)	
< ADI Data Processing >			
IPO_CFG.dir		Interpolated Angle Counting Direction	
	0, 1	0 = normal, 1 = inverted	
GB_CFG.clear	0	Revolution Counter Clear Mode = never	Setting required for ADI.
	3	3 = always (abs = rel)	Default for BiSS and ABZ/UVW output.
ADAPT_CFG.iacal	1	Use ADI or SPI gearbox write to calibrate IA_PHASE	Setting required for ADI.
IA_PHASE	0	Interpolated Angle Phase Shift	Alignment of zero angle (ST) to ADI data (MT).
range	0...16383	(positive integers)	Can be auto calibrated.
CALIB_CFG		Auto Calibration Mode	
	0xE5	IA Phase Calibration Mode	Other calibration functions disabled.
	0xE1	Regular Calibration Mode	

Table 13: <ADI> Parameters

ADI Setup

ADI_CFG.biss determines whether the ADI is a BiSS or SSI master. Choose the protocol used by the external MT sensor.

The BiSS protocol implemented by the ADI ignores the CDS bit and does not send a CDM bit (no control data communication). A 6-bit CRC must be provided by the external MT sensor but is ignored. As shown in Figures 22 and 23, the ADI CLK output remains high after the last configured data bit is received, forcing the external MT sensor into timeout.

ADI_CFG.freq determines the BiSS/SSI clock frequency of the ADI. Choose a clock frequency that is compatible with the external MT sensor.

ADI_CFG.mode determines whether just the first or all valid ADI position reads update the revolution counter.

If ADI_CFG.mode = 0, *all* valid ADI position reads (STAT_VAL.adi = 0) update the counter and the MT position jumps immediately to the new ADI position. If ADI_CFG.mode = 1, only the *first* valid ADI position read (STAT_VAL.adi = 0) after startup updates the counter and the MT position jumps immediately to the new ADI position. Subsequent valid ADI position reads are only compared to the revolution counter value and do not update the MT position.

Following all counter writes, the new position written (npw) bit in the SPI status byte is set to confirm the counter update. npw remains set until explicitly cleared by setting the clear bit (clr) in the SPI control word. npw is not set for counter compares.

Regardless of ADI_CFG.mode, after the first valid write to the revolution counter (npw = 1 in the SPI status byte), STAT_VAL.match is activated if a subsequent valid ADI position does not match the current position.

ADI_LEN is used to configure the length (number of bits) expected in the different fields in the ADI data frame. Set the ADI_LEN field lengths to match the external MT sensor.

Note: The MSBs of the ADI revolution counter bits are ignored if the revolution counter length is configured smaller.

GB_CFG.syncbits determines the number of synchronization bits used when initializing or updating the revolution counter from the ADI (or SPI). The configuration should match the number of synchronization bits supplied by the external MT sensor.

The synchronization bits ensure a proper counter updating even when the drive is running, and when the external MT sensor is misaligned. Whenever available, using more synchronization bits is recommended to increase the misalignment tolerance (see comment in Table 13).

A maximum of four synchronization bits can be processed by iC-TW39. If the external MT sensor provides more bits to be clocked out, **ADI_LEN.sgap** must be configured to ignore the number of unused least significant bits (see gap bits in Figure 22, and 23).

ADI_LEN.fbk configures for optional status feedback bits, usually a low-active error (nE) and a low-active warning (nW) bit, when output from the external MT sensor.

If ADI_LEN.fbk = 1, STAT_VAL.adierr = 1 when the nE bit in the ADI data frame is active (0) or if the external MT sensor is not ready (refer to next section).
If ADI_LEN.fbk = 2, the nE bit is evaluated as described, and the additional nW bit sets STAT_VAL.adiwrn = 1 when active (0).

ADI Data Processing

IPO_CFG.dir determines the counting (rotation) direction of the interpolated angle. It must be set to match the counting direction of the connected MT sensor. Reversing the code direction of the BiSS/SSI data output is possible independently (refer to section BiSS/SSI Interface).

Note: Always restart the interpolator (command 0x04) after changing the interpolator counting direction.

GB_CFG.clear determines how and when (if ever) crossing the zero angle resets the revolution counter. GB_CFG.clear = 0 (never) must be used when the absolute position is supplied to the iC-TW39 via the ADI (or SPI).

ADAPT_CFG.iacal = 1 setting required for ADI. Phase auto calibration aligns the 0° angle of the interpolator with the rollover point of the cycle counter of the external absolute position device or the most recent SPI gearbox write.

IA_PHASE contains the interpolated angle phase shift. This phase shift moves the 0° angle of the interpolator versus the magnet's field angle. That way the axis angle and the revolution counting rollover can be aligned to the external rollover point of the MT sensor.

The actual phase shift, *iaphase*, is calculated as

$$iaphase[^\circ] = \text{IA\_PHASE} \cdot \frac{360^\circ}{16,384}$$

Aligning the 0° angle of the interpolator to the external MT sensor is possible using IA Phase Calibration Mode (see Table 13). When enabled and started (by pin NCLB or command), the motor axis needs to spin the magnet and the MT sensor for a few revolutions for settling IA_PHASE. However, programming a fixed, system-specific phase shift may work too (e.g. when using iC-PVL scanning the same magnet).

Application Examples

The external MT sensor is ready if the ADI DATA pin (B/V) is high at the first falling edge of the ADI CLK output pin (A/U) and low after the last rising CLK edge (timeout). If either of these conditions is not true, the external MT sensor is assumed to be not ready and STAT_VAL.adierr = 1.
To avoid a permanent latched ADI error on startup, STAT_LATCH.adierr = 0 until the first valid data frame is received from the external MT sensor.

As an example for **SSI mode**, if

ADI_LEN.rc = 3 → *adircbits* = 12
GB_CFG.syncbits = 0 → 4 syncbits
ADI_LEN.sgap = 4 → 4 bits → *adisyncbits* = 8
ADI_LEN.fbk = 2

the ADI expects 12 + 4 + 4 + 2 = 22 bits in the data frame as shown in Figure 22. All data fields are expected MSB first in the data frame. The external MT sensor must provide eight sync bits, but only four are used by the iC-TW39.

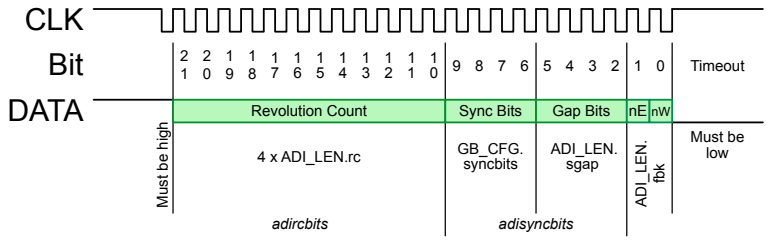


Figure 22: Expected SSI Data Frame

The ADI DATA input must be **high** at the first falling ADI CLK edge, otherwise the external MT sensor is assumed to be not ready (STAT_VAL.adierr = 1). After reading the expected number of bits, the ADI CLK output remains high, forcing a timeout. During timeout, the ADI DATA input must remain **low**, otherwise a fault in the external MT sensor is assumed (STAT_VAL.adierr = 1) and the ADI data is considered invalid.

The expected ADI data frame in BiSS mode is shown in Figure 23.

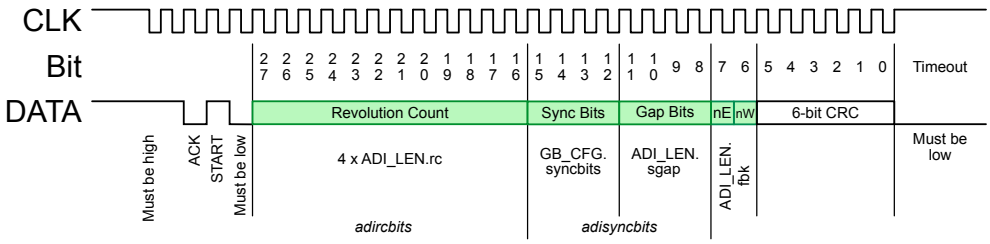


Figure 23: Expected BiSS Data Frame

Using the same example as for SSI mode, in **BiSS mode** the ADI expects 12 + 4 + 4 + 2 + 6 = 28 bits in the data frame as shown in Figure 23. All data fields are expected MSB first in the data frame. Six CRC bits must follow the last configured bit in the data frame, but are ignored by the iC-TW39.

The ADI DATA input must be **high** for the first two falling ADI CLK edges, otherwise the external MT sensor is assumed to be not ready (STAT_VAL.adierr = 1). After reading the expected number of bits, the ADI CLK output remains high, forcing a timeout. During timeout, the ADI DATA input must remain **low**, otherwise a fault in the external MT sensor is assumed (STAT_VAL.adierr = 1) and the ADI data is considered invalid.

THE COMMAND REGISTER

The command register is used to start or stop the iC-TW39 interpolator, save the configuration parameters to EEPROM, perform auto calibration, etc. To execute a command, write the appropriate value to COMMAND[7:0]. When the command has been executed, COMMAND[7:0] is reset to 0x00 by the iC-TW39 and a new command may be sent.

COMMAND (0x4000 Bits 7:0)	
Value	Description
Unprotected Commands	
0x00	Read: Command register ready/idle Write: Command termination
0x04	Start/restart interpolator
0x05	BiSS position preset
0x06	Clear latched status and faults
Protected Commands [1]	
0x02	Stop interpolator
0x0A	Copy COR values to BASE registers
0x0B	Read configuration and COR registers from EEPROM
0x0C [2]	Write configuration and COR register values to EEPROM
0x0D [2]	Write all COR register values to EEPROM
0x0E [2]	Write selected COR register values to EEPROM
0x10	Auto calibrate selected parameters
[1] Command does nothing unless unlocked by BISS_KEY = 0xB4.	
[2] Command does nothing unless the EEPROM is unlocked by TEST.we = 1.	
Do not issue any undescribed command value.	
Do not issue follow-up commands unless 0x00 reads zero.	

Table 14: Command Register

Command 0x00 aborts a command execution in progress (e.g. 0x10 for auto calibration). Reading the COMMAND register returns the command value in execution or 0x00 for the idle state.

Command 0x02 stops the interpolator. When the interpolator is stopped, the ABZ/UVW outputs are in a high impedance state. The NERR output remains operational.

Command 0x04 re-calculates all derived parameter values and then starts or restarts the interpolator using the current configuration values.

Command 0x05 executes a position preset by loading the BiSS preset phase shift registers (BISS_NRPPH and BISS_RCPPH) with the negative of the current absolute position. After this command is executed, the BiSS Interface outputs a zeroed MT and ST position. The new preset register values are written to the EEPROM and are available at power-up.

Command 0x06 clears all the latched status bits in the STAT_LATCH register. After executing this command, STAT_LATCH = 0 if no status conditions are active.

Command 0x0A copies the values in the correction parameter registers to the corresponding base registers as shown below.

Command 0x0A	
Correction Register	Base Register
S_OFS_COR	→ S_OFS_BASE
C_OFS_COR	→ C_OFS_BASE
SC_BAL_COR	→ SC_BAL_BASE
SC_PH_COR	→ SC_PH_BASE

Table 15: Command 0x0A

Note that command 0x0A does *not* store the new base register values to EEPROM; this must be done using command 0x0C.

Command 0x0B reads the configuration and COR registers from the internal EEPROM and starts the interpolator.

Command 0x0C writes the values of the configuration and COR registers to the internal EEPROM and may take up to 1 second to complete.

Command 0x0D writes all the COR register values to the internal EEPROM, and may take up to 1 second to complete.

Command 0x0E writes the values of the COR registers to the internal EEPROM, and may take up to 1 second to complete.

Command 0x10 initiates auto calibration of the correction parameters. This command must be manually terminated after calibration is complete by writing 0x00 to COMMAND[7:0]. When this command is terminated, the COR register values are copied to the corresponding BASE registers, and both register values are transferred to the EEPROM. Allow 1 second to complete.

AUTO CALIBRATION AND ANGLE ERROR CORRECTION

Parameter	Default	Description	Comments
SC_GNA_COR	5	Analog Correction: S/C Gain	These parameters will be auto calibrated by iC-TW39 on command (or NCLB button).
range	0...23		
S_OFSA_COR	0	Analog Correction: Sine Offset	
C_OFSA_COR	0	Analog Correction: Cosine Offset	
range	±31	6-bit 2's complement value sign-extended to 16 bits	
SC_GN_COR	100	Digital Correction: S/C Gain	
range	0...4095		
SC_BAL_COR	0	Digital Correction: S/C Balance	These parameters will be auto calibrated and dynamically auto adapted.
S_OFS_COR	0	Digital Correction: Sine Offset	
C_OFS_COR	0	Digital Correction: Cosine Offset	
SC_PH_COR	0	Digital Correction: S/C Phase	
range	±2 047	12-bit 2's complement value sign-extended to 16 bits.	
CALIB_CFG.inl	0	Advanced INL Calibration	Constant speed required for calibration.
range	0, 1	0 = disabled, 1 = enabled	

Note: All COR parameters of this table will be auto calibrated by iC-TW39. Default means factory default configuration if provided.

Table 16: <Auto Calibration and Angle Error Correction> Parameters

Once the iC-TW39 has been configured and installed to the magnet, the TMR sensor signals must be calibrated to determine proper values for gain, offset correction, channel balance, and phase correction. This is most easily done using the auto calibration feature of the iC-TW39 to automatically determine optimum values for these parameters.

The registers used by auto calibration are shown in Table 16.

The COR registers contain the angle error correction parameters. The correction values are determined when auto calibration is performed and are updated during operation by auto adaption.

Calibration Procedure

Auto calibration can be initiated in hardware using the NCLB input or via a software command using the BiSS Interface.

With auto calibration initiated, provide ten or more magnet revolutions and the iC-TW39 tunes the correction parameters to provide lowest angular error and jitter in the interpolated AB and/or UVW outputs.

The magnet rotation applied for auto calibration does not need to be at a constant speed nor must it be unidirectional. However, a minimum of 1.5 revolutions without direction reversal is required for auto calibration to make any changes in the correction parameter values.

After providing sufficient magnet revolutions, auto calibration is terminated by releasing the NCLB input or a software command and the tuned correction values will be automatically stored to the internal EEPROM for use on subsequent startups.

Advanced INL Calibration

When enabling INL calibration in addition, the magnet must be rotated at constant speed. The drive's speed ripple may not exceed 0.5 %, and so running higher speeds is usually helpful to benefit from any inertia of rotating masses. Note that several revolutions without direction reversal are required for settling. It is recommended to validate the INL calibration procedure by measurements, e.g. using a reference encoder.

After providing sufficient magnet revolutions, auto calibration and INL calibration is terminated by releasing the NCLB input or a software command and the tuned correction values will be automatically stored to the internal EEPROM for use on subsequent startups.

Note: The INL calibration can be reset by writing 0x00 to address 0x070C (INL_AMP) and 0x070E (INL_PH).

Pin-Triggered Auto Calibration (NCLB pin)

Auto calibration is initiated by pulling the NCLB input low. A push-button switch and pull-up resistor connected between NCLB (as shown in Figure 9 on page 14) is an easy way to achieve this in series production.

The recommended sequence for pin-triggered auto calibration is:

1. Ensure all configuration registers have valid values for the desired application (e.g. download the default configuration provided by the GUI).
2. Pull NCLB input low.
3. Rotate the magnet as explained under Calibration Procedure.
4. Release the NCLB input (it is pulled high by the external pull-up resistor). The COR register values are copied to the corresponding BASE registers, and the COR and BASE register values are stored to the EEPROM. Do not interrupt the power supply, wait for at least 1 second.

Command-Triggered Auto Calibration
Auto calibration is accomplished using the BiSS Interface to send the auto calibration command (0x10) to the command register. After sending the command, rotate the magnet as for pin-triggered auto calibration.

When calibration is complete, stop auto calibration by writing 0x00 to the command register.

Finally, the EEPROM needs to be updated for use on subsequent startups. The recommended sequence for command-triggered auto calibration is:

1. Ensure all configuration registers have valid values for the desired application (e.g. download the default configuration provided by the GUI).
2. Initiate auto calibration by writing 0x10 to the command register (0x4000).
3. Rotate the magnet as explained under Calibration Procedure.
4. Terminate auto calibration by writing 0x00 to the command register.
5. Copy the calibrated COR register values to the BASE registers by writing 0x0A to the command register.
6. Store the chip configuration and the calibrated COR and BASE register values to the internal EEPROM by writing 0x0C to the command register.

Note: After calibration, all the residue registers of the Error Monitoring (see RESI registers in Table 20) will be near zero. If this is not the case, auto calibration should be repeated.

BASE Registers
The newly calibrated values are also copied to the corresponding BASE registers when auto calibration is terminated as shown below.

Correction Register	Base Register
S_OFS_COR	→ S_OFS_BASE
C_OFS_COR	→ C_OFS_BASE
SC_BAL_COR	→ SC_BAL_BASE
SC_PH_COR	→ SC_PH_BASE

Table 17: Auto Load BASE Registers

For automatic angle error correction in operation, values for the **BASE and LIM** registers must be available from the EEPROM. Initially, it is recommended to set the BASE registers to 0 and the LIM registers to 2 047 to avoid unintentional excess adaption faults. Once auto adaption is working properly, the LIM values can be reduced as required to enable the excess adaption monitor. Refer to the following section for further information on error and adaption monitoring.

EXCESSIVE ERROR AND ADAPTION MONITOR

Parameter	Default	Description	Comments
Sensor Amplitude Monitor			
SC_AMP_LOW	1200	Weak Signal Threshold	1200 = 50 % of nominal signal.
range	0...2880	(positive integer)	
Excessive Error Monitor			
SC_OFS_TH	200	Sin/Cos Offset Residue Threshold	Alarm thresholds of uncompensated signal errors (RESI registers).
SC_BAL_TH	200	Sin/Cos Balance Residue Threshold	
SC_PH_TH	200	Sin/Cos Phase Residue Threshold	
IA_PH_TH	100	Interpolated Angle Phase Residue Threshold	
range	0...2047	(positive integers)	
Excessive Adaption Monitor			
S_OFS_BASE	0	Sine Offset Base Value	These values will be configured by iC-TW39 upon releasing pin NCLB.
C_OFS_BASE	0	Cosine Offset Base Value	
SC_BAL_BASE	0	Sin/Cos Balance Base Value	
SC_PH_BASE	0	Sin/Cos Phase Base Value	
range	±2 047	12-bit 2's complement value sign-extended to 16 bits.	
SC_OFS_LIM	2047	Sin/Cos Offset Limit	Stop limits for auto adaption.
SC_BAL_LIM	2047	Sin/Cos Balance Limit	
SC_PH_LIM	2047	Sin/Cos Phase Limit	
range	0...2047	(positive integers)	
Temperature Monitor			
T_ALARM	1200	Alarm Temperature = approx. 120 °C	Adjustable between –50 °C to 150 °C.
range	-500...1500	2's complement value	

Table 18: <Monitor> Configuration Parameters

Parameter	Default	Description	Comments
Sensor Amplitude Monitor			
SC_AMP *	...	Sin/Cos Vector Amplitude	Calculated by iC-TW39.
range	0...4095		
Excessive Error Monitor			
S_OFS_RESI *	0	Sine Offset Residue	These values will be determined by iC-TW39 in application.
C_OFS_RESI *	0	Cosine Offset Residue	
SC_BAL_RESI *	0	Sin/Cos Balance Residue	
SC_PH_RESI *	0	Sin/Cos Phase Residue	
(IA_PH_RESI *)	0	(If using ADI: Interpolated Angle Phase Residue)	
range	±2 047	12-bit 2's complement value sign-extended to 16 bits.	
S_OFS_MAX *	0	Max. Sine Offset Residue	These values will be determined by iC-TW39 in application.
C_OFS_MAX *	0	Max. Cosine Offset Residue	
SC_BAL_MAX *	0	Max. Sin/Cos Balance Residue	
SC_PH_MAX *	0	Max. Sin/Cos Phase Residue	
(IA_PH_MAX *)	0	(If using ADI: Max. IA Phase Residue	
range	±2 047	12-bit 2's complement value sign-extended to 16 bits.	
Temperature Monitor			
T_NOW *	274	Current Temperature = approx. 27.4 °C	Temperature measurement data.

*) Read only register. Values are not stored on the chip's EEPROM.

Table 19: <Monitor> Operation Parameters

Sensor Amplitude Monitor

The iC-TW39 continuously monitors its sensor signals by calculating **SC_AMP**, the Lissajous vector amplitude of the TMR sensor's sin/cos signals according to $\sqrt{Sin^2 + Cos^2}$. The calculation is continuously updated every 500 µs even when the magnet is not moving. Following auto calibration, the target amplitude of 2400 should have been reached due to gain adaption.

During operation, iC-TW39 evaluates the vector amplitude for signal loss and sensor failure detection.

The corresponding status bit STAT_VAL.scamp is activated if the vector amplitude increases to 120 % (value 2880), or decreases to the weak signal threshold **SC_AMP_LOW** (value to be configured). Setting

SC_AMP_LOW to 1200 configures a reasonable alarm threshold of 50 % the nominal vector amplitude.

Excessive Error Monitor

iC-TW39 continuously calculates the residual offset, balance, and phase error of the corrected sensor signals. These residues represent the **uncorrected sine and cosine signal errors**.

There are five read-only **RESI registers** representing the residual signal errors. All of these residues are near zero after auto calibration and are kept near zero during operation by permanent auto adaption. The residue registers are only updated after full revolutions of the magnet.
The residual interpolated angle phase error is also calculated and reflects the phase drift between the ST angle and, if there is any, an external MT sensor connected to the ADI.

The four **TH registers** configure the alarm thresholds for activation of the status bit STATUS_VAL.resi and the latching on STATUS_LATCH.resi. That way the NERR output can be enabled, should any of the residue values become excessive, i.e. exceeds the maximum error residue that should be allowed during operation.

In operation, the **.resi** status bit is set whenever the absolute value of one of the residues (RESI registers) exceeds its corresponding threshold (TH registers). See STATUS/FAULT MONITOR on page 42 for more information.

Residue and Residue Threshold Registers	
Residue Register	Residue Threshold Register
S_OFS_RESI C_OFS_RESI	SC_OFS_TH
SC_BAL_RESI	SC_BAL_TH
SC_PH_RESI	SC_PH_TH
(IA_PH_RESI)	(IA_PH_TH)

Table 20: Residue and Residue Threshold Registers

Additionally, five **MAX registers** capture the maximum error residue values encountered since startup. These registers are useful for diagnosing transient issues or evaluating worst-case application performance.

Maximum residue registers contains signed values, but the determination of the maximum residue is based on the absolute value of the residue:
If |*_RESI| > |*_MAX| then *_MAX = *_RESI.

MAX registers can be cleared by a restart command or when cycling power.

Excessive Adaption Monitor

The excessive adaption monitor detects when one or more of the error correction parameters has changed too much due to auto adaption during operation. Such excessive adaption is often the sign of a failing sensor or system. Excessive adaption is indicated by the status bit STAT_VAL.adapt and latched on STAT_LATCH.adapt.

The four **BASE registers** are used to store the initial sin/cos error correction parameters after the sensor has been installed and calibrated.

The three **LIM registers** configure the maximum allowed deviation of the sin/cos error correction parameters versus their base values. If a limit is reached in operation, the **.adapt** status bit for excessive adaption is set and the auto adaption of the corresponding error correction parameter stopped.

Note: The excessive adaption monitor is disabled when all BASE register values are set to 0 and all LIM register values to 2 047.

Configuration of Excessive Adaption Monitor
To configure this monitoring, the values for the base and limit registers must be entered and stored in the EEPROM.

Correction, Base, and Limit Registers		
Correction Register	Base Register	Limit Register
S_OFS_COR C_OFS_COR	S_OFS_BASE C_OFS_BASE	SC_OFS_LIM
SC_BAL_COR	SC_BAL_BASE	SC_BAL_LIM
SC_PH_COR	SC_PH_BASE	SC_PH_LIM

Table 21: Correction, Base, and Limit Registers

Use auto calibration to set the nominal error correction values in the correction (COR) registers. When auto calibration is terminated by releasing pin NCLB, the COR register values are automatically copied to the corresponding BASE registers.

Alternatively, the COR to BASE command (0x0A) can also be used to copy the COR register values to the corresponding BASE registers.

Configure the three limit (LIM) registers with the maximum parameter deviation that should be allowed for error correction.

Configure the desired action to take when this condition occurs using the **.adapt** status (bit 10) in the status registers. Store all these values to the internal EEPROM using one of the EEPROM write commands.

Temperature Monitor

The iC-TW39 provides an on-chip temperature sensor and monitor. An alarm status condition is activated when the chip temperature exceeds the configured alarm temperature.

T_NOW is a read-only register containing the current temperature of the iC-TW39 in tenths of degrees Celsius. The actual chip temperature in °C, *tnow* is calculated as

$$tnow[^\circ C] = \frac{T\_NOW}{10}$$

T_ALARM configures the alarm temperature in tenths of degrees Celsius. Its value is calculated as

$$T\_ALARM = 10 \cdot talarm[^\circ C]$$

where *talarm* is the actual alarm temperature in °C.

In operation, the status bit STAT_VAL.talarm is activated whenever T_NOW $\geq$ T_ALARM and deactivated whenever T_NOW < T_ALARM.

STATUS / FAULT MONITOR

Parameter	Value	Description	Comments
Status			
STAT_VAL.xxx *	0, 1	Status register (current); 1 = active	Controlled by iC-TW39.
STAT_LATCH.xxx *	0, 1	Status register (latched)	
Fatal Status			
STAT_FATAL.xxx *	0, 1	1 = Malfunction	Controlled by iC-TW39.
Status Control			
STAT_CFG.autoclr	1	BiSS nE/nW Autoclear = on	
	0	BiSS nE/nW active according to STAT_LATCH	
STAT_CFG.long	0	Fault indication at NERR = for duration of condition	
	1	Fault indication at NERR = prolonged by 40 ms	
STAT_CFG.filter	0	Status Event Filtering = off	
	1, 2, 3, 4	Status Event Filtering = 10 µs, 150 µs, 2.5 ms, 40 ms	
Watchdog			
WATCHDOG *	127	127 = Chip is running	Controlled by iC-TW39.
Status Evaluation and Action Masking			
STAT_SEL.xxx	0, 1	Selection of current or latched status (0 = current)	
STAT_IE.xxx	0, 1	Indication Enable for NERR (1 = enabled)	Recommended: .scamp = 1
STAT_HIZ.xxx	0, 1	ABZ/UVW Output Shutdown (1 = enabled)	
STAT_BE.xxx	0, 1	Indication of Latched Status on BiSS error bit	Recommended: .irq = 1
STAT_BW.xxx	0, 1	Indication of Latched Status on BiSS warning bit	

*) These registers are not stored in the chip's EEPROM.

Table 22: <Status and Fault Monitor>

Status Register

STAT_VAL contains bits that indicate the current status of the signal path. These bits are active for the duration of the specified condition. This register is also available at addresses 0x4C and 0x4D in the BiSS slave register.

STAT_VAL and **STAT_LATCH**		
Bit	Name	Description
15	talarm	Temperature alarm
14	–	Not in use
13	irq	NERR fault input/output active
12	adiwrn	Absolute data interface warning
11	adierr	Absolute data interface fault
10	scamp	Input amplitude out of range
9	adapt	Adaption limit exceeded
8	resi	Correction residue threshold exceeded
7	–	Not in use
6	match	ADI revolution count mismatch
5	vsync	Velocity too high for synchronization
4	lagfatl	Fatal position lag
3	alim	Excessive acceleration
2	vlim	Excessive velocity
1	falarm	Input frequency alarm
0	oflow	Signal path overflow

Table 23: Status Register

STAT_VAL.talarm indicates that chip temperature is above the limit set in the T_ALARM register.

STAT_VAL.irq indicates that the NERR input/output is active (low) due either to an internal condition or to external activation of the NERR input/output. When pin NERR is low, STAT_VAL.irq = 1. See Evaluation of I/O pin NERR on page 45 for more information.

With the ADI in use, **STAT_VAL.adierr** and **.adiwrn** indicate that the error (nE) bit and the warning (nW) bit in the ADI data frame is active (0) or that the external multiturn sensor is not ready.

STAT_VAL.scamp indicates that the sin/cos vector amplitude (calculated by $\sqrt{sin^2 + cos^2}$) is outside the allowed tolerance of 50 % to 120 %.

See Sensor Amplitude Monitor on page 39 for more information.

STAT_VAL.adapt indicates that one or more of the correction parameters has deviated from its base value by more than its specified limit.

STAT_VAL.adapt		
Correction Register	Base Register	Limit Register
S_OFS_COR C_OFS_COR	S_OFS_BASE C_OFS_BASE	SC_OFS_LIM
SC_BAL_COR	SC_BAL_BASE	SC_BAL_LIM
SC_PH_COR	SC_PH_BASE	SC_PH_LIM

Table 24: Adaption Limit Exceeded

Specifically, whenever

$$|\text{S\_OFS\_COR} - \text{S\_OFS\_BASE}| > \text{SC\_OFS\_LIM}$$

$$|\text{C\_OFS\_COR} - \text{C\_OFS\_BASE}| > \text{SC\_OFS\_LIM}$$

$$|\text{SC\_BAL\_COR} - \text{SC\_BAL\_BASE}| > \text{SC\_BAL\_LIM}$$

$$|\text{SC\_PH\_COR} - \text{SC\_PH\_BASE}| > \text{SC\_PH\_LIM}$$

See EXCESSIVE ERROR AND ADAPTION MONITOR on page 40 for more information.

STAT_VAL.resi indicates that one or more of the correction residue values has exceeded its alarm threshold.

STAT_VAL.resi	
Residue Register	Residue Threshold Register
S_OFS_RESI C_OFS_RESI	SC_OFS_TH
SC_BAL_RESI	SC_BAL_TH
SC_PH_RESI	SC_PH_TH
IA_PH_RESI	IA_PH_TH

Table 25: Correction Residue Threshold Exceeded

Specifically, whenever

$$|\text{S\_OFS\_RESI}| > \text{SC\_OFS\_TH}$$

$$|\text{C\_OFS\_RESI}| > \text{SC\_OFS\_TH}$$

$$|\text{SC\_BAL\_RESI}| > \text{SC\_BAL\_TH}$$

$$|\text{SC\_PH\_RESI}| > \text{SC\_PH\_TH}$$

$$|\text{IA\_PH\_RESI}| > \text{IA\_PH\_TH}$$

See EXCESSIVE ERROR AND ADAPTION MONITOR on page 40 for more information.

With the ADI in use, **STAT_VAL.match** indicates that the most recent data from an external multiturn position sensor did not match the internal revolution count (RC).

With the ADI in use, **STAT_VAL.vsync** indicates that iC-TW39 stopped the data synchronization to an external multiturn position sensor because the motor speed has exceeded the configured frequency limit.

STAT_VAL.lagfatl indicates a fatal lag condition at which all position outputs are invalid (unexpected direction reversal). This occurs if a .vlim status persists until the AB output position falls behind the input angle by more than 180 degrees.

STAT_VAL.alim indicates that the position lag is limited to a maximum of 22.5° due to excessive acceleration (e.g. due to an accidental motor blockage). This condition is not fatal and resolves with decreasing acceleration.

STAT_VAL.vlim indicates either that the AB output frequency is being limited (due to the configured AB_LIMIT), or the UVW output frequency exceeds 8.33 MHz. This condition is not fatal and the AB/UVW outputs are still valid, although if it persists, it will eventually cause a .lagfatl status condition.

STAT_VAL.falarm indicates that the motor speed exceeds the permissible maximum of 360 000 rpm.

STAT_VAL.oflow indicates that the signal path is saturated somewhere, most likely due to ADC overflow. This condition is not fatal, but does result in reduced interpolation accuracy.

Latched Status Register

STAT_LATCH contains the same status conditions as the STAT_VAL register, except that the bits are latched when activated and stay active until cleared. This register is also available at addresses 0x4E and 0x4F in the BiSS slave register.

Latched status bits can be cleared by writing 0 to the bit. Writing 1 to a bit does nothing, allowing bits to be cleared individually. Command 0x06 can be used to clear all latched status bits at once.

In addition, if BiSS nE/nW Autoclear is enabled (STAT_CFG.autoclr = 1), the STAT_LATCH register is cleared when either nE or nW has been active for at least one BiSS data frame. Note that the STAT_LATCH is set again if a condition persists.

If the optional Absolute Data Interface (ADI) is used, STAT_LATCH.adierr remains zeroed on startup until the first valid data frame is received from the ADI.

Fatal Status Register

STAT_FATAL contains bits that indicate fatal faults, and one bit that indicates the bootup state. The STAT_FATAL register is also available at addresses 0x50 and 0x51 in the BiSS slave register.

Any fatal fault will inhibit startup of the iC-TW39 or stop it during operation. Fatal faults also activate NERR, disable the ABZ and UVW outputs, activate the BiSS Error (nE) and Warning (nW) bits, and activate the fatal fault bit (fflt) in the SPI status byte.

Fatal fault conditions must be cleared either by cycling power, toggling the reset input (NRST), or using the start/restart command. See THE COMMAND REGISTER on page 36 for more information.

STAT_FATAL		
Bit	Name	Description
5	boot	Startup boot state active
4	interr	Internal chip fault
3	corchk	EEPROM correction values checksum fault
2	cfgchk	EEPROM configuration checksum fault
1	tune	EEPROM tuning values fault
0	ee2bit	EEPROM read double bit error

Table 26: Fatal Status Register

STAT_FATAL.boot indicates that the iC-TW39 startup sequence is in the bootup state.

STAT_FATAL.interr indicates that an internal fault occurred in the iC-TW39. The chip must be power-cycled to reset this condition.

STAT_FATAL.corchk indicates a checksum error of the correction parameters in the internal EEPROM. This fault is un-recoverable and the EEPROM must be re-programmed.

STAT_FATAL.cfgchk indicates a checksum error of the configuration parameters in the internal EEPROM. This fault is un-recoverable and the EEPROM must be re-programmed.

STAT_FATAL.tune indicates that the factory-set tuning parameters in the EEPROM have been corrupted. This fault is un-recoverable and the chip must be replaced.

STAT_FATAL.ee2bit indicates a double bit error occurred when reading the internal EEPROM. This fault is un-recoverable and the EEPROM must be re-programmed.

Status Control

A few general monitor configurations are available using **STAT_CFG**.

STAT_CFG.filter determines how long a status condition must have been continuously active before the corresponding bit in the STAT_VAL and STAT_LATCH registers is set. This filtering avoids nuisance tripping of the status bits.

STAT_CFG.long determines how long NERR is active when a configured status condition occurs. Prolonging NERR is useful to ensure that transient conditions are visible via the fault LED.

STAT_CFG.autoclr determines whether the BiSS error and warning bits (nE and nW) are automatically cleared after one BiSS data frame.
With autoclear disabled (by 0), the nE and nW bits remain active as long as any configured bit in the STAT_LATCH register is active. With autoclear enabled (by 1), the STAT_LATCH bits configured to activate nE (STAT_BE) and nW (STAT_BW) are cleared after every BiSS data frame. In this case, the nE or nW bits are active due to a configured STAT_LATCH condition for only one single-cycle data frame.

Watchdog

The **WATCHDOG** register is continuously updated by the iC-TW39 while it is operating correctly. Clear the watchdog register by writing 0 to it. After a minimum wait time of 1 ms, it should read 127 (0x007F) if the iC-TW39 is operating correctly. Any other value (0...126 or 128...65 535) indicates a serious internal malfunction.

Status Evaluation and Action Masking

The STAT_SEL, STAT_IE, STAT_HIZ, STAT_BW, and STAT_BE registers are mask registers configuring the desired alarm action to take when a status bit comes active. All mask registers use the same bit name extensions as those in the STAT_VAL register.

The evaluation logic for a single status bit is shown schematically in Figure 24. This logic is the same for all continuously monitored status conditions reported to the STAT_VAL register, except for the .irq bit. As the internal interrupt .irq reflects the I/O pin status of NERR, it is evaluated slightly differently as shown in Figure 25.

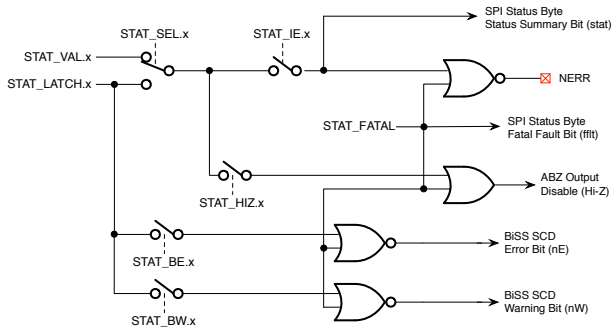


Figure 24: Single Condition Status and Fault Logic

Evaluation of I/O pin NERR

To allow the open-drain NERR pin to function as both a system error input (i.e. interrupt request input) as well as an output, the logic for the .irq status bit is slightly different.

As shown in Figure 25, the selected irq bit is not used to activate the NERR pin. This allows the NERR pin to be used as an interrupt request input in hosted applications where the host polls the SPI status byte. Note that STAT_FATAL bits can still activate the NERR output.

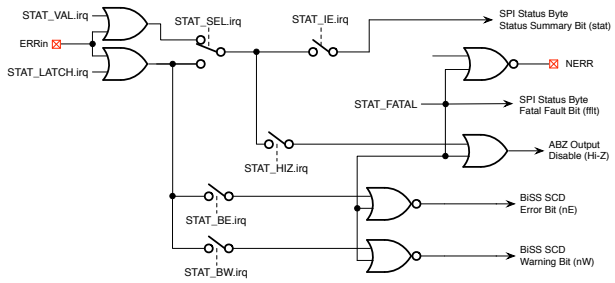


Figure 25: Interrupt Request Using NERR

Action Masking

The **STAT_SEL** register selects whether the dynamic status bits in STAT_VAL or the latched status bits in STAT_LATCH are used to alarm, i.e. to activate a fault LED connected at NERR.

If a given STAT_SEL bit is zero, the corresponding bit of the dynamic register STAT_VAL is used, otherwise the latched register STAT_LATCH.
In general, keeping STAT_SEL zeroed is recommended in stand-alone applications to obtain a dynamic non-latched LED indication.

The **STAT_IE** register enables (by 1) a current or latched status condition, as selected by STAT_SEL, to activate the fault output, NERR. An active fatal fault condition also activates the NERR output.

The **STAT_HIZ** register enables (by 1) a current or latched status bit, as selected by STAT_SEL, to shut down the ABZ/UVW outputs. Given this case, the ABZ/UVW outputs are in a high-impedance state.

The STAT_HIZ register provides an independent selection of which of the selected status conditions disable the ABZ/UVW outputs. Thus each status condition can be individually configured to activate the fault LED at NERR or disable the ABZ/UVW outputs, or both.

For the BiSS Interface, only the latched status conditions can be individually selected to set the active-low error (nE) and warning (nW) bits in the BiSS data frame. These bits can be configured to automatically clear, in which case they may be active for a single BiSS data frame only.

The **STAT_BE** register enables (by 1) a latched status bit in the STAT_LATCH register to activate the BiSS error bit, nE. The **STAT_BW** register enables (by 1) a latched status bit in the STAT_LATCH register to activate the BiSS warning bit, nW.
Note that an active fatal fault condition always activates both bits.

DEVICE IDENTIFICATION

Parameter	Value	Description	Comments
Identification Numbers			
SERIAL	...	Read-only Serial Number	Factory programmed.
CHIP_ID	0x001D	Chip Identification Number	
CHIP_REV	0x1031	Chip Revision Number	0x1031 = Y2
DEV_SN	0	Device Serial Number	
DEV_ID	0	Device ID	
MFR_ID	0	Manufacturer ID	

Table 27: <Device ID>

SERIAL is the unique, factory assigned, 32-bit serial number of each iC-TW39. This provides full traceability for tracking specific sensors or when contacting iC-Haus for support.

CHIP_ID is a read-only register containing the iC-TW39 chip ID for identification purposes.

CHIP_REV is a read-only register containing the iC-TW39 chip revision for identification purposes.

A user-defined device serial number of 6 bytes, a device ID of 4 bytes, and the BiSS device manufacturer ID (2 bytes) can be assigned to **DEV_SN**, **DEV_ID**, and **MFR_ID**. Refer to section User Data Registers for description.

EEPROM

Parameter	Value	Description	Comments
TEST.we	0	EEPROM Unlock 0 = locked (write protection enabled) 1 = unlocked (write protection disabled)	

Table 28: <EEPROM>

The iC-TW39 contains a built-in EEPROM for storage of configuration data. These values are read from the EEPROM automatically at startup and can be read and written using various commands.

The **TEST** register is *not* stored in EEPROM and is set to 0 at every startup. The EEPROM must be unlocked by **TEST.we = 1** to write to it using the COMMAND register.

The EEPROM can also be written at the rising edge of the NCLB input regardless of the value of TEST.we. See AUTO CALIBRATION AND ANGLE ERROR CORRECTION on page 37 for more information.

PROGRAMMER's REFERENCE – REGISTER MAP

A complete memory map of the iC-TW39 is shown in Tables 29 and 30. Register features are shown in the Type column as follows:

E indicates that the register value is stored in the internal EEPROM and restored at startup or restart. Unless otherwise stated, these registers may be written by the user via the BiSS, SPI, or Encoder Link interfaces, but the modified values are not automatically stored to the EEPROM.

D indicates that the register is dynamic; its value may be modified by the iC-TW39 during operation. The user may also write to these registers to override the calculated value.

R indicates that the register is dynamic and read-only. Its value may be modified by the iC-TW39 during operation but cannot be modified by the user.

V indicates that the register is read / write and volatile. The values are not stored in the EEPROM.

Registers without a code in the Type column may be read and written by the user.

Registers not shown are reserved and must not be accessed.

Address	Register Name	Description																Type
		Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0x0000	MAIN_CFG	0	0	0	0	1	0	nio			0 1		0	0	1	0 1		E
0x0008	ABZ_CFG	0	0	0	0	1	zpol	bpol	apol	dir	zwidth		1 0		0	0 1		E
0x000A	ABZ_RES[15:0]	AB Output Resolution (LSW)																E
0x000C	ABZ_RES[19:16]	Must be 0												AB Output Resolution (MS Bits)				E
0x000E	ABZ_PH	ABZ phase shift (0...65 535)																E
0x0010	AB_LIMIT	AB frequency limit																E
0x0012	UVW_CFG										pol	dir	pairs					E
0x0016	UVW_PH	UVW phase shift (0...65 535)																E
0x0018	BISS_CFG0								ssi	at	dir	0 0		mtlen				E
0x001A	BISS_CFG1											1		0 0		bp		E, D
0x001C	BISS_RES[15:0]	BiSS Singleturn Resolution (Increments per Revolution) LSW																E
0x001E	BISS_RES[25:16]	Must be 0						BiSS Singleturn Resolution (Increments per Revolution) MS Bits										E
0x0020	BISS_NRPPH[15:0]	BiSS Angle Preset Phase Shift (LSW)																E, D
0x0022	BISS_NRPPH[25:16]	Must be 0						BiSS Angle Preset Phase Shift (MS Bits)										E, D
0x0024	BISS_RCPPH[15:0]	BiSS Multiturn Preset Phase Shift (LSW)																E, D
0x0026	BISS_RCPPH[31:16]	BiSS Multiturn Preset Phase Shift (MSW)																E, D
0x0028	BISS_DLEN	Must be 0										BiSS Data Length						R
0x002A	BISS_CFG2															passmode		V
0x002E	BISS_PASS	rd	BiSS register address							BiSS register data								D
0x0042	BISS_KEY	BiSS Register Protection Key																
0x0054	TEST																we	
0x0100	STAT_CFG												autoclr	long	filter			E
0x0102	STAT_SEL	talarm	cl	irq	adiwrn	adierr	scamp	adapt	resi	zero	match	vsync	lagfatl	alim	vlim	falarm	oflow	E
0x0104	STAT_IE	talarm	cl	irq	adiwrn	adierr	scamp	adapt	resi	zero	match	vsync	lagfatl	alim	vlim	falarm	oflow	E
0x0106	STAT_HIZ	talarm	cl	irq	adiwrn	adierr	scamp	adapt	resi	zero	match	vsync	lagfatl	alim	vlim	falarm	oflow	E
0x0108	STAT_BE	talarm	cl	irq	adiwrn	adierr	scamp	adapt	resi	zero	match	vsync	lagfatl	alim	vlim	falarm	oflow	E
0x010A	STAT_BW	talarm	cl	irq	adiwrn	adierr	scamp	adapt	resi	zero	match	vsync	lagfatl	alim	vlim	falarm	oflow	E
0x010E	STAT_VAL	talarm	cl	irq	adiwrn	adierr	scamp	adapt	resi	zero	match	vsync	lagfatl	alim	vlim	falarm	oflow	D
0x0110	STAT_LATCH	talarm	cl	irq	adiwrn	adierr	scamp	adapt	resi	zero	match	vsync	lagfatl	alim	vlim	falarm	oflow	D
0x0112	STAT_FATAL											boot	interr	corchk	cfgchk	tune	ee2bit	D
0x0114	STAT_START													abs	rel	run	boot	D
0x0200	ADI_CFG													biss	0	mode	freq	E
0x0202	ADI_LEN				rc				000			sgap				fbk		E
0x0400	IPO_CFG													dir	0	01		E
0x0700	GB_CFG								0	clear		rclen				syncbits		E
0x0708	HYST										Output Hysteresis							E
0x4000	COMMAND									Command register								D
0x4004	ADAPT_CFG										iacal=1	1	11		1	1	1	E
0x4006	CALIB_CFG							0 0		gppre	1	1	0	inl	0	0	1	E
0x4008	T_ALARM	Alarm Temperature (–500...1500)																E
0x400C	SC_AMP_LOW	Must be 0				Weak Signal Threshold (0...SC_AMP_TARG)												E
0x4010	SC_OFS_LIM	Must be 0						Sin/Cos digital offset limit (0...2047)										E
0x4012	SC_OFS_TH	Must be 0						Sin/Cos offset residue threshold (0...2047)										E
0x4014	SC_BAL_LIM	Must be 0						Sin/Cos balance limit (0...2047)										E
0x4016	SC_BAL_TH	Must be 0						Sin/Cos balance residue threshold (0...2047)										E
0x4018	SC_PH_LIM	Must be 0						Sin/Cos phase limit (0...2047)										E
0x401A	SC_PH_TH	Must be 0						Sin/Cos phase residue threshold (0...2047)										E
0x401C	IA_PH_TH	Must be 0						Interpolated angle phase residue threshold (0...2047)										E
0x401E	S_OFS_BASE	Sine offset base value (±2047)																E
0x4020	C_OFS_BASE	Cosine offset base value (±2047)																E
0x4022	SC_BAL_BASE	Sin/Cos balance base value (±2047)																E
0x4024	SC_PH_BASE	Sin/Cos phase base value (±2047)																E
0x4026	S_OFS_COR	Sine digital offset correction value (±2047)																E, D
0x4028	S_OFSA_COR	Sine analog offset correction value (±31)																E, D
0x402A	C_OFS_COR	Cosine digital offset correction value (±2047)																E, D
0x402C	C_OFSA_COR	Cosine analog offset correction value (±31)																E, D
0x402E	SC_BAL_COR	Sin/Cos balance correction value (±2047)																E, D

Table 29: Register Map

Address	Register Name	Description															Type
		Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0x4030	SC_GN_COR	Must be 0				Sin/Cos digital gain correction value (0...4095)												E, D
0x4032	SC_GNA_COR	Must be 0											Sin/Cos analog gain correction value (0...23)					E, D
0x4034	SC_PH_COR	Sin/Cos phase correction value (±2047)																E, D
0x403C	SERIAL[15:0]	Chip serial number (LSW)																R
0x403E	SERIAL[31:16]	Chip serial number (MSW)																R
0x4048	SC_AMP	Sin/Cos vector amplitude (0...4095)																R
0x404E	S_OFS_RESI	Sine offset residue (±2047)																R
0x4050	C_OFS_RESI	Cosine offset residue (±2047)																R
0x4052	SC_BAL_RESI	Sin/Cos balance residue (±2047)																R
0x4054	SC_PH_RESI	Sin/Cos phase residue (±2047)																R
0x4058	IA_PH_RESI	Interpolated angle phase residue (±2047)																R
0x405E	S_OFS_MAX	Maximum sin offset residue (±2047)																D
0x4060	C_OFS_MAX	Maximum cos offset residue (±2047)																D
0x4062	SC_BAL_MAX	Maximum sin/cos balance residue (±2047)																D
0x4064	SC_PH_MAX	Maximum sin/cos phase residue (±2047)																D
0x4066	IA_PH_MAX	Maximum IA phase shift residue (±2047)																D
0x4068	T_NOW	Current Chip Temperature (–500...1500)																R
0x4094	PROFILE	BiSS Profile ID																E, D
0x4096	DEV_SN[15:0]	Serial Number[23:16] (User-defined device serial number)								Serial Number[31:24] (User-defined device serial number)								E
0x4098	DEV_SN[31:16]	Serial Number[7:0] (User-defined device serial number)								Serial Number[15:8] (User-defined device serial number)								E
0x409A	DEV_ID[15:0]	Device ID[39:32] (User-defined device ID)								Device ID[47:40] (User-defined device ID)								E
0x409C	DEV_ID[31:16]	Device ID[23:16] (User-defined device ID)								Device ID[31:24] (User-defined device ID)								E
0x409E	DEV_ID[47:32]	Device ID[7:0] (User-defined device ID)								Device ID[15:8] (User-defined device ID)								E
0x40A0	MFR_ID	Manufacturer ID[7:0] (User-defined manufacturer ID)								Manufacturer ID[15:8] (User-defined manufacturer ID)								E
0xE000	CHIP_ID	iC-TW39 Chip ID																R
0xE002	CHIP_REV	iC-TW39 Chip Revision																R

Table 30: Register Map (continued)

PROGRAMMER's REFERENCE – SPI COMMUNICATION

The SPI port is a 4-wire slave interface which operates in CPOL = 0 and CPHA = 0 mode only. This means that the base (resting) value of SCLK is low, SI is sampled on the rising edge of SCLK, and SO is changed on the falling edge of SCLK. The active-low Slave Select input, NCS, is used by the host processor to enable the SPI port to initiate communication.

SPI communication uses an overlapped packet protocol where the response to a command is returned while the next command is being sent. Figure 26 shows this for a single-device application, where the host controls a single iC-TW39 slave (see Figure 11).

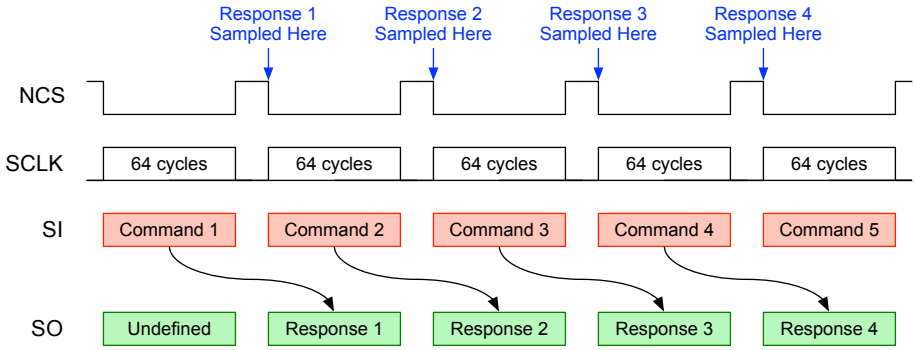


Figure 26: SPI Overlapped Packet Protocol

SPI command and response packets are always 64 bits long and are sent most-significant bit first. The host initiates communication with the iC-TW39 by driving Slave Select (NCS) low and then clocking a 64-bit packet (Command 1) to the Slave Input, SI. The host drives NCS high at the end of the command packet and the iC-TW39 executes the command.

After waiting for the command to be executed, the host again drives NCS low and sends the next packet (Command 2) to SI while at the same time reading the 64-bit response (Response 1) to the initial command on the Slave Output, SO.

The iC-TW39 always returns a response packet while reading a command packet. The response packet returned while writing the first command packet is not defined.

A simpler non-overlapped protocol that is easier to implement in the host processor can be used when high SPI bandwidth is not necessary. With this protocol, every other command and response is ignored, as shown in Figure 27.
This provides a more straightforward write-read-write-read protocol, but at half the maximum bandwidth of the overlapped packet protocol. Note that any command can be specified instead of the alternating null write, but a null write (64 zeroes) is easy to implement in the host processor.

Note: The host must not pulse NCS low without shifting 64 bits of data into SI. Doing so will cause unpredictable results and an unstable device. After the host drives NCS low, 64 SCLKs *must* be received by the iC-TW39 before NCS is driven high again.
Note: NCS must also be high when NRST is released.

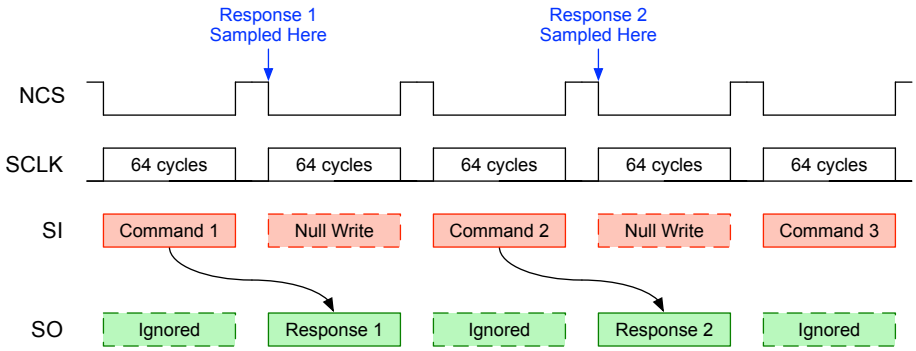


Figure 27: Simple SPI Protocol

The available commands are shown in Figure 28 and explained in detail on the following pages.

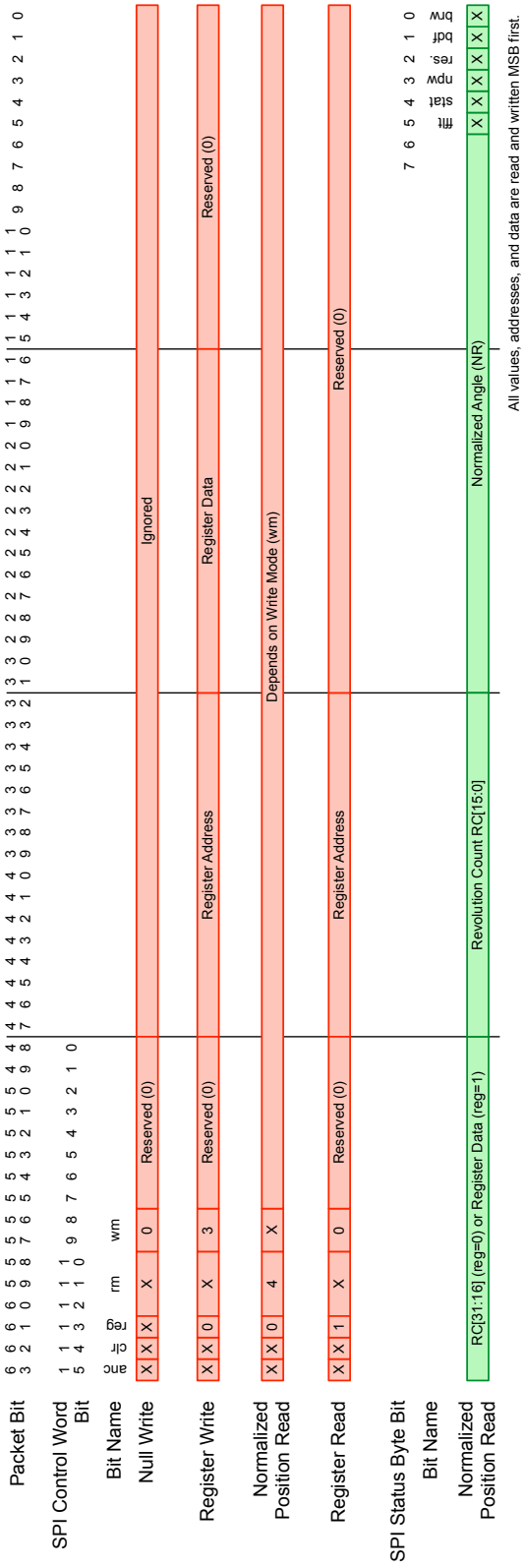


Figure 28: SPI Command Reference

SPI Command Packet Formats

SPI command packets are formatted as shown in Figure 29.

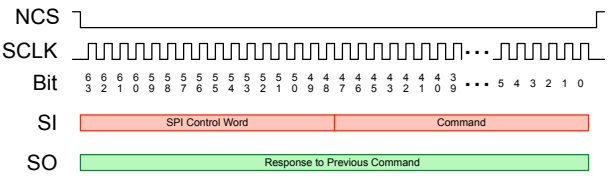


Figure 29: Command Packet Format

SPI Control Word

The SPI control word is the first 16 bits of every SPI command packet.

Command Bit	SPI Control Word		
	Bit	Name	Description
63	15	anc	Set anchor position
62	14	clr	Clear npw and bdf bits
61	13	reg	Register write
60:58	12:10	rm	Read mode
57:56	9:8	wm	Write mode
55:48	7:0	–	Reserved (must be 0)

Table 31: SPI Control Word

The type of data written by the SPI command is determined by the write mode (wm) field in the SPI control word as shown below.

SPI Write Modes	
wm	Description
3	Register Write
0	Null Write (read only)

Table 32: SPI Write Modes

The type of data returned in the next response packet is determined by the read mode (rm) field and the reg bit in the SPI control word.

SPI Read Modes	
rm	Description
7...5	Reserved (do not use)
4	Position Read
3...0	Reserved (do not use)

Table 33: SPI Read Modes

All values are read on the falling edge of NCS. However, the internal update rates of the various values are different. In all cases, the value read is the most recently updated internal value. See Response Packet Formats on page 51 for more details on the internal update rates.

If reg = 1, register data is returned along with the data specified by the read mode field. See Register Read on page 52 for more information.

If clr = 1, the next falling edge of NCS also clears the npw and bdf bits in the SPI status byte.

Null Write (Read Only)

The Null Write command packet is formatted as shown below.

Null Write: wm = 0	
Bits	Description
63:48	SPI Control Word
47:0	Ignored

Table 34: Null Write Command Packet

The Null Write (Read Only) command does not write any data to the iC-TW39. The command bits in the command packet are ignored, but must be present to complete the 64-bit packet. The data specified by the read mode field in the control byte is returned with the next SPI command.

Register Write

The Register Write command packet is formatted as shown below.

Register Write: wm = 3	
Bits	Description
63:48	SPI Control Word
47:32	Register Address
31:16	Register Data
15:0	Reserved (must be 0)

Table 35: Register Write Command Packet

The specified register data is written to the register at the specified register address *and* the data specified by the read mode field in the control word is returned in the next response packet.

Response Packet Formats

The format of the response packet is determined by the read mode field and reg bit in the control byte of the previous command packet.

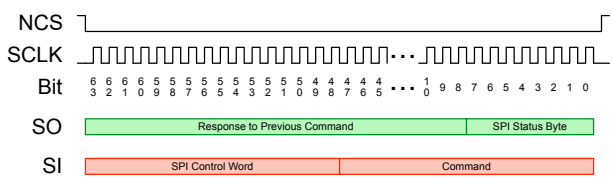


Figure 30: Response Packet Format

SPI Status Byte

The last six bits of every SPI response packet contain the six LSBs of the SPI status byte. The SPI status byte reports an active status or fatal fault condition as well as other conditions useful in hosted applications.

Response	SPI Status Word		
Bit	Bit	Name	Description
7:6	7:6	–	0 (Reserved)
5	5	fflt	Fatal fault occurred
4	4	stat	Active status condition
3	3	npw	New position written
1	1	bdf	New BiSS data frame
0	0	brw	BiSS read/write request

Table 36: SPI Status Byte

If fflt = 1, one or more of the bits in the STAT_FATAL register is set, indicating that a fatal fault occurred.

If stat = 1, one of the configured status conditions is active. See STATUS/FAULT MONITOR on page 42 for more information.

If npw = 1, the counter has been updated with new native position values (RC) from the absolute data interface.

If bdf = 1, a new BiSS SCD frame has been requested by the BiSS master.

If brw = 1, a BiSS register read or write has been requested by the BiSS master.

Position Read

The Position Read response packet is formatted as shown below.

Position Read Response: rm = 4	
Bits	Description
63:32	Revolution Count (RC)
31:6	Angle
5:0	SPI Status Byte [5:0]

Table 37: Position Read Response Packet

The position is updated internally every 20 ns and the position returned by the position read command is the most recently updated internal value, so it may be up to 20 ns old. In addition, the reported position may lag behind the actual sensor position due to signal path filter lag and operating conditions.

If the register read bit (reg) is set in the SPI control word, the 16 most significant bits of the revolution count are replaced by the requested register data. See Register Read on page 52 for more information.

Register Read
The Register Read response packet is formatted as shown below.

Register Read Response: reg = 1	
Bits	Description
63:48	Register Data Word
47:6	Data dependant on Read Mode (rm)
5:0	SPI Status Byte [5:0]

Table 38: Register Read Response Packet

The Register Data Word contains the value of the register at the address specified in the previous Register Read command packet. This value overwrites the 16 most significant bits of the Revolution Count data (rm ≠ 7).

DESIGN REVIEW: Function Notes

iC-TW39_Y2		
No.	Function, Parameter/Code	Description and Application Notes
–		None at time of release.

Table 39: Notes on chip functions regarding iC-TW39 chip revision Y2

REVISION HISTORY

Rel.	Rel. Date*	Chapter	Modification	Page
A1	2021-12-16		Initial release	all

Rel.	Rel. Date*	Chapter	Modification	Page
A2			Refer to the revision history of the release.	

Rel.	Rel. Date*	Chapter	Modification	Page
B1	2023-02-01	ELECTRICAL CHARACT.	Items 003, 005, 103, 104, 201, 204, 205: update of conditions and limits	8
		OPERATING REQ: BiSS Interface	Figures 3, 4 updated; Items moved: I001→I007, I008→I016	11
		ABZ OUTPUT	Figure 13 updated	21
		ABZ + UVW OUTPUT	Section added	23
		ORDERING INFORMATION	Section updated	55

Rel.	Rel. Date*	Chapter	Modification	Page
B2	2023-02-08	ELECTRICAL CONNECTIONS	Note added to Figure 9	14
		ANGLE PROCESSOR	Update of Figure 12	18

Rel.	Rel. Date*	Chapter	Modification	Page
B3	2024-03-15	FEATURES	INL is ±, added 20 MHz SPI interface	1
		DESCRIPTION	Revised	2
		PACKAGING INFORMATION	Update of footnotes: No. 1 added, former No. 8 removed (NPRE preset function is available)	5
		PACKAGE DIMENSIONS	Added information that the magnet must be centered over the TMR element, updated drawing	6
		OPERATING REQUIREMENTS: BiSS Interface	Item I011: update of limit Item I012: added	11
		DEVICE FUNCTIONS	Removed note that chip is not pre-programmed	16
		ANGLE PROCESSOR	Figure 12 updated	18
		BiSS/SSI INTERFACE	Updated note on SSI blind write capability	24
		BiSS ELECTRONIC DATA SHEET	Section added	29
		BiSS PASSTHROUGH MODE	Section added	31
		ABSOLUTE DATA INTERFACE (ADI)	Section added	33
		AUTO CALIBRATION AND ANGLE ERROR CORRECTION	Note added on INL reset	37
		PROGRAMMER	Added register type V Table 29: address 0x001A, bit 4: changed from 0 to reserved address 0x0008: Updated bits 15:11 address 0x0018: Updated bits 5:4	47
		PROGRAMMER	Table 30: addresses 0x002A and 0x002E added	48

Rel.	Rel. Date*	Chapter	Modification	Page
B4	2024-04-23	ABSOLUTE DATA INTERFACE (ADI)	Added parameter ADAPT_CFG.iacal to Table 13 and added parameter description	33, 34
		PROGRAMMER	Table 29: Registers 0x0200, 0x0202, 0x0400, 0x0700, 0x4004 added	47

* Release Date format: *YYYY-MM-DD*

ORDERING INFORMATION

Type	Package	Options	Order Designation
iC-TW39	32-pin QFN, 5 mm x 5 mm, thickness 0.9 mm, RoHS compliant		iC-TW39 QFN32-5x5
Evaluation Board	PCB module, size approx. 61 mm x 64 mm	Supplied with precision magnets and adapter cable	iC-TW39 EVAL TW39_1M
iC-TW39 GUI		Evaluation software for Windows PC (entry of IC parameters, file storage, and transfer to DUT)	For download link refer to www.ichaus.de/product/ic-tw39/

Please send your purchase orders to our order handling team:

Fax: +49 (0) 61 35 - 92 92 - 692
E-Mail: dispo@ichaus.com

For technical support, information about prices and terms of delivery please contact:

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