iC-MV 8-BIT HALL ENCODER WITH CASCADABLE SERIAL INTERFACE

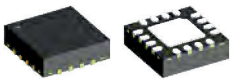
FEATURES

- Integrated Hall sensors with signal conditioning
- Automatic gain control with error detection (loss of magnet)
- 8-bit real-time interpolation for up to 24 000 rpm
- Binary interpolation factors from 2 to 8 bit
- Programmable zero position
- Cascadable serial shift register with SSI compatibility
- Bus-compatible EEPROM I^2C interface
- Space saving features: small 3 mm x 3 mm QFN package, magnet size of Ø 3 mm
- Standby mode
- Extended temperature range of -40...+125 °C

APPLICATIONS

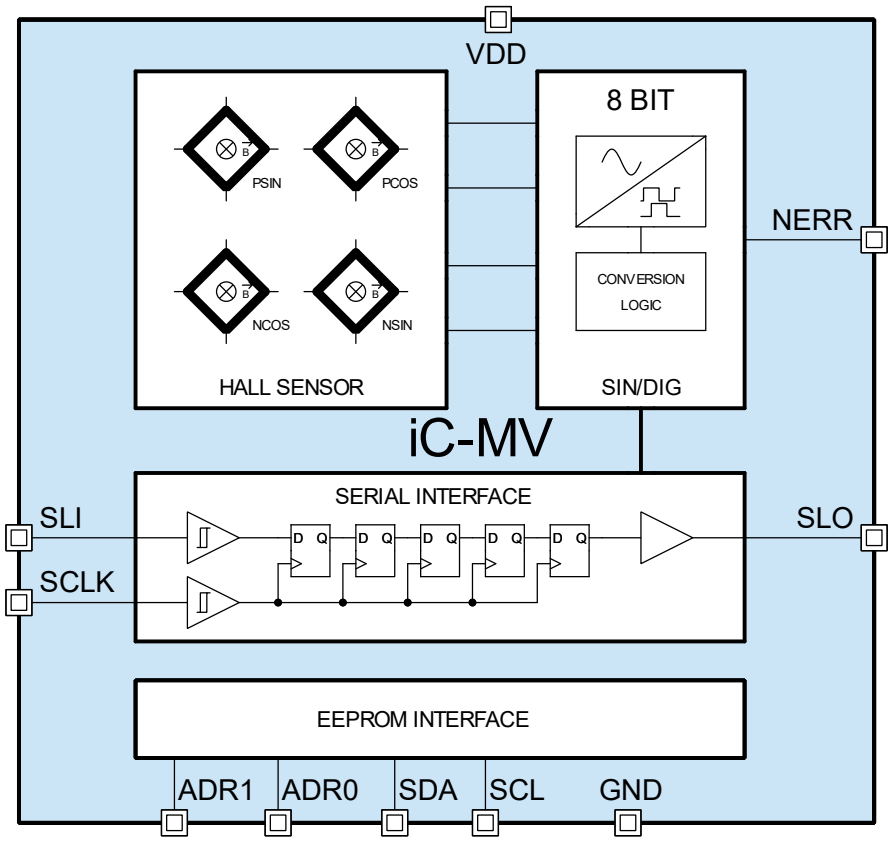
- Absolute multiturn encoders
- Absolute rotary encoders
- Contactless rotary switches

PACKAGES



QFN16
3 mm x 3 mm x 0.9 mm
RoHS compliant

BLOCK DIAGRAM



DESCRIPTION

Magnetic encoder iC-MV has been optimized for multiturn measuring systems with up to four dependent axes and gear reduction ratios of between 1:2 and 1:32.

The sensor generates one sine and one cosine cycle per revolution of the magnet, enabling the angle to be clearly determined by the integrated 8-bit sine-to-digital converter. The internal signal conditioning unit provides a constant signal level that is independent of the magnetic field strength, supply voltage, and temperature. A loss-of-magnet condition can be indicated at output NERR and via the serial interface (SSI protocol with an optional error bit).

Two to four iC-MVs can be connected in series using their SLI and SLO ports. During data transmission, the position data of the fastest turning iC-MV is sent to the next slowest device. This then corrects its position data to match that of the previous IC and sends this in protocol to the next slowest chip. This procedure provides the SSI master with a multiturn data word that is synchronized with itself. Furthermore, in place of mechanical phase alignment between the gear stages, iC-MV features an offset register to compensate for the phase angle electronically.

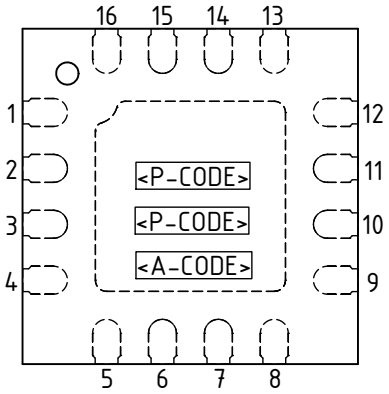
All inputs and outputs are protected against destruction by ESD (electrostatic discharge). For test purposes an electric signal coupling is possible at the integrated Hall sensors (e.g. in the ABZ operation).

General notice on application-specific programming
Parameters defined in the datasheet represent supplier's attentive tests and validations, but - by principle - do not imply any warranty or guarantee as to their accuracy, completeness or correctness under all application conditions. In particular, setup conditions, register settings and power-up have to be thoroughly validated by the user within his specific application environment and requirements (system responsibility).

CONTENTS

PACKAGING INFORMATION

PIN CONFIGURATION
QFN16 (3 mm x 3 mm)

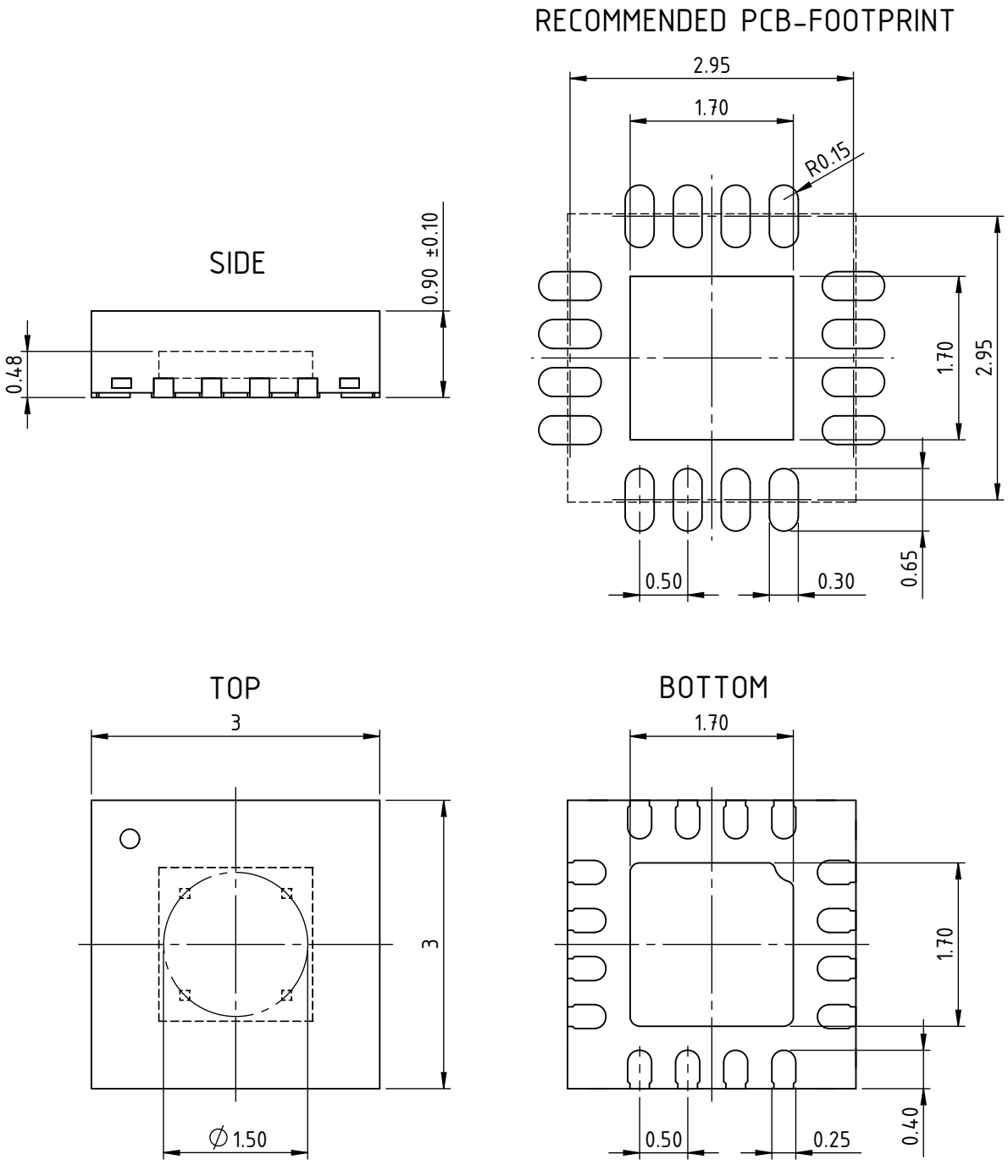


PIN FUNCTIONS

No.	Name	Function
1	n.c.[1]	
2	VDD	+4.5 V to +5.5 V Supply Voltage
3	NERR	Open Drain Error Output (NOSBY = 0x1), Standby Input (NOSBY = 0x0), Analog Output GAIN and NCOS
4	n.c.[1]	
5	ADR1	Address Pin 1 (active hi), Analog Input VTC (MODE)
6	ADR0	Address Pin 0 (active hi), Analog Input VTS (MODE)
7	n.c.[1]	
8	GND	Ground
9	n.c.[1]	
10	SDA	EEPROM Interface, I^2C Data Line
11	SCL	EEPROM Interface, I^2C Clock Line
12	n.c.[1]	
13	SLO	Serial Data Output (SSI), Analog Output PCOS (Analog Out), Threshold Output STOUT, Clock Output CLK (Digital Test), Incremental Output Z (ABZ Operation)
14	n.c.[1]	
15	SLI	Serial Data Input (SSI), Analog Output NSIN (Analog Out) and VREF (Digital Test), Incremental Output A (ABZ Operation)
16	SCLK	Serial Clock Input (SSI), Analog Output PSIN (Analog Out) and Analog Output GAIN (Digital Test), Incremental Output B (ABZ Operation)
	BP	Backside Paddle [2]

IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes);
1) Pin numbers marked n.c. are not connected.
2) Connecting the backside paddle is recommended by a single link to GND. A current flow across the paddle is not permissible.

PACKAGE DIMENSIONS



All dimensions given in mm.
Tolerance of sensor pattern: ±0.10mm / ±1° (with respect to center of backside pad).
Tolerances of form and position according to JEDEC MO-220.

drb_qfn16-3x3-1_mv_z1_pack_1, 15:1

ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these ratings device damage may occur.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	V()	Voltage at VDD		-0.3	6	V
G002	Vpin()	Voltage at ADR1, ADR0, SCL, SDA, SCLK, SLI, SLO, NERR		-0.3	6	V
G003	Imx(VDD)	Current in VDD		-10	20	mA
G004	Imx()	Current in ADR1, ADR0, SCL, SDA, SCLK, SLI, SLO, NERR		-10	10	mA
G005	Vd()	ESD Susceptibility at all pins	HBM, 100 pF discharged through 1.5 kΩ		2	kV
G006	Tj	Junction Temperature		-40	150	°C
G007	Ts	Chip Storage Temperature		-40	150	°C

THERMAL DATA

Operating conditions: VDD = 4.5...5.5 V

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range	QFN16-3x3 soldered to PCB according to JEDEC 51	-40		125	°C
T02	Rthja	Thermal Resistance Chip to Ambient	QFN16-3x3 soldered to PCB according to JEDEC 51		45		K/W

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating condition: VDD = 5 V ±10 %, Tj = -40...125 °C, 4 mm NdFeB magnet unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
General							
001	V(VDD)	Permissible Supply Voltage VDD		4.5		5.5	V
002	I(VDD)	Supply Current in VDD Normal Mode	normal mode (LOPM = 0x0), without load		4	6	mA
003	I(VDD)	Supply Current in VDD Low Power Mode	low power mode (LOPM = 0x1), without load		2	4	mA
004	I(VDD)	Supply Current in VDD	NOSBY = 0x0, NERR = lo, ENPU = 0x0		0.4	1.4	mA
005	Vc()hi	Clamp-Voltage hi at SLO, SDA, SCL, ADR0, ADR1, SLI, SCLK	Vc()hi = V() – V(VPD), I() = 1 mA	0.4		1.5	V
006	Vc()lo	Clamp-Voltage lo at SLO, NERR, SDA, SCL, ADR0, ADR1, SLI, SCLK	I() = -1 mA	-1.5		-0.3	V
Hall Sensor Array							
101	Hext	Permissible Magnetic Field Strength	at chip surface	20		100	kA/m
102	fmag	Operating Magnetic Field Frequency	LOPM = 0x0 LOPM = 0x1			400 50	Hz Hz
103	rpm	Rotating Speed of Magnet	LOPM = 0x0 LOPM = 0x1			24000 3000	rpm rpm
104	dsens	Diameter of Hall Sensor Circle			1.5		mm
105	xdis	Permissible Lateral Displacement of Magnet Axis to Center of Hall Sensors	4 mm magnet			0.2	mm
106	xpac	Displacement Chip Center to Package Center	package QFN16	-0.05		0.05	mm
107	ϕpac	Angular Alignment of Chip vs. Package	package QFN16	-0.6		0.6	deg
108	hpac	Distance Chip Surface to Package Surface	package QFN16		0.4		mm
Automatic Gain Control							
201	tampl	Settling Time of Gain Control	to 70 % of final amplitude		2	5	ms
202	V()gain	Gain Output Voltage	TEST = 0b001 measurable at NERR or TEST = 0b011 measurable at SCLK	0.1		3.5	V
Sine-to-Digital Converter							
801	RESsdc	Converter Resolution			8		bit
802	AAabs	Absolute Angular Accuracy	(LOPM = 0x00) Vpp(VTS, VTC) = 4 V calibrated	-2.8		2.8	deg
803	AAabs	Absolute Angular Accuracy	(LOPM = 0x01) Vpp(VTS, VTC) = 4 V calibrated	-3.5		3.5	deg
804	AArel	Relative Angle Error	(LOPM = 0x00) ideal input signals, quasi static	-15		15	%
805	AArel	Relative Angle Error	(LOPM = 0x01) ideal input signals, quasi static	-35		35	%
Power Down Reset							
901	Vref(SLI)	Reference Voltage	TEST = 0b011	45	50	55	%VDD
902	VDDon	Turn-on Threshold VDD (Power-Up-Enable)	increasing voltage	3.3	3.8	4.4	V
903	VDDoff	Turn-off Threshold VDD (Power-Down-Reset)	decreasing voltage	2.8	3.4	4.1	V
904	VDDhys	Turn-on Threshold Hysteresis		0.3			V
Serial Interface: SCLK, SLO, SLI							
A01	Vs()hi	Saturation Voltage hi	Vs()hi = V(VPD) – V(), I() = -1.6 mA			0.4	V
A02	Vs()lo	Saturation Voltage lo	I() = 1.6 mA			0.4	V
A03	Isc()lo	Short-Circuit Current lo	V() = VDD	10		90	mA
A04	Isc()hi	Short-Circuit Current hi	V() = 0 V	-90		-10	mA
A05	tr()	Rise Time at SLO	CL = 50 pF			60	ns
A06	tf()	Fall Time at SLO	CL = 50 pF			60	ns

ELECTRICAL CHARACTERISTICS

Operating condition: VDD = 5 V ±10 %, Tj = -40...125 °C, 4 mm NdFeB magnet unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
A07	Vt()hi	Threshold Voltage hi at SCLK, SLI				2	V
A08	Vt()lo	Threshold Voltage lo at SCLK, SLI		0.8			V
A09	Vt()hys	Threshold Hysteresis at SCLK, SLI		150	250		mV
A10	Ipu()	Pull-up Current at SCLK, SLI	V() = 1 V...VDD	-60	-30	-6	µA
A11	Vpu()	Pull-up Voltage at SCLK, SLI	Vpu() = VDD – V(), I() = -5 µA			0.6	V
A12	fin()	Permissible Clock Frequency at SCLK				2	MHz
A13	t_{tos}	SSI Timeout at SLO		14		29	µs
EEPROM Interface SCL, SDA, ADR0, ADR1							
B01	Vs()lo	Saturation Voltage lo at SCL, SDA	I() = 4 mA			0.4	V
B02	Isc()lo	Short-Circuit Current lo at SCL, SDA		10		90	mA
B03	Vt()hi	Input Threshold Voltage hi				2	V
B04	Vt()lo	Input Threshold Voltage lo		0.8			V
B05	Vt()hys	Input Hysteresis at SCL, SDA	Vt()hys = Vt()hi – Vt()lo	300	500		mV
B06	Vt()hys	Input Hysteresis at ADR0, ADR1	Vt()hys = Vt()hi – Vt()lo	150	250		mV
B07	Ipu()	Input Pull-up Current at SCL, SDA	V() = 0...VDD – 1 V	-60	-30	-6	µA
B08	Vpu()	Input Pull-up Voltage at SCL, SDA	Vpu() = VDD – V(), I() = -5 µA			0.6	V
B09	fclk()	Clock Frequency at SCL		50	80	100	kHz
B10	tbusy()cfg	Configuration Time	for a single iC-MV (chained iC-MV need to be added)	1	3	5	ms
B11	Ipd()	Pull-down Current Source at ADR0, ADR1	V() = 1 V...VDD	6	30	70	µA
Oscillator							
C01	fosc()	System Clock	TEST = 0b011, measured at pin SLO	0.8	1.1	1.6	MHz
Error Output / Standby Input NERR							
H01	Vs()lo	Saturation Voltage lo	I() = 4 mA			0.4	V
H02	Isc()lo	Short-Circuit Current lo	V() = VDD	5		80	mA
H03	Rpu()	Pull-up Resistor	ENPU = 0x1	7	11	15	kΩ
H04	Vt()hi	Input Threshold Voltage hi	NOSBY = 0x1			2	V
H05	Vt()lo	Input Threshold Voltage lo	NOSBY = 0x1	0.8			V
H06	Vt()hys	Threshold Hysteresis	NOSBY = 0x1, Vt()hys = Vt()hi – Vt()lo	150	250		mV

OPERATING REQUIREMENTS: Serial Interface (SSI)

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
SSI						
I001	t_{MAS}	Permissible Clock Period		500	t_{tos} *	ns
I002	t_{MASh}	Clock Signal hi Level Duration		250	0.5 x t_{tos}	ns
I003	t_{MASl}	Clock Signal lo Level Duration		250	0.5 x t_{tos}	ns

* Refer to Item No. A13.

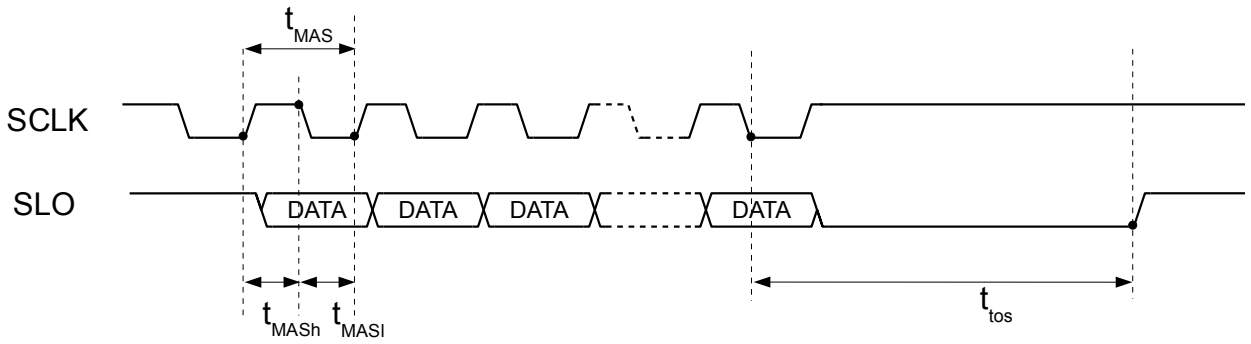


Figure 1: Timing SSI

CONFIGURATION

OFFSET: Position Offset (P. 14)
DIR: Code Direction (P. 14)
RNF: Edge of Data Output (P. 14)
EMODE: Error Bit Options (P. 15)
DL: Data Length (P. 15)
ERRSY: Synchronization Monitoring (P. 15)

NOSBY: Standby Enable (P. 15)
LOPM: Low Power Mode (P. 15)
ENPU: Pull-up Enable (P. 15)
SYNC: Position Data Synchronization (P. 16)
MODE: Operating Mode (P. 17)

OVERVIEW

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
iC-MV 1: ADDR = 0b00								
0x00	OFFSET(7:0)							
0x01	DIR	RNF	EMODE(2:0)			DL(2:0)		
0x02	ERRSY	NOSBY	LOPM	ENPU	SYNC	MODE(2:0)		
0x03	0x00							
iC-MV 2: ADDR = 0b01								
0x04	OFFSET(7:0)							
0x05	DIR	RNF	EMODE(2:0)			DL(2:0)		
0x06	ERRSY	NOSBY	LOPM	ENPU	SYNC	MODE(2:0)		
0x07	0x00							
iC-MV 3: ADDR = 0b10								
0x08	OFFSET(7:0)							
0x09	DIR	RNF	EMODE(2:0)			DL(2:0)		
0x0A	ERRSY	NOSBY	LOPM	ENPU	SYNC	MODE(2:0)		
0x0B	0x00							
iC-MV 4: ADDR = 0b11								
0x0C	OFFSET(7:0)							
0x0D	DIR	RNF	EMODE(2:0)			DL(2:0)		
0x0E	ERRSY	NOSBY	LOPM	ENPU	SYNC	MODE(2:0)		
0x0F	CRC(7:0) over Addr = 0x00 bis 0x0E							

Table 5: Register layout

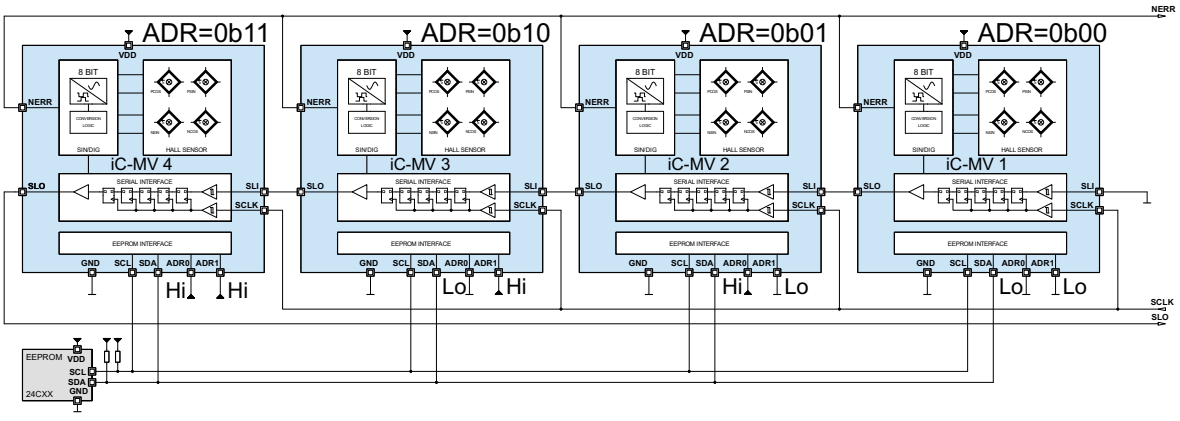


Figure 2: I²C Device Addressing

THE SENSOR PRINCIPLE

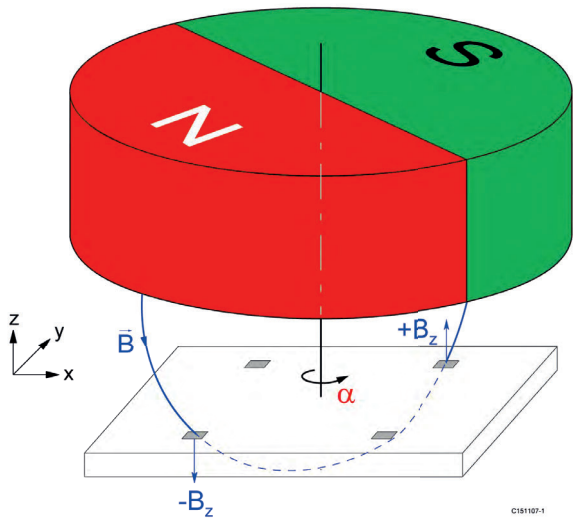


Figure 3: Sensor Principle

When combined with a rotating, permanent magnet and an EEPROM, iC-MV makes a complete encoder system. Ideal sensor signals are received when using a diametrically magnetized, cylindrical permanent magnet of neodymium iron boron (NdFeB) or samarium cobalt (SmCo). The magnet cylinder's diameter should be between of 2 mm to 4 mm.

iC-MV has four Hall sensors adapted to measure angles by converting the magnetic field into Hall voltages. Solely the magnetic field's z component is evaluated at which the field lines pass through two opposing sensors in opposite directions (see Figure 3). The arrangement of the Hall sensors has been specifically selected to allow a large tolerances in the assembly of iC-MV in relation to the magnet axis.

Differential Hall signals are generated by the combination of two Hall sensors each. When the magnet rotates around its longitudinal axis, sine and cosine voltages are generated which are used to determine the applied angle.

HALL SENSORS

The four Hall sensors are placed in the center of the QFN16 package in a circle with a diameter of 1.5 mm and have a 90 ° angle distance to one another.

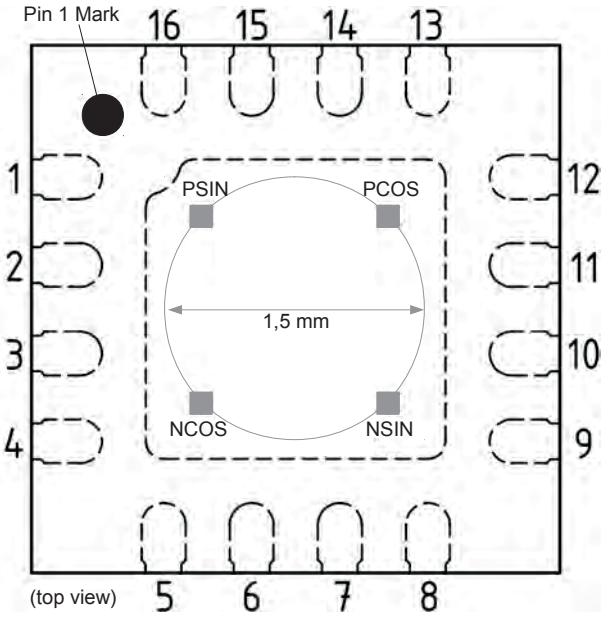


Figure 4: Position of the Hall sensors

When a magnetic south pole approaches the package surface the magnetic field shows a positive component in z direction (i.e. from the top of the package). The individual Hall sensors each generate their own positive signal voltage.

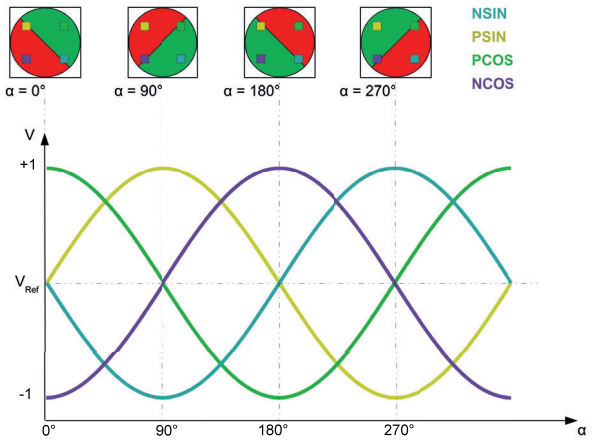


Figure 5: Analog Signals (single ended)

To determine the angle position of a diametrically polarized magnet placed above the device, the signal difference of the opposed Hall sensors is generated. This results in the sine being $V_{SIN} = V_{PSIN} - V_{NSIN}$ and the cosine being $V_{COS} = V_{PCOS} - V_{NCOS}$.

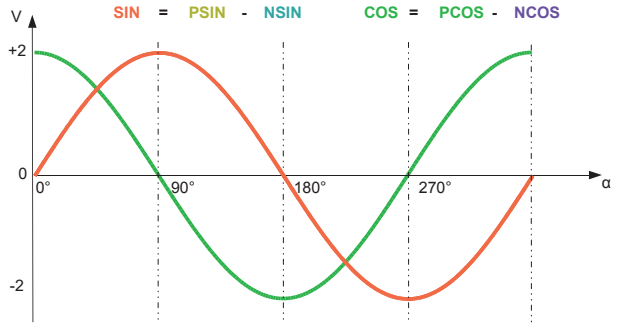


Figure 6: Analog Signals (differential)

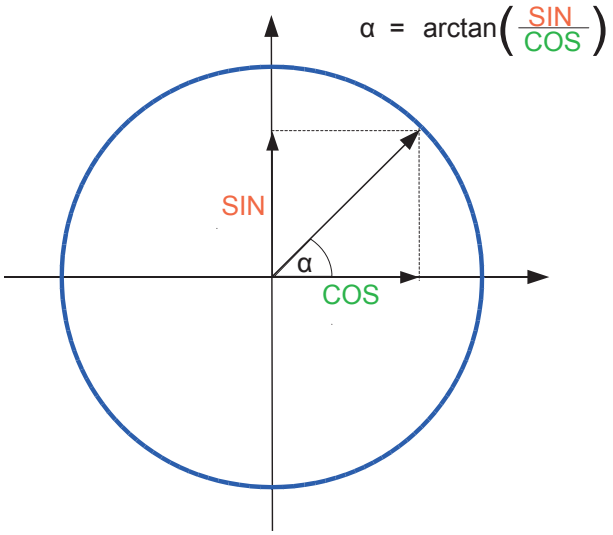


Figure 7: XY Plot and Angle Function

The magnet's zero angle position is characterized by the resulting cosine voltage value being maximized and the sine voltage value being zero.

With further clockwise rotation of the magnet the poles then overlap the PSIN and NSIN sensors so that the sine voltage value maximized. Sine and cosine signals are generated which represent the angle position of the magnet α (Figure 7).

All Hall sensor signals can be switched to the outside for test purposes.

This is the case when the magnet's south pole is located exactly above sensor PCOS and the north pole exactly above sensor NCOS. Sensors PSIN and NSIN are located along the pole threshold so that both do not generate a Hall signal.

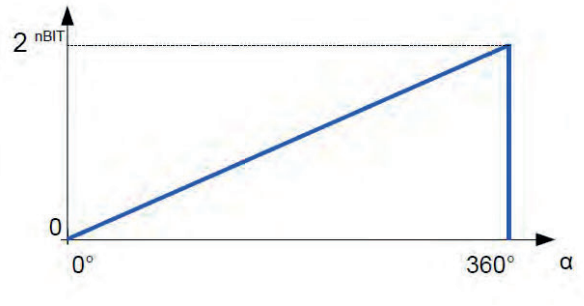


Figure 8: Converter Resolution

MULTITURN PRINCIPLE

iC-MV can form an absolute measuring system over several revolutions, through which the number of revolutions is saved in the gear. The singleturn's drive shaft activates the first axis in the gear. In the following example the transmission ratio between all axes is: *Ratio* = $\frac{1}{N}$.

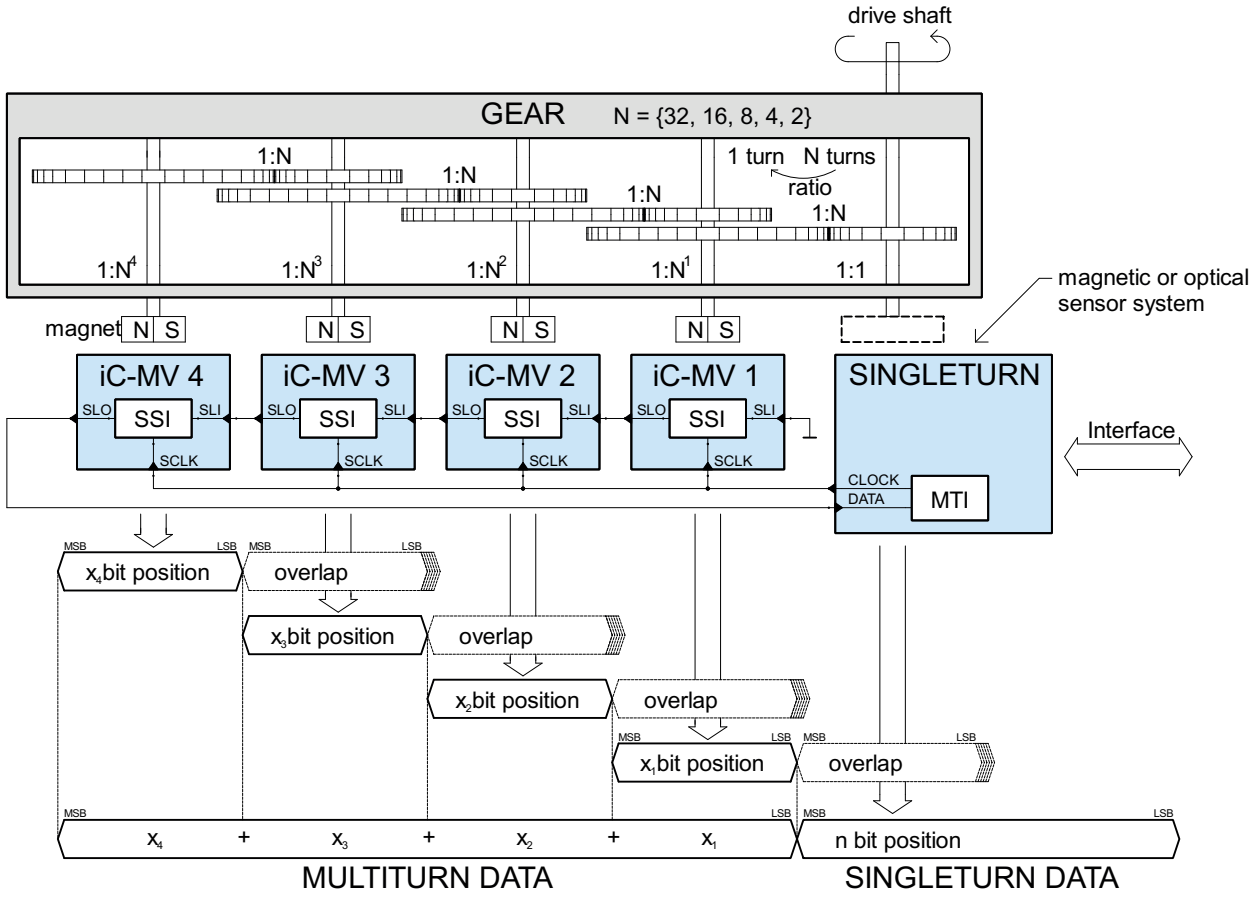


Figure 9: General System and Data Display

The iC-MVs connected together in series constitute a large serial shift register. The entire data length is dependent on the position data length of the individual iC-MVs and on the number of configured error bits, as well as on the number of iC-MVs existing in the system.

The individual iC-MVs' position data length is dependent on the gear axes' transmission ratio relative to one another. The fourth or last iC-MV in the chain is the first component to transmit its data.

REGISTERS

OFFSET(7:0): Position Offset
The content of the offset register is added to the current position. It allows the position data to be adjusted in a way that a synchronization of the position data is possible. The offset calculation is described in the chapter Synchronization and Calculation Example.

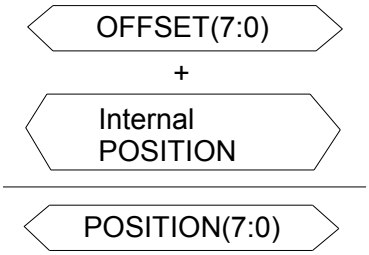


Figure 10: Offset Addition

OFFSET(7:0)	Addr. 0x0; bit 7:0
Code	Description
0x00	0
...	...
0x7F	127
...	...
0xFF	255

Table 6: Position Offset

DIR: Code Direction
The bit DIR inverts the position register's code direction and has to be inverted for the counter-rotating axes, so that all iC-MVs have the same code direction.

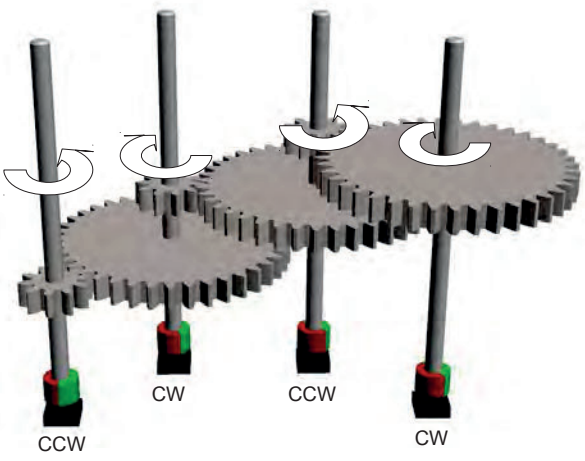


Figure 11: Code Direction

DIR	Addr. 0x1; bit 7
Code	Description
0x0	Code direction falling at clockwise rotation (CW)
0x1	Code direction falling at counterclockwise rotation (CCW)

Table 7: Code Direction

RNF: Edge of Data Output
In the SSI protocol, position data is usually output at the pin SLO with the rising clock edge of SCLK. In order to increase the calculation time for components in the chain, position data can be output with the falling clock edge.

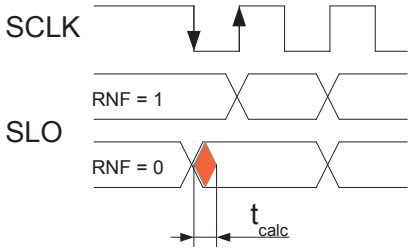


Figure 12: Increasing the Calculation Time

Chain components are to be configured with RNF = 0x0; only the last component (iC-MV 4, refer to Figure 9) is to be configured with RNF = 0x1.

RNF	Addr. 0x1; bit 6
Code	Description
0x0	falling edge
0x1	rising edge

Table 8: Edge of Data Output

EMODE(2:0): Error Bit Options
The EMODE indicates how a faulty condition is displayed. The configuration of the error bit options should be identical with all iC-MVs. If EMODE is configured with 0x01 or 0x03 an error bit is attached to the end of the position data. Each iC-MV modifies this error bit according to its error status. A faulty status is dominant. With EMODE = 0x07 or 0x05 each iC-MV complements its own error bit at the end of the sensor data.

EMODE(2:0)	Addr. 0x1; bit 5:3
Code	Description
0x00	No error bit
0x01	1 serial error bit lo active
0x03	1 serial error bit hi active
0x05	n serial error bit lo active
0x07	n serial error bit hi active

Table 9: Error Bit Options

Note:
If EMODE is configured with 0x01 the SLI pin of iC-MV1 has to be left open or connected to VDD. If EMODE is configured with 0x03 the SLI pin of iC-MV1 has to be connected to GND.

DL(2:0): Data Length
The data length indicates how many positions of the position register are clocked out. The data length of the first iC-MV in the chain can be set to a bigger value because of the singleturn synchronisation.

DL(2:0)	Addr. 0x1; bit 2:0
Code	Description
0x00	DL + 1 = 1 bit*
...	...
0x02	DL + 1 = 3 bit
0x03	DL + 1 = 4 bit
0x04	DL + 1 = 5 bit
...	...
0x07	DL + 1 = 8 bit
Note	*) Do not use DL = 0x00 for ABZ interface.

Table 10: Data Length

ERRSY: Synchronization Monitoring
If the data length is programmed to 4 bit (DL = 0x03) the synchronization monitoring can activated via bit ERRSY. In this case the error/warning bit will be set if the edge of the permissible synchronizing range is reached or exceeded because the position data is possibly not consistent.

ERRSY	Addr. 0x2; bit 7
Code	Description
0x0	Synchronization monitoring deactivated
0x1	Synchronization monitoring activated

Table 11: Synchronization Monitoring

NOSBY: Standby Enable
If the NOSBY bit is not set, iC-MV can be switched to standby operation by switching NERR to lo. The position data is thereby maintained. In order to save energy, the additional pull up resistor should be switched off via Bit ENPU. In case of a faulty configuration, iC-MV remains in standby enable. If the NOSBY bit is set, a loss-of-magnet condition will be indicated at output NERR.

NOSBY	Addr. 0x02; bit 6	
Code	Pin function NERR	Condition
0x00	Standby input (lo active)	ENPU = 0x0
0x01	Error output (lo active)	ENPU = 0x1

Table 12: Standby Enable

LOPM: Low Power Mode
The low power mode minimizes the sampling rate and thereby reduces the current consumption of iC-MV to approx. 2 mA. For a faster start-up the low power mode is deactivated until the gain control is engaged. While settling, the supply power is specified according to Item No. 002.

LOPM	Addr. 0x2; bit 5
Code	Description
0x0	Low power mode deactivated
0x1	Low power mode activated

Table 13: Low Power Mode

ENPU: Pull-up Enable
Pin NERR has an pull up Resistor of approx. 200 kΩ. Bit ENPU activates an additional pull-up resistor of approx. 11 kΩ at pin NERR.

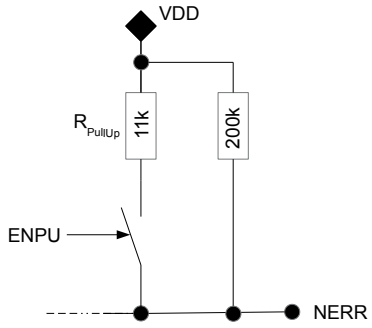


Figure 13: Pull-up Resistor

ENPU	Addr. 0x02; bit 4	
Code	Pin function ENPU	Condition
0x00	Pull-up deactivated	NOSBY = 0x0
0x01	Pull-up activated	NOSBY = 0x1

Table 14: Pull-up Enable

SYNC: Position Data Synchronization
The SYNC bit activates the synchronization of the position data. If the SYNC bit is deactivated, the position data is output unaltered.

SYNC	Addr. 0x2; bit 3
Code	Description
0x0	Synchronization deactivated
0x1	Synchronization activated
Note	SYNC = 0x1 shifts the zero pulse in ABZ operation to a length of 180 °.

Table 15: Position Data Synchronization

Note:
The calculated offset correction is essential to allow a successful synchronization.

MODE(2:0): Operating Mode
For testing of individual functions, several operating modes are built in and can be selected via the MODE register. In Mode Analog Output, Digital Test, Function Test and Converter Test, a test voltage can be applied to ADR0 and ADR1 alternatively to magnetic stimulation. In this case, a sinus test voltage VTS is applied to pin ADR0 and a cosine test voltage VTC is applied to pin ADR1 with an amplitude of Vpp(VTS, VTC) of 0.1 V .. 4.5 V.

Output signals according to operating mode									
Operating Mode	MODE(2:0)	**Pin ADR0**	**Pin ADR1**	**Pin SLI**	**Pin SCLK**	**Pin SLO**	**Pin SDA**	**Pin SCL**	**Pin NERR**
Normal Operation	0x00	ADR0	ADR1	SLI	SCLK	SLO	SDA	SCL	NERR
Adjustment	0x01	ADR0	ADR1	SLI	SCLK	SLO	SDA	SCL	GAIN
Analog Out	0x02	VTS	VTC	NSIN	PSIN	PCOS	SDA	SCL	NCOS
Digital Test	0x03	VTS	VTC	VREF	GAIN	CLK	0	0	NERR
Function Test	0x04	VTS	VTC	SLI	SCLK	SLO	SDA	SCL	NERR
Threshold Test	0x05	ADR0	ADR1	SLI	SCLK	STOUT	SDA	SCL	NERR
Converter Test	0x06	VTS	VTC	A	B	Z	SDA	SCL	NERR
ABZ Operation	0x07	ADR0	ADR1	A	B	Z	SDA	SCL	NERR

Table 16: Operating Modes

- **Normal Operation**
  If MODE is programmed to 0x00, iC-MV runs in normal operation. iC-MV is addressed via ADR(1:0). The position data can be read via the pin SLO and the pin NERR is configured as standby enable. The signal feed occurs magnetically.

- **Adjustment**
  MODE = 0x01 is used for adjustment. Thereby the automatic gain control's signal gain is output as voltage at the pin NERR. This process can be used as a distance control. The pull-up resistor should be switched off via the ENPU bit.

- **Analog Out**
  With MODE = 0x02, sine and cosine voltage signals Vpp(VTS, VTC) can be introduced to the Hall sensors via the pins ADR1(VTC) and ADR0(VTS). The required offset signal is first measured at ADR1 and ADR0. In analog out operation the sine/cosine signals are made available in front of the interpolator at the pins SLI, SCLK, SLO, and NERR.

- **Digital Test**
  For testing the saturation voltage, pins SDA and SCL are set to 'lo' in MODE = 0x03. The oscillator clock, V(Vref) and the gain signal are made available. CLK, gain and VREF can be measured in the digital test. The gain signal can be monitored when applying the VTS and VTC voltages.

- **Function Test**
  In MODE = 0x04, signals are fed in via ADR1 and ADR0 just like in MODE = 0x02. The function test has the same feature as the normal operation, however, the signal feed occurs electrically. In this test operation e.g. the interpolator can be tested.

- **Threshold Test**
  MODE = 0x05 can be used to test the input circuit threshold. NOSBY bit has to be programmed to 0x0 so that the NERR pin is configured as an input. In this operating mode, the threshold of the pins is tested. The input pins' thresholds can be determined at STOUT.

- **Converter Test**
  With MODE = 0x06 the converter test is activated. Sine and cosine voltage signals are introduced via ADR1 and ADR0 and the incremental signals are output at SLI, SCLK, and SLO.

- **ABZ Operation**
  MODE = 0x07 has the same function as the normal operation. The position output occurs incrementally at pins SLI, SCLK, and SLO. NOSBY bit has to be programmed to 0x1 so that the NERR pin is configured as an output.

EEPROM INTERFACE AND iC-MV ADDRESSING

An external EEPROM is required for the configuration of iC-MV. In the typical multiturn application, up to four iC-MVs share one EEPROM. iC-MV 1 is assigned with a low level at pins ADR1 and ADR0. Thus, 0b00 is the address of the first iC-MV in the SSI chain. iC-MV 2 is assigned with a low level at ADR1 and a high level at ADR0 and hence the address 0b01 (see Figure 2). The addresses for following iC-MVs can be generated from Table 18 according to this principle.

Depending on the address, each iC-MV has a different address range for its configuration. At address 0xF, the CRC checksum (polynomial 0x11D / start value = 1) is valid for the entire 15 bytes. Each iC-MV checks this CRC byte. In case of an error, the reading process is restarted. Pin SLO provided by the SSI interface and pin NERR are at a high level until a successful start-up (CRC check OK) is reached.

At the beginning of every communication eight bus cleaning cycles are run through, i.e. stop sequences are sent in order to reset a possibly remaining slave.

Pin ADR1	Pin ADR0	EEPROM Address Range
lo	lo	iC-MV 1: 0x00 - 0x03
lo	hi	iC-MV 2: 0x04 - 0x07
hi	lo	iC-MV 3: 0x08 - 0x0B
hi	hi	iC-MV 4: 0x0C - 0x0F

Table 17: Address Range

iC-MV Addressing				
Number of iC-MV	1	2	3	4
iC-MV 1	0b00			
iC-MV 2		0b01		
iC-MV 3			0b10	
iC-MV 4				0b11

Table 18: Address Allocation

SERIAL INTERFACE (SSI)

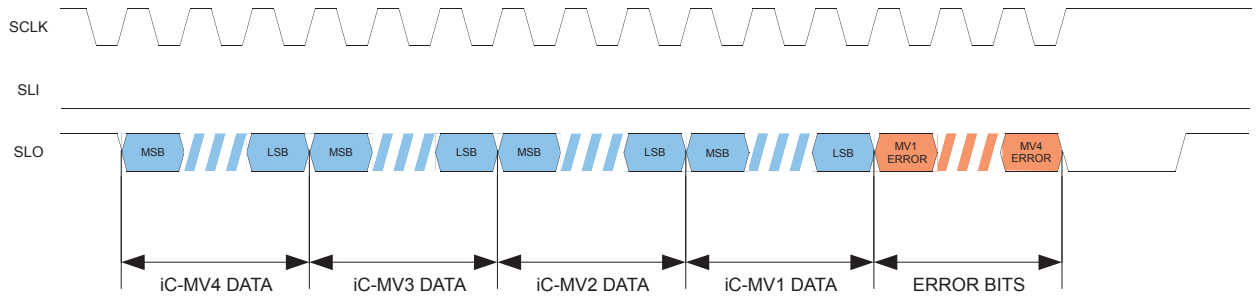


Figure 14: SSI protocol

Two to four iC-MV devices are serially cascaded with their SLI and SLO ports and are each connected with the clock, SCLK. During an SSI transmission, iC-MV 1's position data is transferred to iC-MV 2 and so on up until the master. This is illustrated in Figure 9. Each iC-MV synchronizes its position data to the predecessor and sends them to the next device. The SSI master thus receives internally synchronized multiturn data. The number of data bits to be transmitted is determined by the data length DL(2:0). During synchronization the MSB of the preceding iC-MV is compared to the own synchronization bit and the position value is corrected by one, if necessary. This requires the iC-MV's offset register to be programmed correctly.

ABZ INTERFACE

In MODE = 0x07 the ABZ interface is activated. An incremental output occurs at SLI, SCLK and SLO. In ABZ mode register bit SYNC extends the zero pulse about 90 °. The resolution can be adjusted via DL(2:0).

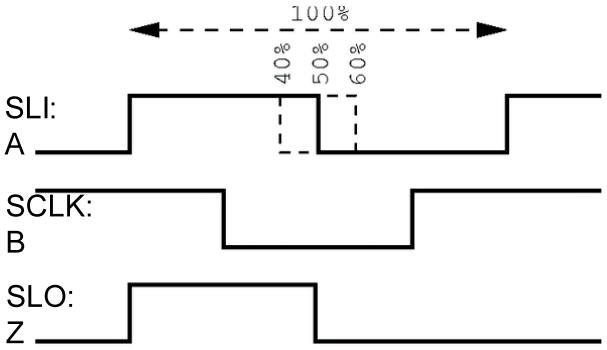


Figure 15: ABZ Signals

Note:
DL = 0x00 is not possible. The converter hysteresis is 1.4 ° and the minimum threshold distance is two oscillator clocks.

ADJUSTMENT

For the adjustment test mode is activated via MODE = 0x01. The automatic gain control's signal gain is output at pin NERR. In this test mode ENPU = 0x0 and NOSBY = 0x1 must be set. The signal level on the signal gain can be used as a measurement for the axial adjustment between iC-MV and the magnet.

Adjustment: Axial
The GAIN signal should be set between approx. 200 mV and 400 mV via axial adjustment. This corresponds to a distance of about 1 mm.

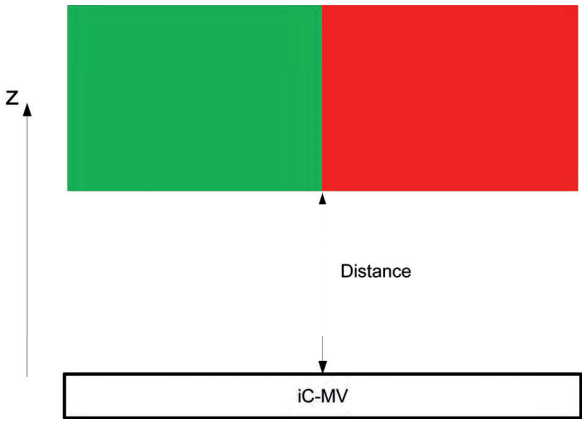


Figure 16: Axial Adjustment

Adjustment: Radial
The radial adjustment is determined by the mechanical arrangement of the system components (package, gear, axis offset and PCB).

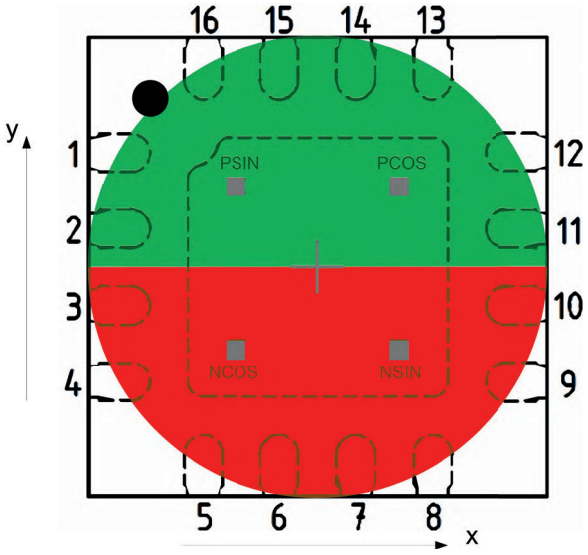


Figure 17: Radial Adjustment

SYNCHRONIZATION AND CALCULATION EXAMPLE

Calculation example for a gear reduction of 1:32

Step 1: Set configuration offset calculation
SYNC = 0x0
OFFSET = 0x00
DL = 0x07 (8-bit data length)
HIDATA = bit 7 to 3 of previous iC-MV (or initial singleturn device) position data
LODATA = bit 2 to 0 of following iC-MV position data (refer to Figure 9)

Step 2: Read position data and calculate offset

Offset calculation for ratio 1:32							
OFFSET x		HIDATA x (5 bits)		LODATA (3 bits)		90 ° reserve	calc. of next HIDATA x
OFFSET 1	=	singleturn HIDATA	-	iC-MV 1 LODATA	+	2	pos. MV 1 + OFFSET 1
OFFSET 2	=	iC-MV 1 HIDATA 1	-	iC-MV 2 LODATA	+	2	pos. MV 2 + OFFSET 2
OFFSET 3	=	iC-MV 2 HIDATA 2	-	iC-MV 3 LODATA	+	2	pos. MV 3 + OFFSET 3
OFFSET 4	=	iC-MV 3 HIDATA 3	-	iC-MV 4 LODATA	+	2	pos. MV 4 + OFFSET 4

Table 19: Offset Calculation for Ratio 1:32

Note:
The sequence described above must be followed for the calculation. The calculated offset correction is essential to allow a successful synchronization.

Step 3: Set configuration for ratio 1:32
SYNC = 0x1
OFFSET = Calculation with offset positions from Table 6
DL = 0x04 (5-bit data length)

Note:
When the the singleturn system calculate the sychronisation of the multiturn values the parameter SYNC of MV1 has to be 0x0

Calculation example for a gear reduction of 1:16

Step 1: Set configuration offset calculation
SYNC = 0x0
OFFSET = 0x00
DL = 0x07 (8-bit data length)
HIDATA = bit 7 to 4 of previous iC-MV (or initial singleturn device) position data
LODATA = bit 3 to 0 of following iC-MV position data (refer to Figure 9)

Step 2: Read position data and calculate offset

Offset calculation for ratio 1:16							
OFFSET x		HIDATA x (4 bits)		LODATA (4 bits)		90 ° reserve	calc. of next HIDATA x
OFFSET 1	=	singleturn HIDATA	-	iC-MV 1 LODATA	+	4	pos. MV 1 + OFFSET 1
OFFSET 2	=	iC-MV 1 HIDATA 1	-	iC-MV 2 LODATA	+	4	pos. MV 2 + OFFSET 2
OFFSET 3	=	iC-MV 2 HIDATA 2	-	iC-MV 3 LODATA	+	4	pos. MV 3 + OFFSET 3
OFFSET 4	=	iC-MV 3 HIDATA 3	-	iC-MV 4 LODATA	+	4	pos. MV 4 + OFFSET 4

Table 20: Offset Calculation for Ratio 1:16

Note:
The sequence described above must be followed for the calculation. The calculated offset correction is essential to allow a successful synchronization.

Step 3: Set configuration for ratio 1:16
SYNC = 0x1
OFFSET = Calculation with offset positions from Table 6
DL = 0x03 (4-bit data length)

Note:
When the the singleturn system calculate the sychronisation of the multiturn values the parameter SYNC of MV1 has to be 0x0

Synchronization Monitoring
If the bit ERRSY is activated, the synchronized position data is checked for consistency. The error is displayed via the error bit in the SSI protocol, if configured. Synchronization monitoring only works with DL = 0x03.

Calculation example for a gear reduction of 1:8

Step 1: Set configuration offset calculation
SYNC = 0x0
OFFSET = 0x00
DL = 0x07 (8-bit data length)
HIDATA = bit 7 to 5 of previous iC-MV (or initial singleturn device) position data
LODATA = bit 4 to 0 of following iC-MV position data (refer to Figure 9)

Step 2: Read position data and calculate offset

Offset calculation for ratio 1:8							
OFFSET x		HIDATA x (3 bits)		LODATA (5 bits)		90 ° reserve	calc. of next HIDATA x
OFFSET 1	=	singleturn HIDATA	-	iC-MV 1 LODATA	+	8	pos. MV 1 + OFFSET 1
OFFSET 2	=	iC-MV 1 HIDATA 1	-	iC-MV 2 LODATA	+	8	pos. MV 2 + OFFSET 2
OFFSET 3	=	iC-MV 2 HIDATA 2	-	iC-MV 3 LODATA	+	8	pos. MV 3 + OFFSET 3
OFFSET 4	=	iC-MV 3 HIDATA 3	-	iC-MV 4 LODATA	+	8	pos. MV 4 + OFFSET 4

Table 21: Offset Calculation for Ratio 1:8

Note:
The sequence described above must be followed for the calculation. The calculated offset correction is essential to allow a successful synchronization.

Step 3: Set configuration for ratio 1:8
SYNC = 0x1
OFFSET = Calculation with offset positions from Table 6
DL = 0x02 (3-bit data length)

Note:
When the the singleturn system calculate the sychronisation of the multiturn values the parameter SYNC of MV1 has to be 0x0

Calculation example for a gear reduction of 1:4

Step 1: Set configuration offset calculation
SYNC = 0x0
OFFSET = 0x00
DL = 0x07 (8-bit data length)
HIDATA = bit 7 to 6 of previous iC-MV (or initial singleturn device) position data
LODATA = bit 5 to 0 of following iC-MV position data (refer to Figure 9)

Step 2: Read position data and calculate offset

Offset calculation for ratio 1:4							
OFFSET x		HIDATA x (2 bits)		LODATA (6 bits)		90 ° reserve	calc. of next HIDATA x
OFFSET 1	=	singleturn HIDATA	-	iC-MV 1 LODATA	+	16	pos. MV 1 + OFFSET 1
OFFSET 2	=	iC-MV 1 HIDATA 1	-	iC-MV 2 LODATA	+	16	pos. MV 2 + OFFSET 2
OFFSET 3	=	iC-MV 2 HIDATA 2	-	iC-MV 3 LODATA	+	16	pos. MV 3 + OFFSET 3
OFFSET 4	=	iC-MV 3 HIDATA 3	-	iC-MV 4 LODATA	+	16	pos. MV 4 + OFFSET 4

Table 22: Offset Calculation for Ratio 1:4

Note:
The sequence described above must be followed for the calculation. The calculated offset correction is essential to allow a successful synchronization.

Step 3: Set configuration for ratio 1:4
SYNC = 0x1
OFFSET = Calculation with offset positions from Table 6
DL = 0x01 (2-bit data length)

Note:
When the the singleturn system calculate the sychronisation of the multiturn values the parameter SYNC of MV1 has to be 0x0

ERROR HANDLING

CRC Error

If the EEPROM is not read out at all or not entirely or if a CRC error is detected, the SSI interface provides a steady high level at request.

Error Bit Options

If an amplitude error is recognized e.g. through the loss of the magnet, this is displayed through a low level and sent to the SSI protocol, if activated. The error bit is configured via register bits EMODE(2:0), where *n* is the number of the iC-MV slaves.

EMODE	Addr. 0x01; bit 5:3
Code	Function
0x00	No error bit
0x01	1 serial error bit lo active
0x03	1 serial error bit hi active
0x05	n serial error bits lo active
0x07	n serial error bits hi active

Table 23: Error Bit Options

The error bit is added to the position data. Thereby iC-MV 1 in the SSI chain sends its error bit first. In case additional iC-MVs exist, iC-MV 2 then sends its error bit to the neighboring component.

APPLICATION EXAMPLES

iC-MHM with 4 iC-MVs

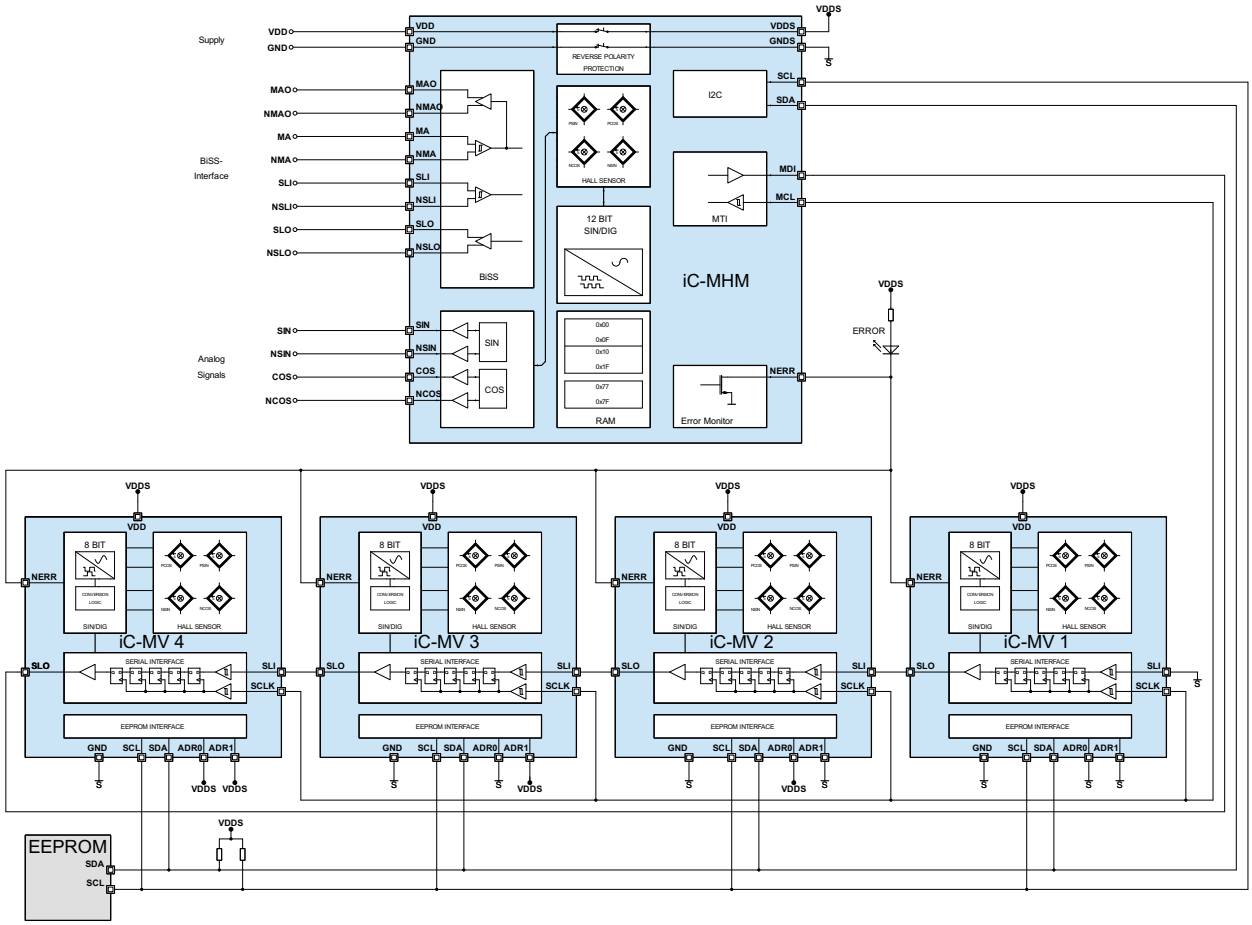


Figure 18: iC-MHM with 4 iC-MVs

Note: Circuit examples are provided for illustration of principle. Additional components required for a successful application may be omitted for clarity.

iC-MN with 3 iC-MVs

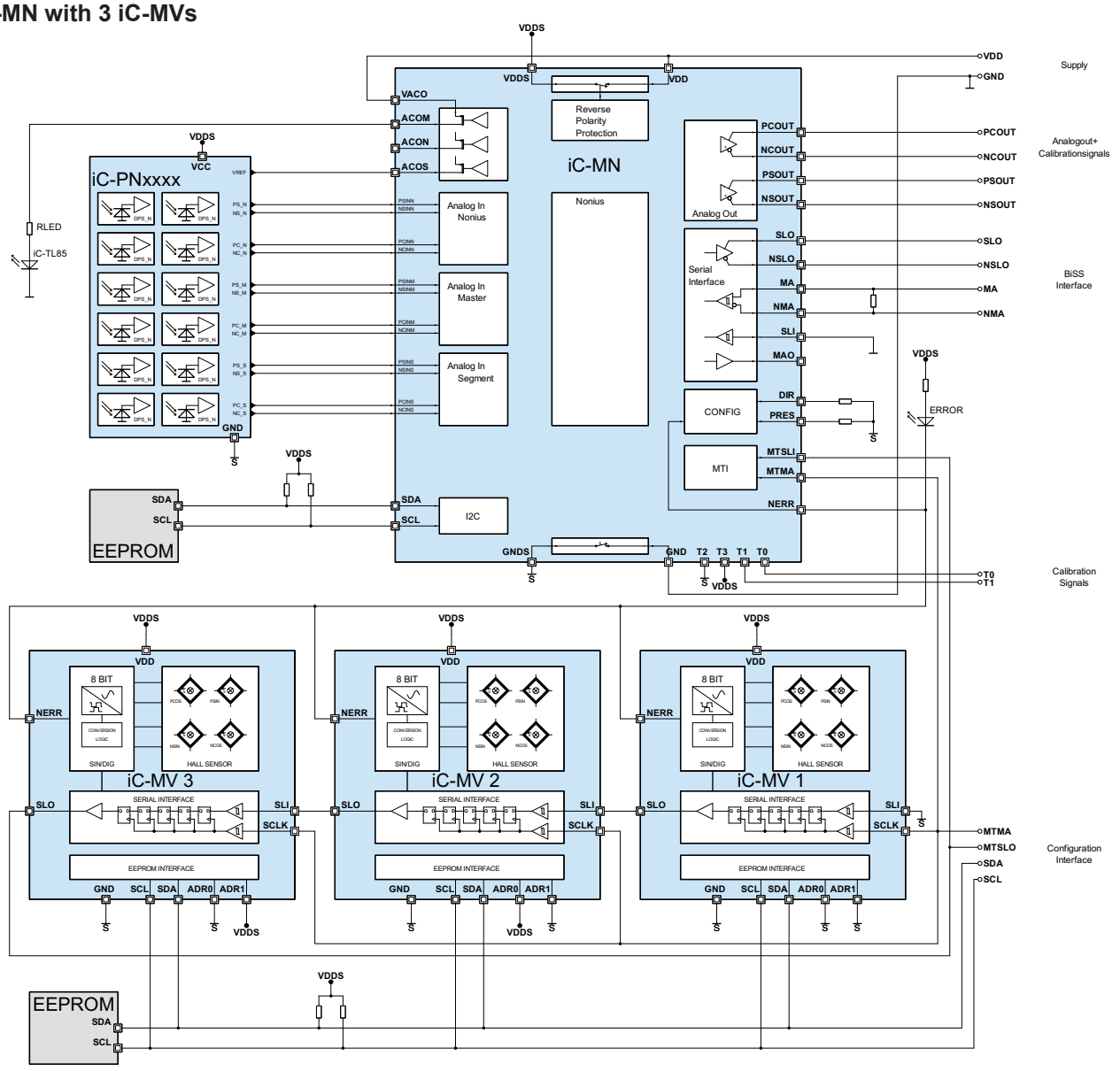


Figure 19: iC-MN with 3 iC-MVs

iC-MU with 3 iC-MVs

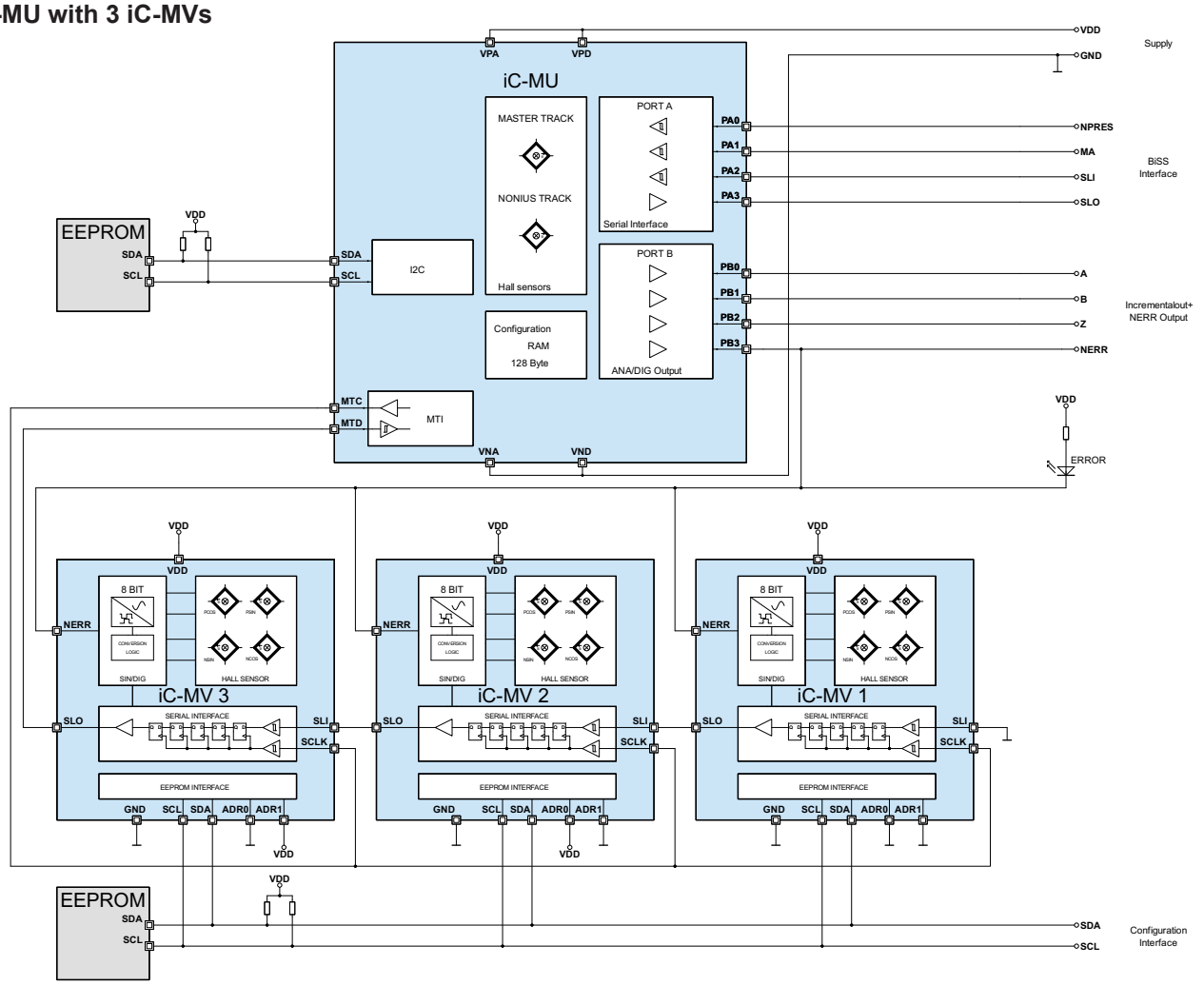


Figure 20: iC-MU with 3 iC-MVs

iC-LGC with 3 iC-MVs

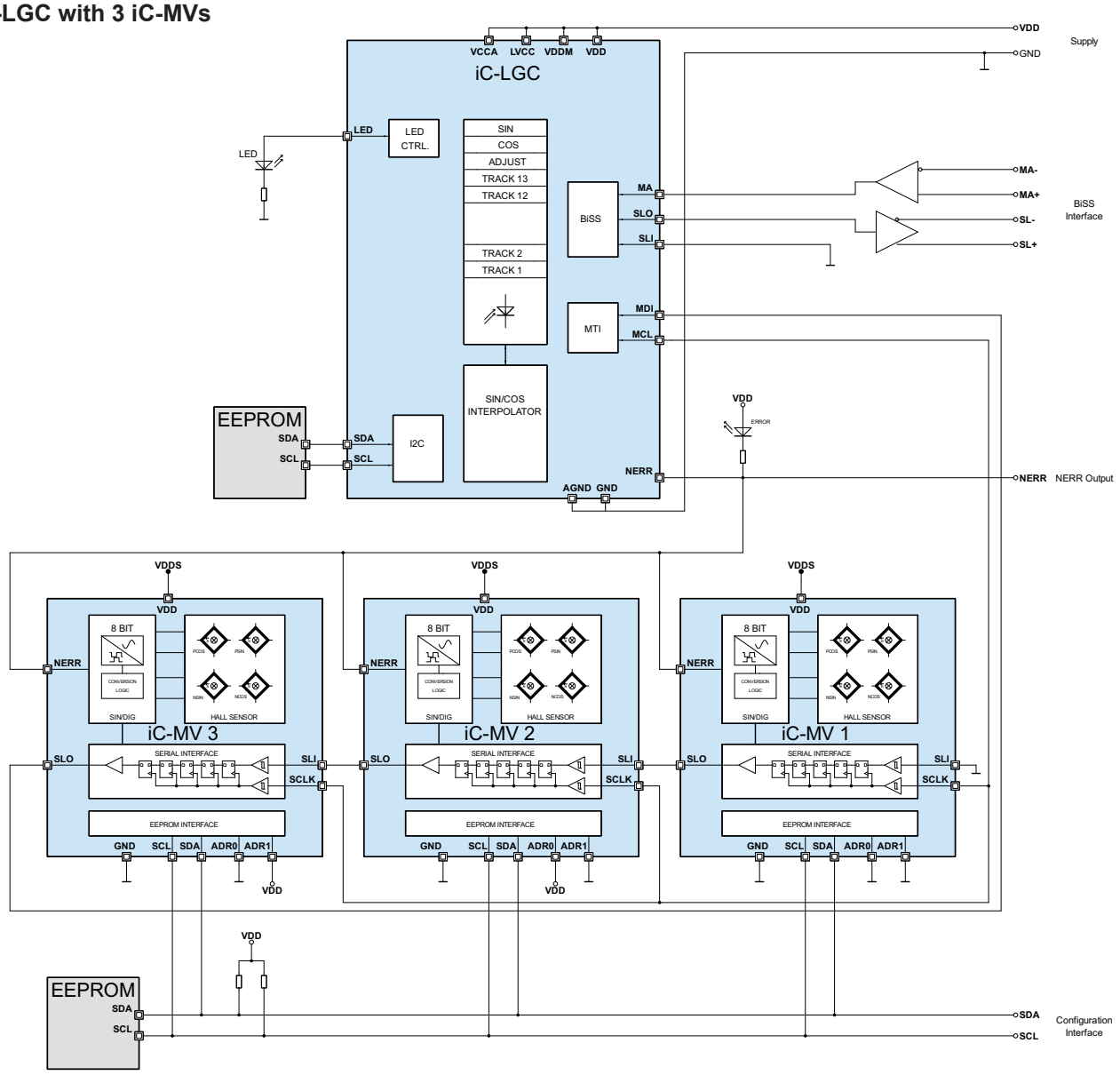


Figure 21: iC-LGC with 3 iC-MVs

MV1A with 4 iC-MVs

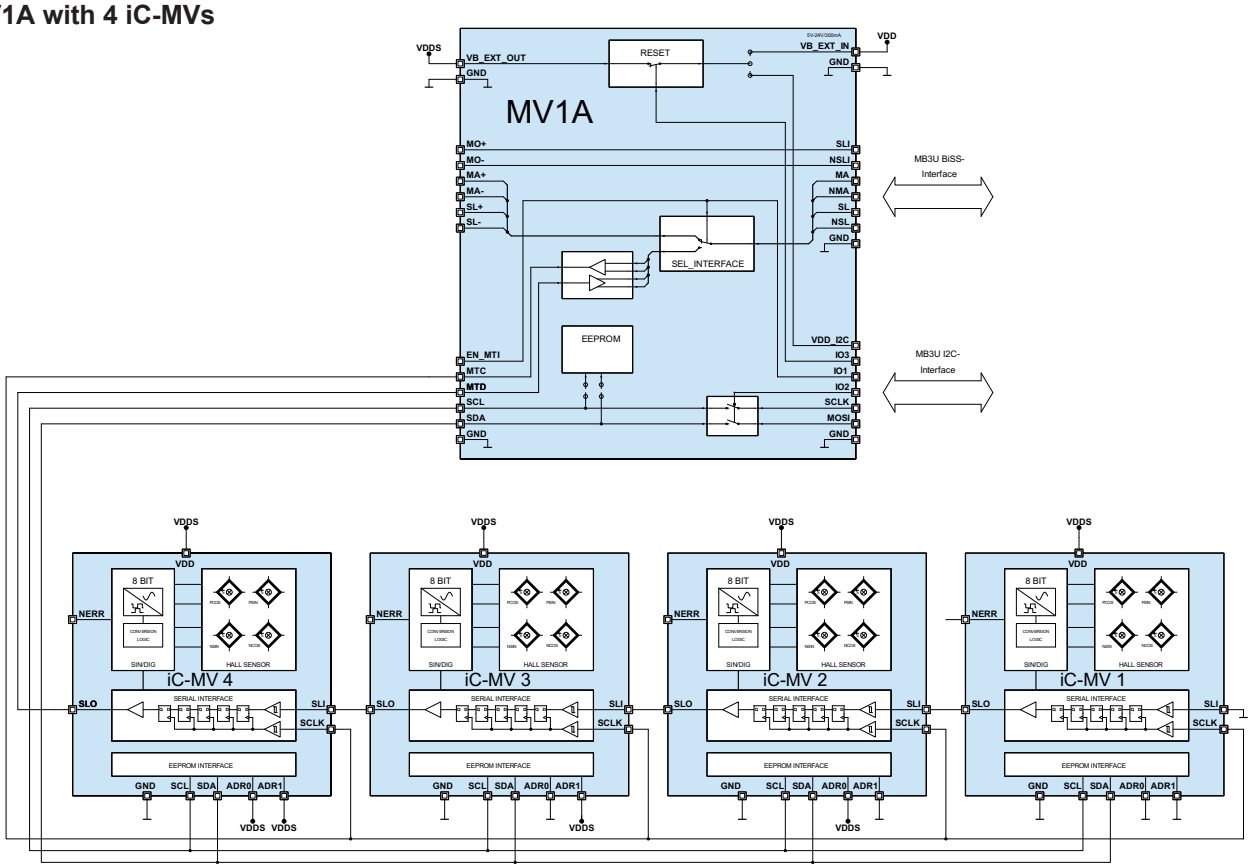


Figure 22: MV1A with 4 iC-MVs

DESIGN REVIEW: Notes On Chip Functions

iC-MV Y1		
No.	Function, Parameter/Code	Description and Application Hints
1	GAIN	GAIN signal doubled in adjustment mode.
2	ENPU	Current consumption reduced in standby mode with ENPU = 0x0.

Table 24: Notes on chip functions regarding iC-MV chip release Y1

iC-MV X2, X3		
No.	Function, Parameter/Code	Description and Application Hints
1		No further notes at time of printing.

Table 25: Notes on chip functions regarding iC-MV chip releases X2, X3

REVISION HISTORY

Rel.	Rel. Date*	Chapter	Modification	Page
A1	14-08-05	All	Initial release	All

Rel.	Rel. Date*	Chapter	Modification	Page
A2	15-03-02		Title revised	

Rel.	Rel. Date*	Chapter	Modification	Page
B1	2017-08-23	ELECTRICAL CHARACTERISTICS	Item 004: typ. value changed Item 202: min. value changed Item 802: min. and max. value changed Item 803: condition extended Item 804: supplemented Item 903: max. value changed Item B06: supplemented Item B12: max. value changed	7 f
		REGISTERS	Description of parameters NOSBY and LOPM extended and Table 12, Table 14 changed	15
		ADJUSTMENT	GAIN signal changed from 100-200 mV to 200-400 mV	19
		SYNCHRONIZATION	Table 19 extended, note added	20
		DESIGN REVIEW	Chapter added	29

Rel.	Rel. Date*	Chapter	Modification	Page
C1	2021-01-07	DESCRIPTION	Note box added	2
		ABSOLUTE MAXIMUM RATINGS	Item No. G002: pin NERR included old Item No. G003: parameter removed Item No. G005: parameter extended with pin ADR1, ADR0, SCLK and SLI	6
		THERMAL DATA	Item No. T01: condition added Item No. T02: typ. value and condition changed	6
		ELECTRICAL CHARACTERISTICS	Item No. 201: typ. and max. value changed Item No. 202: max. value changed Item No. B10: max. value changed and conditions extended old Item No. B11, H07, H08, H09: parameter removed	7, f
		OPERATING REQUIREMENTS	Timing diagram changed	9
		HALL SENSORS	Figure 5 and Figure 6 extended	11, 12
		REGISTERS	Description of parameter DIR in Table 7 changed, note in Table 10 added, Figure 13 extended	14 15
		ABZ INTERFACE	Note for parameter DL added	19
		SCAN TEST	Chapter removed	
		DESIGN REVIEW: Notes On Chip Functions	Release X3 added	29

Rel.	Rel. Date*	Chapter	Modification	Page
C2	2021-06-16		Preliminary removed	
		SYNCHRONIZATION AND CALCULATION EXAMPLE	Examples for gear ratio 1:32, 1:8 and 1:4 added	20, 22, 23

* Release Date format: *YYYY-MM-DD*

ORDERING INFORMATION

Type	Package	Order Designation
iC-MV	QFN16, 3 mm x 3 mm x 0.9 mm RoHS compliant	iC-MV QFN16-3x3

Please send your purchase orders to our order handling team:

Fax: +49 (0) 61 35 - 92 92 - 692
E-Mail: dispo@ichaus.com

For technical support, information about prices and terms of delivery please contact:

iC-Haus GmbH
Am Kuemmerling 18
D-55294 Bodenheim
GERMANY

Tel.: +49 (0) 61 35 - 92 92 - 0
Fax: +49 (0) 61 35 - 92 92 - 192
Web: http://www.ichaus.com
E-Mail: sales@ichaus.com

Appointed local distributors: http://www.ichaus.com/sales_partners