iC-MHM
14-BIT ABSOLUTE ANGLE HALL ENCODER

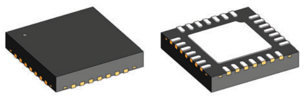
FEATURES

- Quad Hall sensor array for easy assembly
- Monitored auto-gain control, optional fine-calibration for compensation of misalignment
- Absolute resolution of 0.02 ° (14 bit / 360 ° at up to 10 000 rpm)
- Selectable resolution and tracking rate (12 bit at 80 000 rpm)
- Adjustable zero position and code direction
- Differential current-limited sin/cos outputs (1 Vpp into 100 Ω)
- BiSS Interface for CRC-secured communication
- Compatible with BiSS C profiles (BP1, BP3) and SSI
- Integrated RS422 transceiver for up to 10 Mbit/s (at 5 V)
- Higher data rates supported by LVDS compatibility
- System monitoring via BiSS error/warning bits (loss-of-magnet)
- Multiturn input via dedicated SSI MT interface (up to 32 bits)
- Command/pin-triggered position preset for ST/MT data
- 3 General-Purpose I/Os; open-drain error output
- SPI operation optional
- CRC-protected EEPROM setup (multi-master I^{2}C interface)
- Extended temperature range from -40 to +125 °C
- Reverse-polarity and short-circuit-proof interface pins

APPLICATIONS

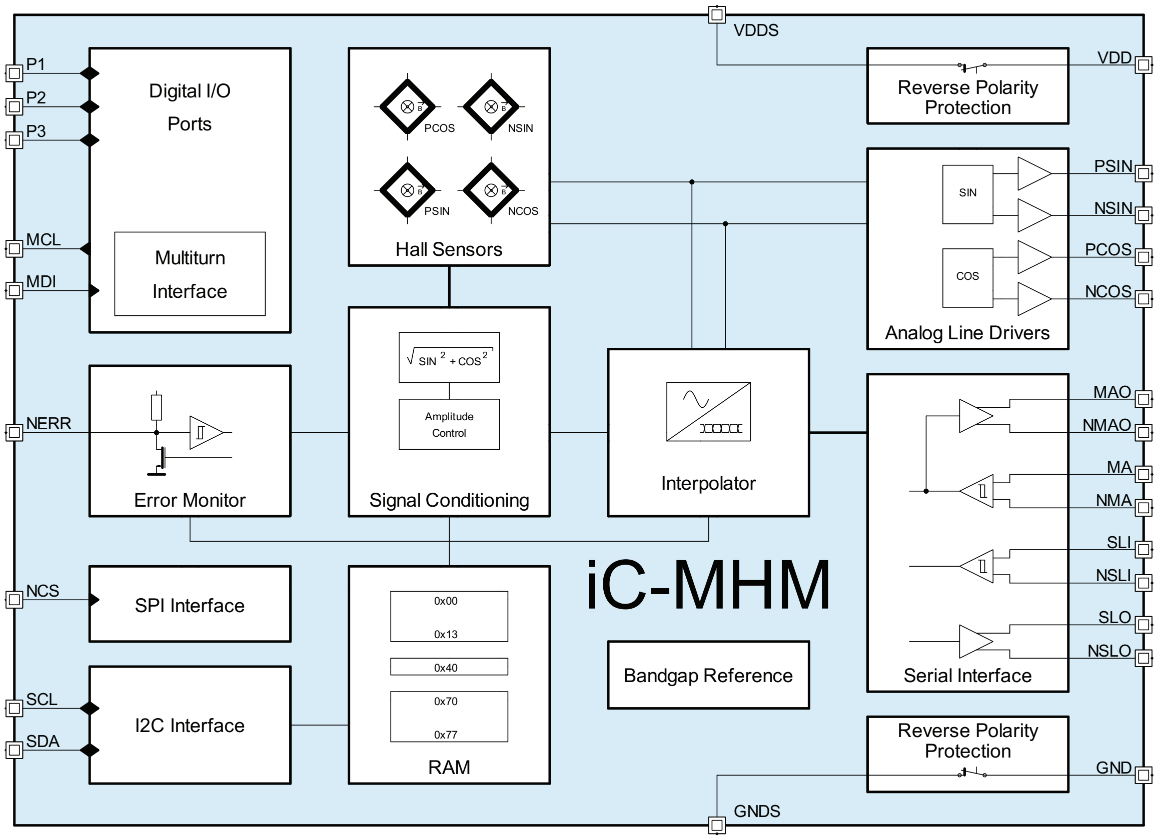
- Absolute angle sensors
- Singleturn/multiturn position encoders
- Motor feedback

PACKAGES



28-pin QFN
5 mm x 5 mm x 0.9 mm
RoHS compliant

BLOCK DIAGRAM



DESCRIPTION

The iC-MHM is an absolute angular position sensor (encoder) using four integrated Hall sensors for sensing a diametrical magnetized permanent magnet. Output is absolute position in BiSS, SSI, or SPI format and/or incremental position via encoder quadrature (ABZ) signals.

The Hall sensors provide differential signals proportional to the sine and cosine of the magnet's angular position. These signals can be calibrated to eliminate voltage offsets, amplitude differences and harmonic distortion. An automatic amplitude control maintains 1 Vpp signal amplitudes regardless of changes in airgap or temperature.

An integrated interpolator uses the calibrated sine and cosine signals to determine the angular position of the permanent magnet with a resolution of 4 096 increments per revolution. Turns count information from an external multiturn sensor can also be read in and synchronized with the interpolated angle using the integrated multiturn SSI interface.

Integrated line drivers and receivers are provided for for BiSS C or SSI stand-alone encoder applications. SSI ring-mode operation is also supported. TTL or LVDS level SPI communication with a host processor or microcontroller can be selected for embedded applications.

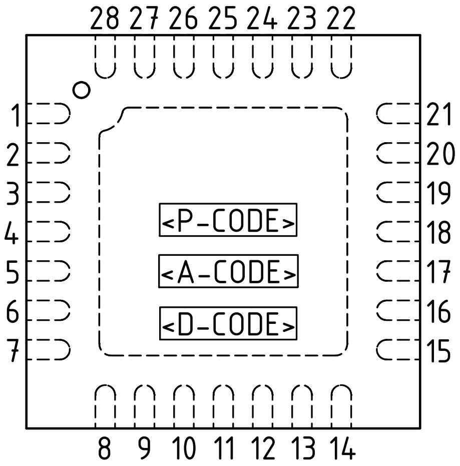
The iC-MHM is configured using the integrated serial port in BiSS C or SPI mode. In stand-alone applications, configuration parameters are stored in an external EEPROM and protected by a CRC for use at startup. The integrated I^2C multi-master interface allows the same EEPROM to be used by external multiturn sensors such as the iC-MV and iC-PV for configuration storage.

A 4-bit digital I/O port provides general-purpose or dedicated discrete I/O for application versatility.

CONTENTS

PACKAGING INFORMATION

PIN CONFIGURATION QFN28-5x5



PIN FUNCTIONS

No.	Name	Function
1	MA[4]	BiSS/SSI Clock Input, SPI Clock Input (SCLK)
2	NMA[4]	BiSS/SSI Clock Input, inverted
3	NSIN	Analog Sine Output, inverted
4	PSIN	Analog Sine Output
5	P1	Digital I/O 1, Preset Input
6	P2	Digital I/O 2, Code Direction Input
7	P3	Digital I/O 3, BiSS Output
8	n.c.[1]	
9	NCS	SPI Enable and Chip Select Input (active low)
10	MCL	Multiturn SSI Clock Output, Digital Output 0
11	MDI	Multiturn SSI Data Input, Digital Input 0
12	NERR	Error Input/Output (active low)
13	SCL	I^2C Clock
14	SDA	I^2C Data
15	n.c.	
16	GNDS[5]	Switched GND (reverse polarity protected)
17	VDDS[5]	Switched VDD (reverse polarity protected)
18	PCOS	Analog Cosine Output
19	NCOS	Analog Cosine Output, inverted
20	NSLI[2, 4]	BiSS Data Input, inverted
21	SLI[2, 4]	BiSS Data Input SPI Data Input (MOSI)
22	NSLO[4]	BiSS/SSI Data Output, inverted
23	SLO[4]	BiSS/SSI Data Output SPI Data Output (MISO)
24	VDD[4]	+5 V Supply Voltage Input
25	n.c.	
26	GND[4]	Ground
27	NMAO[4]	BiSS Clock Output, inverted
28	MAO[4]	BiSS Clock Output
	BP[3]	Backside Paddle

IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes), <D-CODE> = date code (subject to changes);

[1] Pins marked n.c. are not connected.

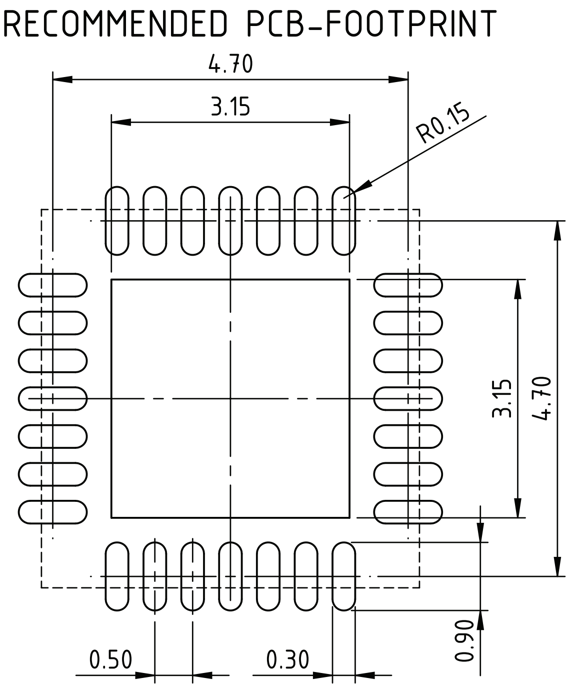
[2] Must be externally biased as shown in Figures 19 and 20.

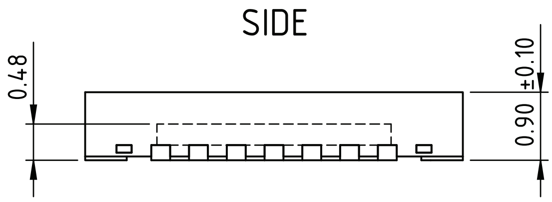
[3] Connection of the backside paddle to GNDS by a single trace is recommended. Current flow across the paddle is not permissible.

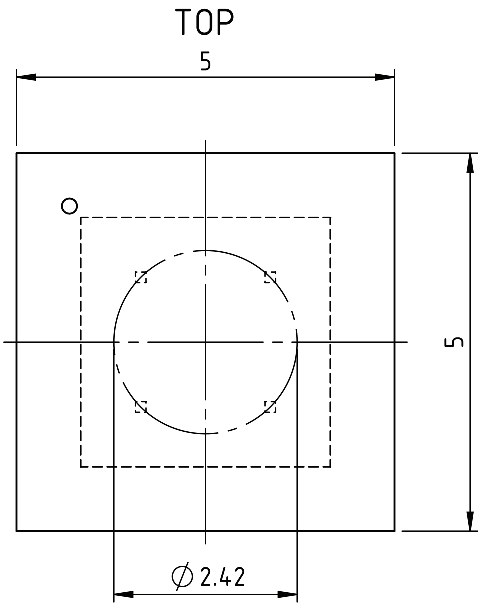
[4] Protect against transient voltages as shown in Figure 8.

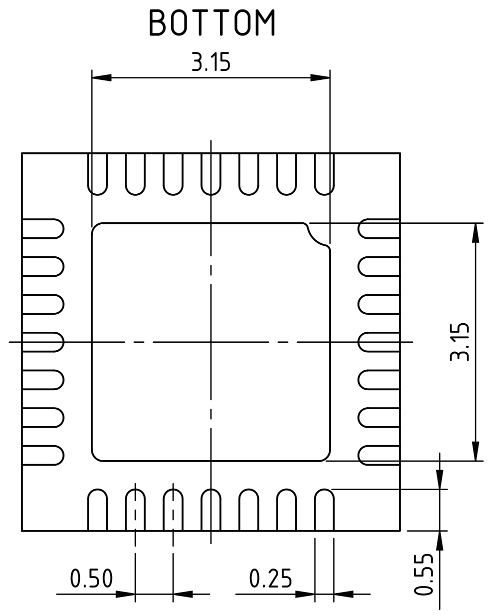
[5] A bypass capacitor of at least 100 nF between and close to these pins is recommended.

PACKAGE DIMENSIONS









All dimensions given in mm.
Tolerances of form and position according to JEDEC MO-220.
Tolerance of sensor pattern: ±0.10mm / ±1° (with respect to center of backside pad).

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ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these ratings device damage may occur.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	V()	Voltage at VDD, GND, PSIN, NSIN, PCOS, NCOS, MAO, NMAO, MA, NMA, SLI, NSLI, SLO, NSLO		-6	6	V
G002	V()	Pin-to-Pin Voltage between VDD, GND, PSIN, NSIN, PCOS, NCOS, MAO, NMAO, MA, NMA, SLI, NSLI, SLO, NSLO			6	V
G003	V()	Voltage at VDDS	no reversed polarity at VDD and GND		VDD	V
G004	V()	Voltage at GNDS referenced to GND	no reversed polarity at VDD and GND	-0.3	0.3	V
G005	V()	Voltage at P1, P2, P3, MCL, MDI, NERR, NCS, SCL, SDA		-0.3	VDDS + 0.3	V
G006	I()	Current in VDD, GND		-50	50	mA
G007	I()	Current in VDDS, GNDS		-25	25	mA
G008	I()	Current in PSIN, NSIN, PCOS, NCOS, MAO, NMAO, MA, NMA, SLI, NSLI, SLO, NSLO, P1, P2, P3, MCL, MDI, NERR, NCS, SCL, SDA		-20	20	mA
G009	Vd()	ESD Susceptibility at all pins	HBM, 100 pF discharged through 1.5 kΩ		2	kV
G010	Ptot	Permissible Power Dissipation			300	mW
G011	Ts	Storage Temperature		-40	150	°C
G012	Tj	Junction Temperature		-40	150	°C

THERMAL DATA

Operating conditions: VDD = 5 V ±10 %

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range		-40		125	°C
T02	Rthja	Thermal Resistance Chip to Ambient	QFN28-5x5 surface mounted to PCB according to JEDEC 51		40		K/W

All voltages are referenced to pin GNDS unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = 5 V ±10 %, Tj = -40...125 °C, CIBM adjusted to 200 µA, 4 mm NdFeB magnet, unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
General							
001	VDD	Permissible Supply Voltage VDD versus GND	load current I(VDDS) < -10 mA	4.5		5.5	V
002	I(VDD)	Supply Current in VDD	without load		25	32	mA
003	I(VDDS)	Permissible Load Current in VDDS	VDD = 5 V ±5 %	-25		0	mA
005	Vc()hi	Clamp-Voltage hi at P1, P2, P3, MCL, MDI, NERR, NCS, SCL, SDA	Vc()hi = V() − VDDS, I() = 1 mA	0.4		1.5	V
006	Vc()lo	Clamp-Voltage lo at all pins	I() = -1 mA	-1.5		-0.3	V
Hall Sensors							
101	Hext	Permissible Magnetic Field Strength	at chip surface	20		100	kA/m
102	fmag	Operating Magnetic Field Frequency	AVGFILT = 0, RESO_ST $\geq$ 4, TLF = 1			1.4	kHz
103	rpm	Rotating Speed of Magnet	refer to Elec. Char. 102			84000	rpm
104	dsens	Diameter of Hall Sensor Circle			2.42		mm
105	xdis	Permissible Lateral Displacement of Magnet Axis to Center of Hall Sensors				0.2	mm
106	xpac	Displacement Chip Center to Package Center	package QFN28-5x5	-0.2		0.2	mm
107	ϕpac	Angular Alignment of Chip vs. Backside Paddle	package QFN28-5x5	-1		+1	Deg
108	hpac	Distance of Chip Surface to Package Surface	package QFN28-5x5		0.4		mm
Signal Conditioning							
201	Vos	Maximum Positive Offset Correction Range	VOSS or VOSC = 0x7F	-37.5	-31.5	-27.5	mV
202	Vos	Maximum Negative Offset Correction Range	VOSS or VOSC = 0x3F	27.5	31.5	37.5	mV
203	Vopt	Optimal Differential Output Voltage	Vopt = Vpp(PSIN) − Vpp(NSIN), ENAC = 0, refer to Figure 13		1		Vpp
Amplitude Control							
301	Vdiff()pk	Differential Output Amplitude	Vampl = Vpp(PSIN) − Vpp(NSIN), ENAC = 1, refer to Figure 13	0.8		1.2	Vpp
302	Vratio	Amplitude Ratio	Vratio = Vpp(PSIN) / Vpp(PCOS)	0.92		1.09	
303	S()ctrl	Settling Time of Amplitude Control	to ±10 % of final setpoint			300	µs
304	Vpp()min	Amplitude Error Threshold for ERR_AMIN	$(V(PSIN-NSIN))^2 + (V(PCOS-NCOS))^2 < Vpp()min$	0.3		0.7	Vpp
305	Vpp()max	Amplitude Error Threshold for ERR_AMAX	$(V(PSIN-NSIN))^2 + (V(PCOS-NCOS))^2 > Vpp()max$	1.20		1.5	Vpp
Bandgap Reference							
401	Vbg	Bandgap Reference Voltage	at pin PCOS, mode TEST = 0x19	1.17	1.24	1.32	V
402	Vref	Reference Voltage	at pin PSIN, mode TEST = 0x19	45	50	55	%VDDS
403	Ibias	Bias Current	at pin NSIN, mode TEST = 0x19; CIBM = 0x8 CIBM = 0x7 bias current adjusted	 -370 -220	 -200	 -100 -180	 µA µA µA
404	VDDon	Turn-on Threshold VDD (Power-Up-Enable)	increasing voltage	3.65	4.0	4.3	V
405	VDDoff	Turn-off Threshold VDD (Power-Down-Reset)	decreasing voltage	3	3.5	3.8	V
406	VDDhys	Turn-on Threshold Hysteresis		0.3			V

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = 5 V ±10 %, Tj = -40...125 °C, CIBM adjusted to 200 µA, 4 mm NdFeB magnet, unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
407	Vosr	Reference Voltage Offset Compensation	at pin NCOS in test mode TEST = 0x19	470	500	530	mV
Clock Generation							
501	fsys	System Clock	bias current adjusted; measured at pin SCL with division factor 256	11.5	14	16	MHz
Interpolator							
601	RESsdc	Resolution			12		bit
602	AAabs	Absolute Angular Accuracy	calibrated signal conditioning	-0.35		0.35	Deg
603	AArel	Relative Angular Accuracy	with reference to one output period at P1(A), P2(B), with RESO_ST = 0x06, TLF > 0x00, refer to Figure 1	-15		15	%
Digital I/O, MT Interface, Error Monitor, SPI Interface, I^2C Interface: P1, P2, P3, MCL, MDI, NERR, NCS, SCL, SDA							
701	Vs()hi	Saturation Voltage hi at P1, P2, P3, MCL	Vs()hi = V(VDDS) – V(), I() = -1.6 mA			0.4	V
702	Vs()lo	Saturation Voltage lo at P1, P2, P3, MCL, SCL, SDA, NERR	versus GNDS, I() = 1.6 mA			0.4	V
703	Isc()hi	Short-Circuit Current hi at P1, P2, P3, MCL	V() = GND, Tj = 25 °C	-90	-50		mA
704	Isc()lo	Short-Circuit Current lo at P1, P2, P3, MCL, SCL, SDA, NERR	V() = VDD, Tj = 25 °C		50	80	mA
705	tr()	Rise Time at P1, P2, P3, MCL	CL = 50 pF, rise 10 % to 90 %			60	ns
706	tf()	Fall Time at P1, P2, P3, MCL, SCL, SDA, NERR	CL = 50 pF, fall 90 % to 10 %			60	ns
707	Vt()hi	Threshold Voltage hi at P1, P2, P3, MDI, NERR, NCS, SCL, SDA				2	V
708	Vt()lo	Threshold Voltage lo at P1, P2, P3, MDI, NERR, NCS, SCL, SDA		0.8			V
709	Vt()hys	Threshold Hysteresis at P1, P2, P3, MDI, NERR, NCS, SCL, SDA		150	250		mV
710	Ipd()	Pull-down Current at P1, P2, P3	V() = 1 V...VDDS	6	30	60	µA
711	Ipu()	Pull-up Current at MDI, NCS	V() = 0 V...VDDS – 1 V	-60	-30	-6	µA
712	Ipu()	Pull-up Current at SCL, SDA, NERR	V() = 0 V...VDDS – 1 V	-800	-300	-60	µA
713	fc()	Clock Frequency at MCL	refer to Elec. Char. 501; CF_MTI = 0x0 refer to Elec. Char. 501; CF_MTI = 0x1		1/8 1/64		fsys fsys
714	fc()	Clock Frequency at SCL	refer to Elec. Char. 501		1/256		fsys
715	tbusy()cfg	Duration of Config Phase	bias current not adjusted; without EEPROM EEPROM access without I^2C read error EEPROM access with I^2C read error			14 24 45	ms ms ms
Analog Line Drivers: PSIN, NSIN, PCOS, NCOS							
801	Isc()hi	Short-Circuit Current hi	short-circuit versus VDD	10	30	50	mA
802	Isc()lo	Short-Circuit Current lo	short-circuit versus GND	-50	-30	-10	mA
803	Ilk()	Leakage Current	versus supply voltage	-1		1	µA
Serial Interface: General							
901	Rpu()	Pull-up Resistor at MA	RTX_MODE = 0 or 1		50		kΩ
902	Rpd()	Pull-down Resistor at SLI	RTX_MODE = 0 or 1		50		kΩ
903	T_{CLK}	Period of Adaptive Timeout Sampling Clock (for EDS)	refer to Characteristics in BiSS Interface PROTOCOL DESCRIPTION		1.33 / fsys		
904	$t_{out}()$	Adaptive Slave Timeout at SLO	NTOA = 0 refer to timing Figure 2 t_{init} measured as first 1.5 · T(MA) each frame.	2 / fsys	t_{init} + 4 / fsys	280 / fsys	

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = 5 V ±10 %, Tj = -40...125 °C, CIBM adjusted to 200 µA, 4 mm NdFeB magnet, unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
905	t_{out}()	Fixed Slave Timeout at SLO	NTOA = 1 refer to timing Figure 5		280 / fsys		
Serial Interface: Outputs MAO, SLO in TTL Mode (RTX_MODE = 1)							
906	Vs()hi	Saturation Voltage hi	Vs()hi = V(VDD) – V(), I() = 4 mA			0.4	V
907	Vs()lo	Saturation Voltage lo	Vs()lo = V(GND) – V(), I() = 4 mA			0.4	V
908	Isc()hi	Short-Circuit Current hi	versus GND	-90	-50		mA
909	Isc()lo	Short-Circuit Current lo	versus VDD		50	120	mA
910	t_{P3}()	Output Propagation Delay at SLO	refer to timing Figure 4			30	ns
911	tr()	Rise Time	CL = 30 pF, rise 10 % to 90 %		4		ns
912	tf()	Fall Time	CL = 30 pF, fall 90 % to 10 %		2.8		ns
913	Rpd()	Pull-down Resistor at NMAO, NSLO		1	2	3	kΩ
Serial Interface: Inputs MA, SLI in TTL Mode (RTX_MODE = 0 or 1)							
914	Vt()hi	Threshold Voltage hi	versus GND			2	V
915	Vt()lo	Threshold Voltage lo	versus GND	0.8			V
916	Vt()hys	Hysteresis		150	300		mV
Serial Interface: Outputs MAO, NMAO, SLO, NSLO in LVDS Mode (RTX_MODE = 2)							
917	V()hi	Output Voltage hi	RL = 100 Ω	1.25		1.6	V
918	V()lo	Output Voltage lo	RL = 100 Ω	0.9		1.25	V
919	Va()diff	Differential Output Voltage	Va(MAO)diff = V(MAO) – V(NMAO), Va(SLO)diff = V(SLO) – V(NSLO), RL = 100 Ω	250	350	450	mV
920	Vacm()	Common Mode Output Voltage	RL = 100 Ω	1.125	1.2	1.375	V
921	t_{P3}()	Output Propagation Delay at SLO	refer to timing Figure 4			30	ns
922	tr()	Rise Time	CL = 5 pF, rise 10 % to 90 %		2		ns
923	tf()	Fall Time	CL = 5 pF, fall 90 % to 10 %		2		ns
Serial Interface: Inputs MA, NMA, SLI, NSLI in LVDS Mode (RTX_MODE = 2)							
924	Vcm()	Input Voltage Range	versus GND	0.8		3.0	V
925	Vt()diff	Differential Input Threshold	Vt(MA)diff = V(MA) – V(NMA), Vt(SLI)diff = V(SLI) – V(NSLI)	-200		200	mV
926	Vt()hys	Differential Input Threshold Hysteresis	Vt(MA)hys = V(MA) – V(NMA), Vt(SLI)hys = V(SLI) – V(NSLI)	25	70		mV
Serial Interface: Outputs MAO, NMAO, SLO, NSLO in RS422 Mode (RTX_MODE = 0 or 3)							
927	Vs()hi	Saturation Voltage hi	Vs()hi = VDD – V(), I() = -50 mA			800	mV
928	Vs()lo	Saturation Voltage lo	Vs()lo = GND – V(), I() = 50 mA			800	mV
929	Isc()hi	Short-Circuit Current hi	V() = GND	-120		-50	mA
930	Isc()lo	Short-Circuit Current lo	V() = VDD	50		120	mA
931	t_{P3}()	Output Propagation Delay at SLO	refer to timing Figure 4			70	ns
932	tr()	Rise-Time lo to hi	Cl = 30 pF, RL = 100 Ω , rise 10 % to 90 %		10		ns
933	tf()	Fall-Time hi to lo	Cl = 30 pF, RL = 100 Ω , fall 90 % to 10 %		10		ns
Serial Interface: Inputs MA, NMA, SLI, NSLI in RS422 Mode (RTX_MODE = 3)							
934	Vcm()	Input Voltage Range	referenced to GND	0		3	V
935	Vt()diff	Differential Input Threshold	Vt(MA)diff = V(MA) – V(NMA), Vt(SLI)diff = V(SLI) – V(NSLI)	-300		300	mV
936	Vt()hys	Differential Input Threshold	Vt(MA)hys = V(MA) – V(NMA), Vt(SLI)hys = V(SLI) – V(NSLI)	75	150		mV
Reverse Polarity Protection: VDDS, GNDS							
C01	Vs()	Saturation Voltage VDDS versus VDD	Vs(VDDS) = VDD – V(VDDS); I(VDDS) = -10 . . . 0 mA I(VDDS) = -25 . . . -10 mA			 150 300	 mV mV

ELECTRICAL CHARACTERISTICS

Operating conditions: VDD = 5 V ±10 %, Tj = -40...125 °C, CIBM adjusted to 200 µA, 4 mm NdFeB magnet, unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C02	Vs()	Saturation Voltage GNDS versus GND	Vs(GNDS) = V(GNDS) − GND; I(GNDS) = 0 . . . 10 mA I(GNDS) = 10 . . . 25 mA			 150 300	 mV mV

CHARACTERISTICS: Diagrams

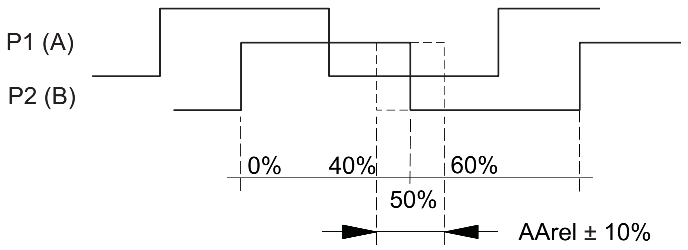

Figure 1: Definition of Relative Angular Accuracy

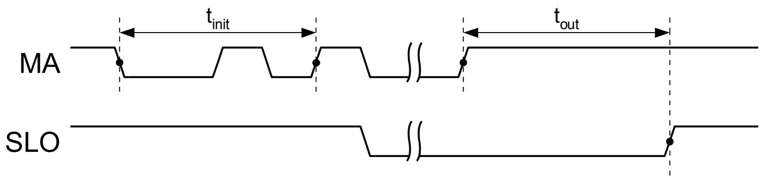

Figure 2: Adaptive Slave Timeout

OPERATING REQUIREMENTS: Multiturn Interface

Operating condition: VDD = 5 V ±10 %, Tj = -40...125 °C, CIBM adjusted to 200 µA

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
SSI Protocol (Figure 3)						
I001	t_{frame}	Clock Frame Repetition		16384/fsys		
I002	t_C	Clock Period		refer to Elec. Char. 713		
I003	t_{L1}, t_{L2}	Clock Signal hi/lo Level Duration		50		% t_C
I004	t_S	Setup Time: Data stable before clock edge lo → hi			50	ns
I005	t_H	Hold Time: Data stable after clock edge lo → hi			10	ns
I006	t_{out}	Permissible Slave Timeout		t_C	40	µs

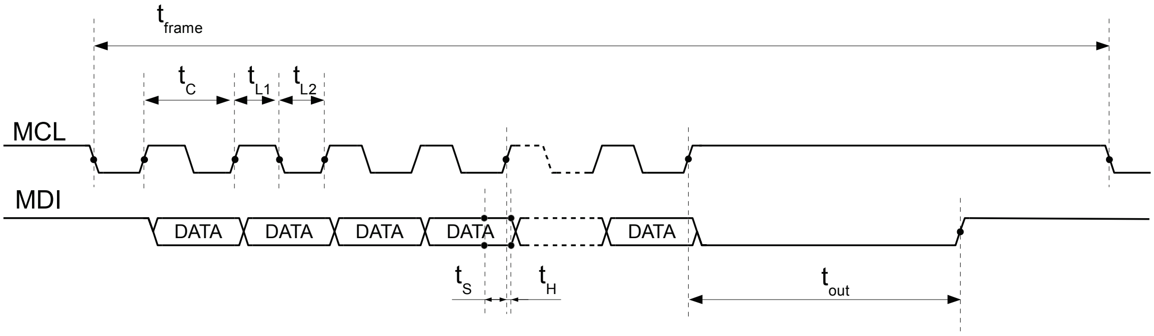

Figure 3: SSI Protocol Timing

OPERATING REQUIREMENTS: Serial Interface (BiSS, SSI)

Operating condition: VDD = 5 V ±10 %, Tj = -40...125 °C, CIBM adjusted to 200 μA

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
BiSS Protocol with RS422 or TTL signal levels (Figure 4)						
I101	t_{frame}	Permissible Frame Repetition		*	indefinite	
I102	t_{busy}	Processing Time w/o Start Bit Delay		$2 \cdot t_C$		
I103	t_{P3}	Output Propagation Delay		refer to Elec. Char. 931		
I104	t_{out}	Adaptive Slave Timeout		refer to Elec. Char. 904		
I105	t_C	Permissible Clock Period	RTX_MODE ≠ 2	70		ns
I106	t_{L1}	Clock Signal hi Level Duration	RTX_MODE ≠ 2	25	t_{out}	ns
I107	t_{L2}	Clock Signal lo Level Duration	RTX_MODE ≠ 2	25	t_{out}	ns
BiSS Protocol with LVDS signal levels (Figure 4)						
I108	t_C	Permissible Clock Period	RTX_MODE = 2	40		ns
I109	t_{L1}	Clock Signal hi Level Duration	RTX_MODE = 2	20	t_{out}	ns
I110	t_{L2}	Clock Signal lo Level Duration	RTX_MODE = 2	20	t_{out}	ns
SSI Protocol (Figure 5)						
I111	t_{frame}	Permissible Frame Repetition		*	indefinite	
I112	t_C	Permissible Clock Period		250		ns
I113	t_{L1}	Clock Signal hi Level Duration		30	t_{out}	ns
I114	t_{L2}	Clock Signal lo Level Duration		30	t_{out}	ns
I115	t_{RQ}	REQ Signal lo Level Duration		30		ns
I116	t_{P3}	Output Propagation Delay		refer to Elec. Char. 931		
I117	t_{out}	Adaptive Slave Timeout		refer to Elec. Char. 904		

*Allow t_{out} to elapse.

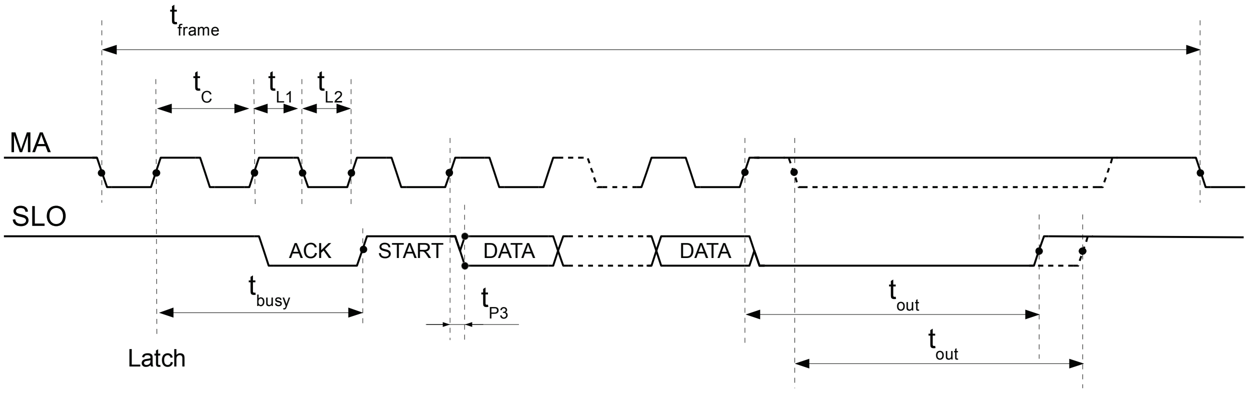

Figure 4: BiSS Protocol Timing

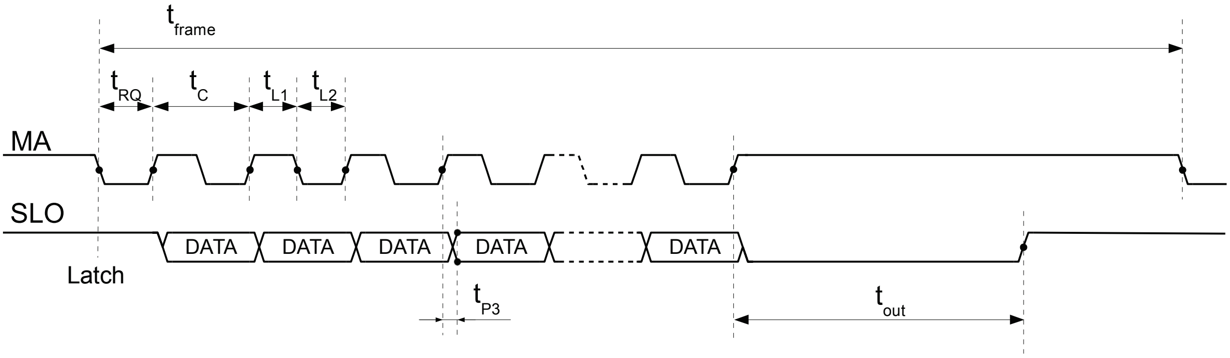

Figure 5: SSI Protocol Timing

OPERATING REQUIREMENTS: Serial Interface (SPI)

Operating condition: VDD = 5 V ±10 %, Tj = -40...125 °C, CIBM adjusted to 200 µA

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
SPI Protocol (Figure 6, 7)						
I201	t_{C1}	Permissible Clock Cycle Time		100		ns
I202	t_{L1}	Clock Signal lo Level Duration		50		ns
I203	t_{L2}	Clock Signal hi Level Duration		30		ns
I204	t_{H1}	Hold Time:NCS lo after MA lo → hi		100		ns
I205	t_{H2}	Hold Time: SLI stable after MA lo → hi		30		ns
I206	t_{S_IO1}	Setup Time: NCS lo before MA lo → hi		50		ns
I207	t_{S_IO2}	Setup Time: SLI stable before SCLK lo → hi		30		ns
I208	t_{P1}	Propagation Delay: SLO stable after MA hi → lo			30	ns
I209	t_{P2}	Propagation Delay: SLO hi after NCS	DISBISS = 0		30	ns
I210	t_{P3}	Propagation Delay: SLO hi impedance after NCS lo → hi	DISBISS = 1		30	ns
I211	t_{W1}	Wait Time: between NCS lo → hi and NCS hi → lo		500		ns
I212	t_{W2}	Wait Time: MA stable after NCS lo → hi		500		ns
I213	t_{H3}	Hold Time: NCS lo after MA hi → lo		50		ns

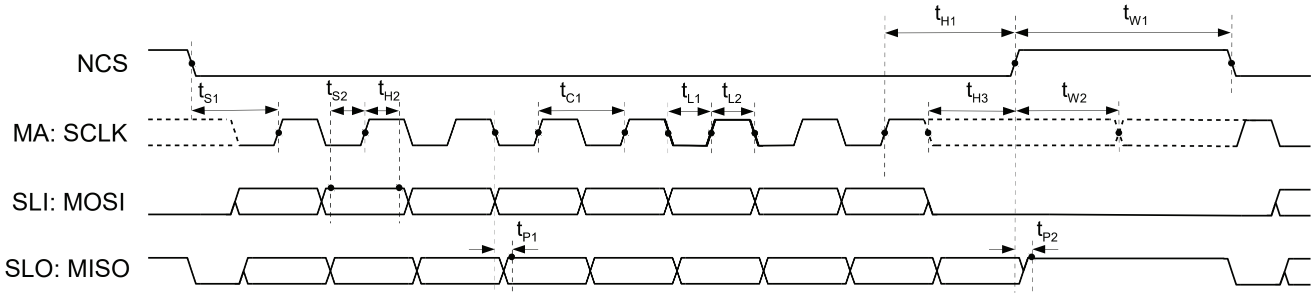

Figure 6: SPI Protocol Timing (DISBISS = 0)

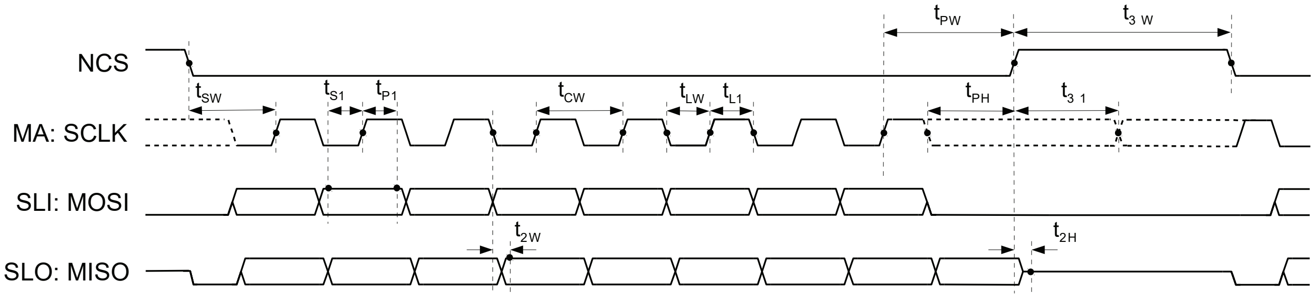

Figure 7: SPI Protocol Timing (DISBISS = 1)

REVERSE POLARITY PROTECTION

The iC-MHM provides reverse polarity protection for itself and external circuitry powered from its switched VDDS pin and switched GNDS pin. The output line drivers are also protected against reverse polarity and short circuits. This means that an incorrect connection of the device or a damaged cable will not harm the iC-MHM or external circuitry connected to its VDDS and GNDS pins.

Specifically, the following pins are protected against reverse polarity: PSIN, NSIN, PCOS, NCOS, MAO, NMAO, MA, NMA, SLI, NSLI, SLO, and NSLO. The maximum voltage difference between these pins must not exceed 6 V. In addition, GNDS must always be less than or equal to VDDS.

Note: Voltage at VDDS shall be bootstrapped by a diode connected vs. VDD to assure correct power-on, if reverse polarity function is used (see Figure 8).

Note: It is necessary to connect VDD to VDDS and GND to GNDS, if reverse polarity is not used.

OVERVOLTAGE PROTECTION

It is recommended to provide transient overvoltage protection for the iC-MHM as shown in Figure 8. This is especially important in applications where a long cable may be used between the iC-MHM and its power supply and data receivers.

Note: Circuit examples are provided for illustration of principle. Additional components required for a successful application may be omitted for clarity.

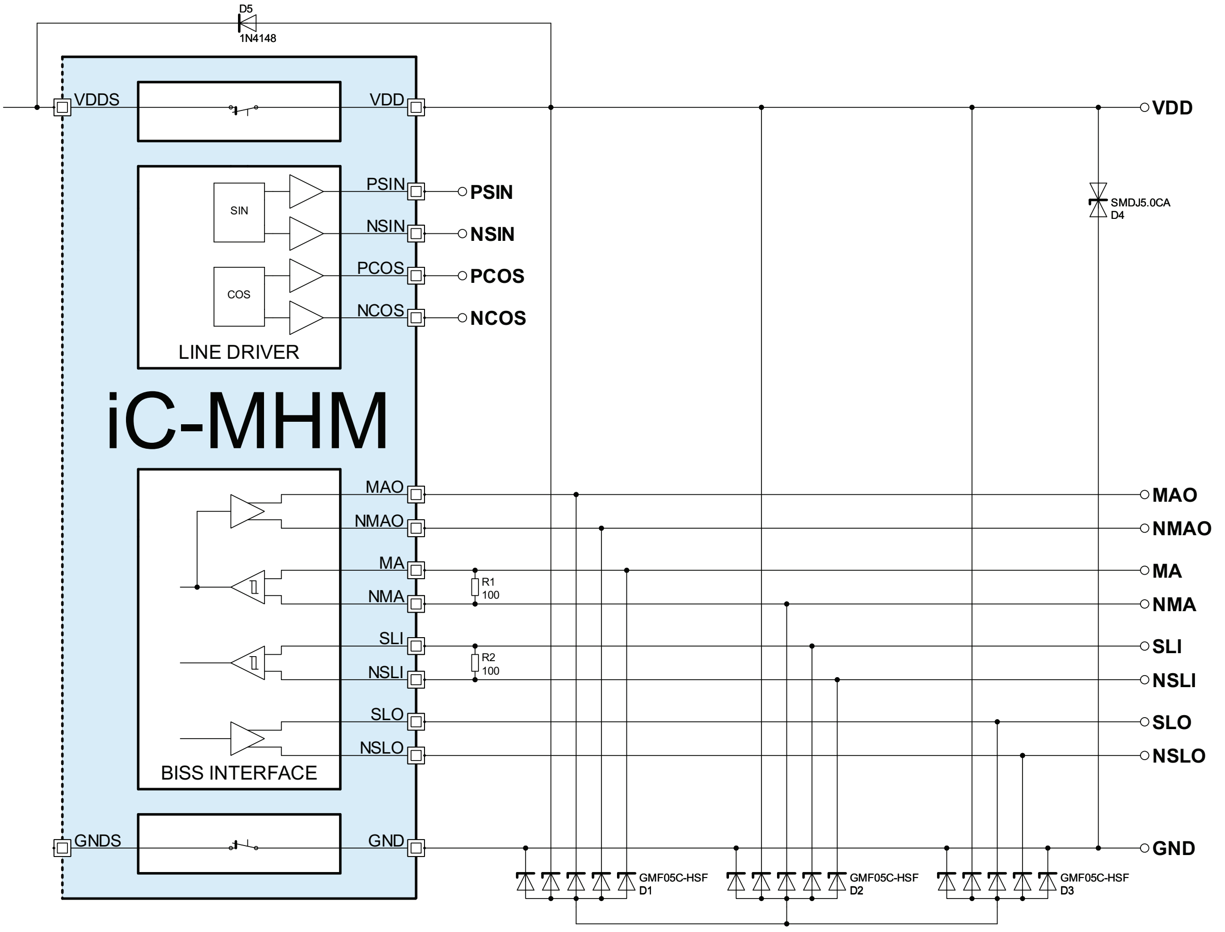

Figure 8: Recommended Transient Overvoltage Protection

CONFIGURATION PARAMETERS

Signal Conditioning .... Page 18

GAINR:	Coarse Gain Range
GAINF:	Fine Gain
ENAC:	Automatic Amplitude Control Enable
VOSS:	Offset Correction Sine
VOSC:	Offset Correction Cosine
GCC:	Gain Correction Cosine
ENF:	Filter Enable
HARMCAL:	Harmonic Calibration

Interpolator .... Page 21

RESO_ST:	Singleturn Resolution
AVGFILT:	Averaging Filter
DIR:	Code Direction
HYS:	Hysteresis
TLF:	Tracking Loop Frequency

Multiturn Interface .... Page 23

CF_MTI:	Clock Frequency
RESO_MT:	Multiturn Resolution
SBL_MTI:	Multiturn Synchronization Bits
EBL_MTI:	Multiturn Error Bits
GET_MTI:	Multiturn Interface Feedthrough

Digital I/O Port .... Page 26

CFG_IOP:	I/O Port Function
F_IO0:	MCL Force Level (pin 10)
F_IO1:	P1 Force Level (pin 5)
F_IO2:	P2 Force Level (pin 6)
F_IO3:	P3 Force Level (pin 7)
S_IO0:	MDI Sense Level (pin 11)
S_IO1:	P1 Sense Level (pin 5)
S_IO2:	P2 Sense Level (pin 6)
S_IO3:	P3 Sense Level (pin 7)
PRES_IO1:	Enable Preset Input P1
DIR_IO2:	Enable Code Direction Input P2
ENCMD2:	BiSS Command 2 Enable

Status Registers .... Page 30

ERR_CFG:	Configuration Data CRC Error
ERR_OFFS:	Output Offset CRC Error
ERR_POS:	Absolute Position Error
ERR_EXT:	External Error
ERR_AMIN:	Minimum Amplitude Error
ERR_AMAX:	Maximum Amplitude Error
ERR_MTI:	Multiturn Interface Error
ERR_MT:	Multiturn Position Error
GAIN:	Gain Control Value
CHIP_REL:	Chip Release

Instruction Registers .... Page 32

INSPROT:	Instruction Register Protection

Test Mode .... Page 33

TEST:	Test Mode

Serial Interface: General .... Page 36

RTX_MODE:	Transceiver Configuration

Serial Interface: BiSS Mode .... Page 37

ENSSI:	BiSS/SSI Protocol Selection
DISBISS:	Disable BiSS Interface
MT12:	Multiturn Bit Length
ENLC:	Sign-of-Life Counter Enable
CRCS:	CRC Start Value
NTOA:	Adaptive Timeout
ENCMD01:	BiSS Command 01 Enable
ENCMD2:	BiSS Command 2 Enable
ENCMD3:	BiSS Command 3 Enable
REGPROT:	BiSS Register Protection
INSPROT:	Instruction Register Protection
I2CDEV:	I²C Device ID
BSEL:	Bank Selection

Serial Interface: SSI Mode .... Page 44

ENSSI:	BiSS/SSI Protocol Selection
DISBISS:	Disable BiSS Interface
EXT_SSI:	SSI Protocol
BIN_SSI:	SSI Numeric Format (Gray or binary)
MT12:	Multiturn Bit Length
NTOA:	Adaptive Timeout
ENLC:	Sign-of-Life Counter Enable

Serial Interface: SPI Mode .... Page 46

DISBISS:	Disable BiSS Interface
RESO_MT:	Multiturn Resolution (SPI)

Configuration .... Page 52

CRC_CFG:	Configuration Data Checksum

Calibration .... Page 54

CIBM:	Bias Current Calibration

Position Offset and Preset .... Page 55

OFFS_MT:	Multiturn Offset
OFFS_ST:	Singleturn Offset
CRC_OFFS:	Position Offset Checksum
PSET_MT:	Multiturn Preset Position
PSET_ST:	Singleturn Preset Position
CRC_PSET:	Preset Position Checksum

REGISTER MAP: RAM

OVERVIEW

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Interpolator								
0x00	HYS		DIR	TLF			AVGFILT	
0x01	0	RESO_ST			0	RESO_MT		
Multiturn Interface								
0x02	GET_MTI	EBL_MTI			SBL_MTI			CF_MTI
Serial Interface								
0x03	ENSSI	EXT_SSI	BIN_SSI	RTX_MODE		MT12	CFG_IOP	
Signal Conditioning								
0x04	ENF	VOSS						
0x05	HARMCAL(4)	VOSC						
0x06	HARMCAL(3:0)				CIBM			
0x07	0	NTOA	DISBISS	TEST				
0x08	GAINR		GAINF					
0x09	ENAC	GCC						
Safety								
0x0A	0	ENLC	CRCS					
Enable								
0x0B	0	ENCMD01	ENCMD2	ENCMD3	DIR_IO2	PRES_IO1	INSPROT	REGPROT
CRC								
0x0C	CRC_CFG							
Output Offset and CRC								
0x0D	OFFS_MT(31:24)							
0x0E	OFFS_MT(23:16)							
0x0F	OFFS_MT(15:8)							
0x10	OFFS_MT(7:0)							
0x11	OFFS_ST(15:8)							
0x12	OFFS_ST(7:0)							
0x13	CRC_OFFS							
Bank Selection								
0x40	I2CDEV			BSEL				
Status Registers (read only)								
0x70	ERR_MT	ERR_MTI	ERR_AMAX	ERR_AMIN	ERR_EXT	ERR_POS	ERR_OFFS	ERR_CFG
0x71	0	0	0	0	S_IO3	S_IO2	S_IO1	S_IO0 (MDI)
0x72	GAIN							
0x73	CHIP_REL*							
Instruction Registers								
0x74	0	0	0	0	0	0	PRESET	RESET
0x75	0	0	0	0	F_IO3	F_IO2	F_IO1	F_IO0 (MCL)
0x76	GAIN							
0x77	Reserved (do not use)							

*Undefined for chip revisions prior to X5

Table 1: Register layout

HALL SENSORS: Principle of Operation

The iC-MHM contains four Hall sensors equally spaced on a 2.42 mm diameter circle for sensing the field of a diametrically magnetized, cylindrical permanent magnet as shown in Figure 9.

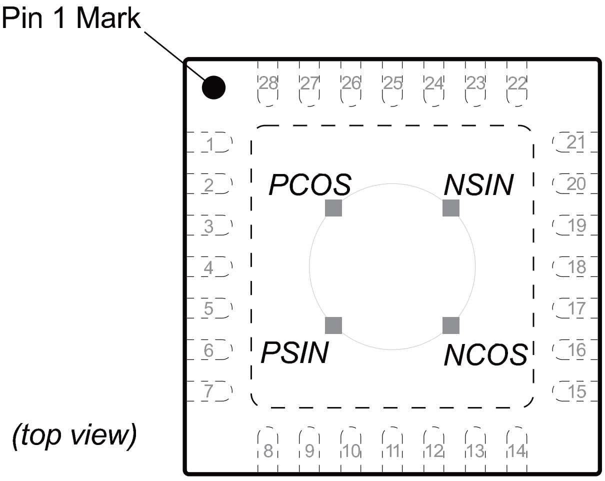

Figure 9: Hall Sensor Locations

This sensor arrangement allows a very tolerant alignment of the iC-MHM to the rotational axis of the magnet.

Each of the four sensors produces a voltage (the Hall voltage) proportional to the magnetic field strength at the position of the sensor. As shown in Figure 10, only the Z component of the magnetic field (the component perpendicular to the surface of the iC-MHM) is sensed.

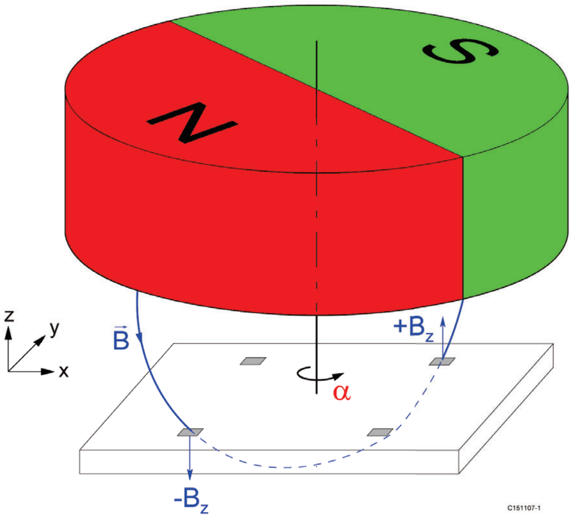

Figure 10: Sensor Principle

Note: The field direction for each sensor is opposite to that of the sensor directly opposite to it. Thus, opposite sensors generate opposite polarity Hall voltages.

By subtracting the Hall voltages from opposite sensors, the effects of homogeneous stray fields are eliminated and two differential Hall signals are generated. As shown in Figure 11, these signals are proportional to the sine and cosine of the magnet angle, α.

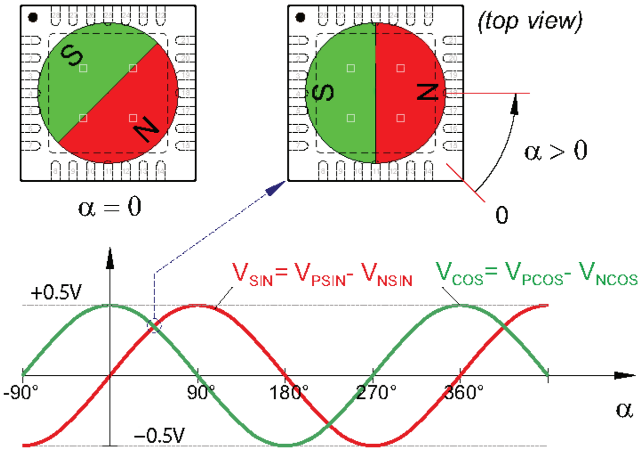

Figure 11: Sine and Cosine Hall Signals

These two signals are used by the interpolator to determine the angular position of the magnet. The zero position ($\alpha = 0$) of the system is where the South pole of the magnet is over the PCOS sensor (the one closest to pin 1 of the iC-MHM) as shown in Figure 12.

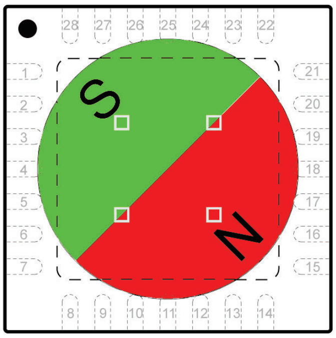

Figure 12: Zero Position of the Magnet

Optimum sensor signals are generated by a diametrically magnetized, cylindrical permanent magnet with a diameter, D, of 4 mm and an axial length, L, of 4 mm. Magnets of neodymium iron boron (NdFeB) or samarium cobalt (SmCo) are very well suited to the iC-MHM and are hardly influenced by external stray fields. Different size magnets can be used with the iC-MHM, but the length-to-diameter ratio, L/D, of the magnet should be between 0.3 to 2 to ensure sufficient field strength.

SIGNAL CONDITIONING

The iC-MHM provides conditioning of the Hall signals to equalize amplitudes, remove offsets, and correct harmonic distortion. An automatic amplitude control is provided which maintains optimum signal amplitudes despite changes in air gap between the magnet and the iC-MHM, temperature, or supply voltage. All correction values must be determined individually for every device and set manually.

Coarse Gain Range (GAINR)

The Hall signals are amplified in two stages. The first stage amplifier gain is set using parameter GAINR.

GAINR	Address 0x08; bits 7:6
Value	Coarse Gain Range
0	5
1	10
2	14.5
3	17.5

Table 2: Coarse Gain Range

Note: A coarse gain range of 17.5 (GAINR = 3) should be used initially as part of the default configuration. After setting the gain, a Reset instruction must be executed via BiSS or SPI for the changed parameter to take effect. Refer to INSTRUCTION REGISTERS on page 32 for more information.

Fine Gain (GAINF)

The second amplifier stage provides a fine gain adjustment using parameter GAINF.

GAINF	Address 0x08; bits 5:0
Value	Fine Gain
0x00	1.000
0x01	1.048
...	$exp(\frac{ln(20)}{64} \cdot GAINF)$
0x3F	19.08

Table 3: Fine Gain

Note: A fine gain of 1.000 (GAINF = 0x00) should be used initially as part of the default configuration. After setting the gain, a Reset instruction must be executed via BiSS or SPI for the changed parameter to take effect. Refer to INSTRUCTION REGISTERS on page 32 for more information.

Automatic Amplitude Control Enable (ENAC)

The integrated automatic amplitude control is enabled using bit ENAC. It is recommended to always use the automatic amplitude control to ensure that the interpolator is operating with optimum signal levels.

ENAC	Address 0x09; bit 7
Value	Description
0	Automatic Amplitude Control Disabled
1	Automatic Amplitude Control Enabled

Table 4: Automatic Amplitude Control Enable

When enabled, the automatic amplitude control maintains the amplitude of the differential sine and cosine signals at 1 Vpp by varying GAINR and GAINF from their initial values as required. The sine and cosine signals can be monitored at the PSIN, NSIN, PCOS, and NCOS outputs as shown in Figure 13.

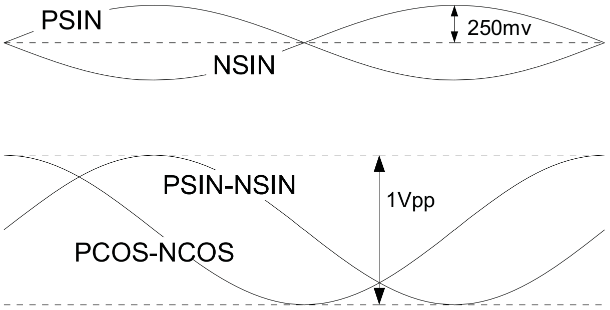

Figure 13: Hall Signal Amplitudes with Automatic Amplitude Control Enabled

When automatic gain control is enabled, the gain control value use at any time is available in the gain status register. Refer to STATUS REGISTERS on page 30 for more information.

If the Hall signal amplitudes are too low even with maximum gain, bit ERR_AMIN in the error status register is set, the error output is activated (pin NERR low), and the error bit in the BiSS SCD, SPI position read command response, and extended SSI frame are also activated (nERR = nE = 0). Likewise, if the Hall signal amplitudes are too large even with minimum gain, bit ERR_AMAX is set, the error output is activated (pin NERR low), and the error bit in the BiSS SCD, SPI position read command response, and extended SSI frame are also activated (nERR = nE = 0). Refer to STATUS REGISTERS on page 30 for more information.

Offset Correction (VOSS and VOSC)

Voltage offset in the sine and cosine signals can be corrected (compensated) using the VOSS and VOSC parameters.

VOSS	Address 0x04; bits 6:0	
VOSC	Address 0x05; bits 6:0	
Value	Offset Correction	Angle Error Correction
0x00	0 mV	0°
0x01	0.5 mV	0.06°
...	...	...
0x3F	31.5 mV	3.7°
0x40	0 mV	0°
0x41	-0.5 mV	-0.06°
...	...	...
0x7F	-31.5 mV	-3.7°

Table 5: Offset Correction Sine and Cosine

An offset correction range of ±31.5 mV is provided for each channel. This will correct angle errors of up to ±3.7° due to offsets. Refer to CALIBRATION PROCEDURE on page 54 for information on calibrating the offset correction values.

Gain Correction Cosine (GCC)

Parameter GCC allows trimming the gain of the cosine channel to ensure that the amplitudes of the sine and cosine signals are identical.

GCC	Address 0x09; bits 6:0	
Value	Gain Correction Cosine	Angle Error Correction
0x00	1.000	0°
0x01	1.0015	0.04°
...	$exp(\frac{ln(20)}{2048} \cdot GCC)$	
0x3F	1.0965	2.7°
0x40	0.9106	-2.7°
...	$exp(-\frac{ln(20)}{2048} \cdot (128 - GCC))$	
0x7F	0.9985	-0.04°

Table 6: Gain Correction Cosine

A gain correction cosine range of approximately ±10% is provided. This will correct angle errors of up to ±2.7° due to gain imbalance. Refer to CALIBRATION PROCEDURE on page 54 for information on calibrating the gain correction cosine.

Filter Enable (ENF)

A filter is provided to suppress noise on the sine and cosine signals. The filter cutoff frequency is set using parameter ENF.

ENF	Address 0x04; bit 7
Value	Cutoff Frequency
0	16 kHz
1	3 kHz

Table 7: Filter Enable

The optimal filter cutoff frequency depends on the maximum magnet rotation speed. In general, use a 3 kHz cutoff frequency (ENF = 1).

Harmonic Calibration (HARMCAL)

After calibration of offsets and gain, a residual angle error harmonic at a frequency of four times per magnet revolution remains. This error can be reduced using parameter HARMCAL.

HARMCAL	Address 0x05; bit 7 Address 0x06; bits 7:4	
Value	Correction	Angle Error Correction
0x00	0 LSB	0°
0x01	1 LSB	0.05°
...	...	...
0x0F	15 LSB	0.75°
0x10	0 LSB	0°
0x11	-1 LSB	-0.05°
...	...	...
0x1F	-15 LSB	-0.75°

Table 8: Harmonic Calibration

Note: Parameter HARMCAL impacts the interpolator but not the sine/cosine output signals.

Figure 14 shows how harmonic calibration operates. The blue signal (top) shows the typical residual angular error of the iC-MHM after offsets and gain have been calibrated. The purple signal (middle) is the HARMCAL (compensation) signal. These two signals are added together to reduce the 4th harmonic angular error, as shown by the green signal (bottom). Refer to CALIBRATION on page 54 for information on tuning the harmonic calibration.

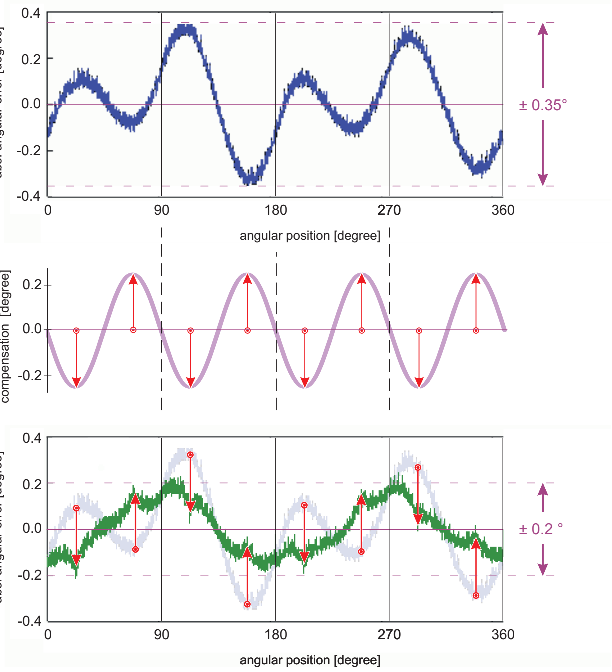

Figure 14: Harmonic Calibration

INTERPOLATOR

The internal interpolator in the iC-MHM converts the conditioned sine and cosine signals from the Hall sensors into an angular position value with a configurable resolution of between 9 and 14 bits. This angular position is available over the serial interface in BiSS, SSI, or SPI modes. In addition, the digital I/O port can be configured to output the change in position as incremental quadrature signals. Refer to DIGITAL I/O PORT on page 26 for more information.

Singleturn Resolution (RESO_ST)

The singleturn resolution of the iC-MHM is determined by the interpolator resolution as set using parameter RESO_ST.

RESO_ST	Address 0x01; bits 6:4	
Value	Resolution: Bits	Counts or Edges per Revolution
0	16	65 536
1	15	32 768
2	14	16 384
3	13	8 192
4	12	4 096
5	11	2 048
6	10	1 024
7	9	512

Table 9: Singleturn Resolution

Note: Resolutions above 12 bits require use of the averaging filter (AVGFILT ≠ 0). Resolutions above 14 bits are not recommended. Resolution of the ABZ signals is limited to 12 bit.

Averaging Filter (AVGFILT)

The averaging filter is enabled using parameter AVGFILT to allow singleturn resolutions above 12 bits.

AVGFILT	Address 0x00; bits 1:0	
Value	Filter	Typical Latency
0	None	0.0 µs
1	Light	1.2 µs
2	Medium	2.3 µs
3	Heavy	4.6 µs

Table 10: Averaging Filter

While the averaging filter allows higher resolutions, it reduces the maximum magnet rotation speed and also introduces latency into the position measurement. For fastest response and highest magnet rotation speed, disable the filter (AVGFILT = 0) and use an interpolator resolution of 12 bits or less (RESO_ST $\geq$ 4).

Code Direction (DIR)

The positive direction of rotation (increasing angular position) is determined by parameter DIR and the enable preset input P1 (if enabled).

If the enable preset input P1 is not used (DIR_IO2 = 0), then with DIR = 0, counterclockwise rotation of the magnet when viewed from the top of the iC-MHM results in increasing angular position. This can be inverted by setting DIR = 1, in which case clockwise rotation of the magnet results in increasing angular position.

DIR	Address 0x00; bit 5
Value	Positive Rotation
0	Counterclockwise (Normal)
1	Clockwise (Inverted)

Table 11: Code Direction (DIR_IO2 = 0)

If the enable preset input P1 is used (DIR_IO2 = 1), then parameter DIR is exclusive-ORed with the state of the code direction input to determine the positive code direction.

Rot. Dir. Input	**DIR**	**Positive Rotation**
0	0	Counterclockwise (Normal)
0	1	Clockwise (Inverted)
1	0	Clockwise (Inverted)
1	1	Counterclockwise (Normal)

Table 12: Code Direction (DIR_IO2 = 1)

Refer to DIGITAL I/O PORT on page 26 for information on configuring the enable code direction input P2 and parameter DIR_IO2.

Parameter DIR and the enable code direction input P2 (if enabled) also reverses the direction of the incremental quadrature outputs, if used (CFG_IOP = 2). Refer to Incremental Quadrature (ABZ) Outputs on page 29 for information on using the digital I/O port as incremental encoder (ABZ) outputs.

Hysteresis (HYS)

Hysteresis is used to prevent flickering of the angular position LSBs and dithering of the incremental quadrature outputs. The amount of hysteresis is determined by parameter HYS.

HYS	Address 0x00; bits 7:6	
Value	Hysteresis (Magnet Rotation Angle)	
	AVGFILT = 0	AVGFILT > 0
0	0.00°	0.00°
1	0.17°	0.00°
2	0.35°	0.09°
3	0.53°	0.61°

Table 13: Hysteresis

Tracking Loop Frequency (TLF)

The optimal frequency of the interpolator tracking loop for any given application is determined by the maximum required rotational speed of the magnet (RPM_{max}), the required angular position resolution (parameter RESO_ST), and the averaging filter setting (AVGFILT). Parameter TLF sets the maximum tracking loop frequency.

TLF	Address 0x00; bits 4:2
Value	Tracking Loop Frequency
0	fsys
1	fsys/2
2	fsys/3
3	fsys/4
4	fsys/5
5	fsys/6
6	fsys/7
7	fsys/8

Table 14: Tracking Loop Frequency

In general, higher tracking loop frequencies provide higher maximum magnet rotation speed . For optimal accuracy with the averaging filter enabled ($AVGFILT \neq 0$), use the tracking loop frequency that is less than or equal to 4 MHz ($TLF \geq 3$).

When the averaging filter is not used ($AVGFILT = 0$), TLF is calculated as:

$$TLF \leq INT\left(\frac{fsys \cdot 60}{2^{(16-RESO\_ST)} \cdot RPM_{max}} - 1\right)$$

Where fsys is the system clock frequency (refer to Elec. Char. item no. 501). To guarantee operation under all conditions, the minimum fsys of 11.5 MHz should be used for all calculations.

For example, for an application without averaging filtering requiring 12-bit singleturn resolution and a maximum magnet rotation speed of 50 kRPM, TLF is calculated as:

$$TLF \leq INT\left(\frac{11\,500\,000 \cdot 60}{2^{(16-4)} \cdot 50\,000} - 1\right) = 2$$

It is recommended to always use the highest TLF value that provides the required maximum magnet rotation speed at the required resolution.

When the averaging filter is used ($AVGFILT \neq 0$), TLF is independent of the resolution (RESO_ST) and is calculated as:

$$TLF \leq INT\left(\frac{fsys \cdot 60}{2^{(13+AVGFILT)} \cdot RPM_{max}} - 1\right)$$

Where fsys is the system clock frequency (refer to Elec. Char. item no. 501). To guarantee operation under all conditions, the minimum fsys of 11.5 MHz should be used for all calculations.

For example, for an application with medium averaging filtering requiring a maximum magnet rotation speed of 3 000 RPM, TLF is calculated as:

$$TLF \leq INT\left(\frac{11\,500\,000 \cdot 60}{2^{(13+2)} \cdot 3\,000} - 1\right) = 6$$

It is recommended to always use the highest TLF value that provides the required maximum magnet rotation speed with the selected level of filtering.

The maximum magnet rotation speed for all settings of TLF, RESO_ST, and AVGFILT is shown in Table 15. Exceeding these speeds causes the averaging position value to lag behind the actual mechanical position of the magnet. A position lag of $\geq 90°$ results in a discontinuity (jump) in the averaging position output and a BiSS, extended SSI, or SPI warning (nWARN = nW = 0). It also activates the error output (pin NERR low) if the incremental outputs are enabled (CFG_IOP = 2). Refer to DIGITAL I/O PORT on page 26 for more information on the incremental outputs.

TLF	Address 0x00; bits 4:2							
Value	Tracking Loop Frequency	Permissible Magnet Rotation Speed [RPM]						
		AVGFILT = 0 (No Filtering)				AVGFILT = 1	AVGFILT = 2	AVGFILT = 3
		9 bit	10 bit	11 bit	12 bit	9 ... 16 bit		
0x00	11.5 MHz	1347 656	673 828	336 914	168 457	42 114	21 057	10 529
0x01	5.75 MHz	673 828	336 914	168 457	84 229	21 057	10 529	5 264
0x02	3.83 MHz	449 219	224 609	112 305	56 152	14 038	7 019	3 510
0x03	2.88 MHz	336 914	168 457	84 229	42 114	10 529	5 264	2 632
0x04	2.3 MHz	269 531	134 766	67 383	33 691	8 423	4 211	2 106
0x05	1.92 MHz	224 609	112 305	56 152	28 076	7 019	3 510	1 755
0x06	1.64 MHz	192 522	96 261	48 131	24 065	6 016	3 008	1 504
0x07	1.44 MHz	168 457	84 229	42 114	21 057	5 264	2 632	1 316

Table 15: Tracking Loop Frequency and Maximum Magnet Rotation Speed for fsys = 11.5 MHz

MULTITURN INTERFACE

The iC-MHM provides a dedicated SSI master interface (the multiturn interface) which is used to read multiturn position (turns count) from an external multiturn counter or sensor. The turns count value is synchronized with the singleturn position (angle) from the iC-MHM to form the complete absolute position value which is then available via the main serial interface in BiSS, SSI, or SPI format.

When enabled (SBL_MTI ≠ 0), the iC-MHM reads the multiturn position at startup and uses it to initialize its internal multiturn counter. In addition, during operation, the multiturn position continues to be read via the multiturn interface approximately every 1.3 ms (Elec. Char. item no. I001) and compared to the internal multiturn position. If the internal multiturn counter value and the external multiturn count differ, the internal value is replaced by the new value from the multiturn interface and bit ERR_MT in the error status register is set. This activates the error output (pin NERR low) and activates the error bit in the BiSS SCD, SPI position read command response, and extended SSI frame (nERR = nE = 0). Refer to STATUS REGISTERS on page 30 for more information.

The SSI multiturn interface uses dedicated clock (MCL) and data (MDI) pins to read the multiturn position from an external device as shown in Figure 15.

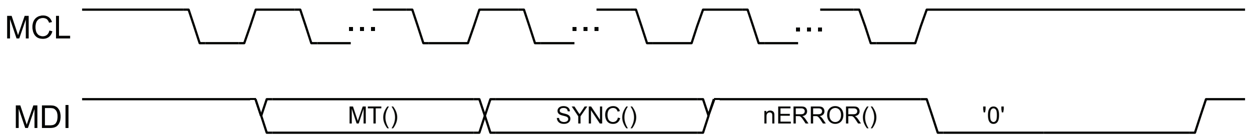

Figure 15: SSI Multiturn Interface Operation

The iC-MHM supplies the SSI clock at pin MCL for the external multiturn sensor at a frequency determined by parameter CF_MTI. The external multiturn sensor must then clock out the required number of multiturn position, synchronization, and error bits, followed by a trailing zero. If the data transmission does not end in a zero or if one of the error bits is active (0), status bit ERR_MTI in the error status register is set. This activates the error output (pin NERR low) and activates the error bit in the BiSS SCD, SPI position read command response, and extended SSI frame (nERR = nE = 0). Refer to STATUS REGISTERS on page 30 for more information.

Clock Frequency (CF_MTI)

Parameter CF_MTI determines the clock frequency used by the SSI multiturn interface to read the external multiturn sensor.

CF_MTI	Address 0x02; bit 0
Value	Clock Frequency
0	fsys/8 (1.4 MHz at fsys = 11.5 MHz)
1	fsys/64 (180 kHz at fsys = 11.5 MHz)

Table 16: Clock Frequency

fsys is the system clock frequency (Elec. Char. item no. 501). In general, use the fastest clock frequency supported by the external multiturn sensor to minimize transmission time.

Multiturn Resolution (RESO_MT)

The number of multiturn bits expected by the iC-MHM from the external multiturn counter and the length of the iC-MHM's internal multiturn counter is determined by parameter RESO_MT.

RESO_MT	Address 0x01; bits 2:0
Value	Resolution (Bits)
0	0 (Multiturn counter not used)
1	4
2	8
3	12
4	16
5	20
6	24
7	32

Table 17: Multiturn Resolution

Any RESO_MT value may be used in BiSS or SSI mode, but only certain values can be used in SPI mode. Refer to Table 88 on page 48 for more information. In all cases, the number of bits supplied by the external multiturn counter must match the RESO_MT value. If the multiturn counter is not needed, set RESO_MT = 0.

Multiturn Synchronization Bits (SBL_MTI)

To guarantee correct multiturn synchronization up to five synchronization bits can be used. Synchronization bits are the MSBs of the singleturn position and indicate the position of the multiturn sensor within a single turn. When one synchronization bit is used, the position of the multiturn sensor is known to 180°. When two bits are used, the position of the multiturn sensor is known to 90°, etc.

When the multiturn count (including synchronization bits) is read from the external multiturn sensor, the synchronization bits are compared to the corresponding bits of the iC-MHM singleturn position. If necessary, the multiturn count read in is corrected by subtracting one turn to provide correct synchronization.

Because the iC-MHM can only decrement the multiturn count read from the SSI multiturn interface, the multiturn sensor must be mounted (or programmed) with a phase advance relative to the iC-MHM. In other words, the 0° point of the multiturn sensor must occur before the 0° point of the iC-MHM with positive rotation.

The amount of phase advance required depends on the number of synchronization bits used as shown in Table 18.

SBL_MTI	Address 0x02; bits 3:1		
Value	Sync Bits	Phase Advance	Tolerance
0	Multiturn Interface Disabled		
1	1	-90 °	± 90 °
2	2	-135 °	± 135 °
3	3	-157.5 °	± 157.5 °
4	4	-168.75 °	± 168.75 °
5	5	-174.375 °	± 174.375 °
6	Reserved (Do not use)		
7	Reserved (Do not use)		

Table 18: Multiturn Synchronization Bits

The tolerances shown in Table 18 are the maximum rotation allowed during the time for the multiturn count to be transmitted from the external multiturn sensor to the iC-MHM. This value must also take into account the mechanical misalignment of the two sensors due to assembly variations.

Exceeding these tolerance values at startup results in a wrong multiturn count being used in the iC-MHM. Exceeding these values during operation sets ERR_MT in the error status register. This activates the error output (pin NERR low) and activates the error bit in the BiSS SCD, SPI position read command response, and extended SSI frame (nERR = nE = 0). Refer to STATUS REGISTERS on page 30 for more information on errors.

The amount of time to transmit the multiturn count from the external multiturn sensor to the iC-MHM, t_{SSI}, is calculated as

$$t_{\mathrm{SSI}} = \frac{8^{(\mathrm{CF\_MTI}+1)}}{fsys} \cdot (RESO\_MT + SBL\_MTI + EBL\_MTI)$$

Where fsys is the system clock frequency (Elec. Char. item no. 501) and t_{out} is the SSI slave timeout (Elec. Char. item no. I006).

For example, for 24 multiturn bits (RESO_MT = 6), one synchronization bit (SBL_MTI = 1), one error bit (EBL_MTI = 1), and an SSI clock frequency of $\frac{fsys}{64}$ (CF_MTI = 1),

$$t_{\mathrm{SSI}} = \frac{8^{(1+1)}}{11\,500\,000} \cdot (24 + 1 + 1) = 145\,\mu s$$

The magnet rotation angle during this time, θ_{SSI}, is calculated as

$$\theta_{\mathrm{SSI}}\,[^\circ] = \frac{Magnet\ Speed\,[RPM]}{60} \cdot t_{\mathrm{SSI}} \cdot 360^\circ$$

Continuing the example, with an input rotation speed of 72 000 RPM, the magnet moves by an angle of

$$\frac{72\,000}{60} \cdot 145\,\mu s \cdot 360^\circ = 62.64^\circ$$

during the multiturn SSI transmission. To guarantee not exceeding the angle tolerance for one synchronization bit (90 °), the alignment error between the multiturn sensor and the iC-MHM can thus be no more than 27 °.

The multiturn interface is disabled when SBL_MTI = 0, but the iC-MHM's internal multiturn counter still counts turns. When the multiturn interface is disabled, the MCL output and MDI input can be used as additional discrete I/O. Refer to DIGITAL I/O PORT on page 26 for more information.

Multiturn Error Bits (EBL_MTI)

Up to four error bits from the external multiturn sensor can be included in the SSI transmission.

EBL_MTI	Address 0x02; bits 6:4
Value	Error Bits
0	0 (Error bits not used)
1	1
2	2
3	3
4	4
5 . . . 7	Reserved (Do not use)

Table 19: Multiturn Error Bits

Error bits are active low. If any bit is 0, ERR_MTI in the error status register is set. This activates the error output (pin NERR low) and activates the error bit in the BiSS SCD, SPI position read command response, and extended SSI frame (nERR = nE = 0). Refer to STATUS REGISTERS on page 30 for more information.

Multiturn Interface Feedthrough Mode

Multiturn interface feedthrough mode allows the external multiturn sensor to be read directly via the serial interface in SSI mode for diagnostic purposes. If the serial interface is set to SSI mode (ENSSI = 1), multiturn interface feedthrough mode is enabled when GET_MTI = 1.

GET_MTI	Address 0x02; bit 7
Value	Multiturn Interface Feedthrough Mode
0	Disabled
1	Enabled

Table 20: Multiturn Interface Feedthrough Mode

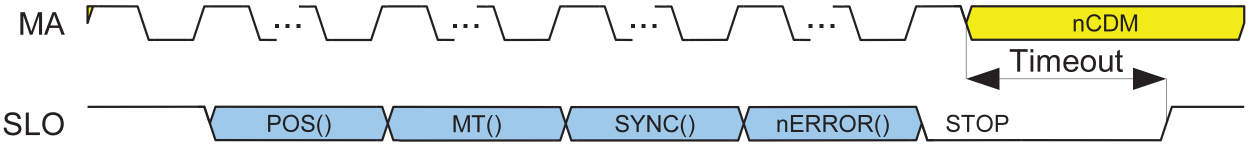

Figure 16: SSI Multiturn Interface Feedthrough

In multiturn interface feedthrough mode, the serial clock input (MA) signal is sent directly to the multiturn interface clock output (MCL), and the data clocked in on the multiturn data input (MDI) is supplementing the internal position data in the SSI transmission. Refer to SERIAL INTERFACE: SSI MODE on page 43 for more information.

DIGITAL I/O PORT

The iC-MHM provides a multi-function 4-bit digital I/O port that can be configured as general-purpose discrete I/O, dedicated discrete I/O, incremental quadrature (ABZ) outputs, or special calibration outputs. Parameter CFG_IOP determines the function of the digital I/O port.

CFG_IOP	Address 0x03; bits 1:0
Value	Digital I/O Port Function
0	Discrete I/O (General-Purpose or Dedicated)
1	Reserved (Do not use)
2	Incremental Quadrature (ABZ) Outputs
3	Calibration Signal Outputs

Table 21: I/O Port Function

Refer to Incremental Quadrature (ABZ) Outputs on page 29 for information on using the digital I/O port as incremental encoder (ABZ) outputs (CFG_IOP = 2).

Refer to CALIBRATION PROCEDURE on page 54 for information on using the digital I/O port for device calibration (CFG_IOP = 3).

Digital I/O 1 (P1)

P1 can be used as a general purpose discrete input or output, a dedicated position preset input, incremental encoder output A, or calibration signal output CS1.

P1	Pin 5		
CFG_IOP 0x03(1:0)	**PRES_IO1** 0x0B(2)	**F_IO1** 0x75(1)	**Function**
0	0	0	Output Low/Input
0	0	1	Output High
0	1	X	Preset Input
1	X	X	Reserved
2	X	X	Inc. Output A
3	X	X	Cal. Signal CS1

Table 22: Digital I/O 1

To use P1 as a general-purpose discrete output, set CFG_IOP = 0 and PRES_IO1 = 0. The state of P1 is then controlled by bit F_IO1 in the discrete output instruction register.

F_IO1	Address 0x75; bit 1
Value	Function
0	P1 Drives Weak Low (Force)
1	P1 Drives Strong High (Force)

Table 23: Discrete Output Instruction Register Bit F_IO1

Because P1 only drives a weak low when F_IO1 = 0, a buffer on P1 is recommended to provide a robust output.

To use P1 as a general-purpose discrete input, set CFG_IOP = 0, PRES_IO1 = 0, and F_IO1 = 0. The state of P1 is then available as bit S_IO1 in the discrete input status register.

S_IO1	Address 0x71; bit 1
Value	Condition
0	P1 Low (Sense)
1	P1 High (Sense)

Table 24: Discrete Input Status Register Bit S_IO1

The weak low driven by P1 when F_IO = 0 is overcome by the input signal when P1 is used as a discrete input.

To use P1 as a dedicated position preset input, set CFG_IOP = 0 and PRES_IO1 = 1. A position preset sequence is then initiated when P1 is high.

PRES_IO1	Addr. 0x0B; bit 2
Value	Function
0	P1 is General-Purpose Discrete I/O
1	P1 is Position Preset Input

Table 25: Enable Preset Input P1

When P1 is low, the iC-MHM operates normally. When P2 is high, a position preset sequence is initiated. Refer to POSITION OFFSET and PRESET (Zero Position) on page 55 for more information.

Digital I/O 2 (P2)

P2 can be used as a general purpose discrete input or output, a dedicated code direction input, incremental encoder output B, or calibration signal output CS2.

P2	Pin 6		
CFG_IOP 0x03(1:0)	**DIR_IO2** 0x0B(3)	**F_IO2** 0x75(2)	**Function**
0	0	0	Output Low/Input
0	0	1	Output High
0	1	X	Code Dir. Input
1	X	X	Reserved
2	X	X	Inc. Output B
3	X	X	Cal. Signal CS2

Table 26: Digital I/O 2

To use P2 as a general-purpose discrete output, set CFG_IOP = 0 and DIR_IO2 = 0. The state of P2 is then controlled by bit F_IO2 in the discrete output instruction register.

F_IO2	Address 0x75; bit 2
Value	Function
0	P2 Drives Weak Low (Force)
1	P2 Drives Strong High (Force)

Table 27: Discrete Output Instruction Register Bit F_IO2

Because P2 only drives a weak low when F_IO2 = 0, a buffer on P2 is recommended to provide a robust output.

To use P2 as a general-purpose discrete input, set CFG_IOP = 0, DIR_IO2 = 0, and F_IO2 = 0. The state of P2 is then available as bit S_IO2 in the discrete input status register.

S_IO2	Address 0x71; bit 2
Value	Condition
0	P2 Low (Sense)
1	P2 High (Sense)

Table 28: Discrete Input Status Register Bit S_IO2

The weak low driven by P2 when F_IO2 = 0 is overcome by the input signal when P2 is used as a discrete input.

To use P2 as a dedicated code direction input, set CFG_IOP = 0 and DIR_IO2 = 1. The positive code direction (increasing angle) is then controlled by the level at P2 and parameter DIR.

DIR_IO2	Addr. 0x0B; bit 3
Value	Function
0	P2 is General-Purpose Discrete I/O
1	P2 is Code Direction Input

Table 29: Enable Code Direction Input P2

Refer to Code Direction (DIR) on page 21 for information on determining code direction using the dedicated code direction input and parameter DIR.

Digital I/O 3 (P3)

P3 can be used as a general purpose discrete input or output, a BiSS command controlled output, incremental encoder output Z, or calibration signal output CS3.

P3	Pin 7		
CFG_IOP 0x03(1:0)	**ENCMD2** 0x0B(5)	**F_IO3** 0x75(3)	**Function**
0	0	0	Output Low/Input
0	0	1	Output High
0	1	X	BiSS Output
1	X	X	Reserved
2	X	X	Inc. Output Z
3	X	X	Cal. Signal CS3

Table 30: Digital I/O 3

To use P3 as a general-purpose discrete output, set CFG_IOP = 0 and ENCMD2 = 0. The state of P3 is then controlled by bit F_IO3 in the discrete output instruction register.

F_IO3	Address 0x75; bit 3
Value	Function
0	P3 Drives Weak Low (Force)
1	P3 Drives Strong High (Force)

Table 31: Discrete Output Instruction Register Bit F_IO3

Because P3 only drives a weak low when F_IO3 = 0, a buffer on P3 is recommended to provide a robust output.

To use P3 as a general-purpose discrete input, set CFG_IOP = 0, ENCMD2 = 0, and F_IO3 = 0. The state of P3 is then available as bit S_IO3 in the discrete input status register.

S_IO3	Address 0x71; bit 3
Value	Condition
0	P3 Low (Sense)
1	P3 High (Sense)

Table 32: Discrete Input Status Register Bit S_IO3

The weak low driven by P3 when F_IO3 = 0 is overcome by the input signal when P3 is used as a discrete input.

To use P3 as a BiSS-controlled output, set CFG_IOP = 0 and ENCMD2 = 1. The level at P3 is then determined by BiSS commands.

ENCMD2	Addr. 0x0B; bit 5
Value	Function
	Conditions: CFG_IOP = 0
0	P3 is General-Purpose Discrete I/O
1	P3 is BiSS Command Controlled Output
Note:	Pin level is low following power-on.

Table 33: BiSS Command 2 Enable: Controlling Pin P3

An addressed BiSS command with CMD = 2 sets P3 high. A BiSS broadcast command with CMD = 2 resets P3 low. Refer to SERIAL INTERFACE: BiSS MODE on page 37 for more information.

Digital I/O 0 (MDI and MCL)

When the multiturn SSI interface is disabled (SBL_MTI = 0), the MDI input (pin 11) and MCL output (pin 10) can be used as an additional general-purpose discrete input and output, respectively. Alternatively, these pins can be used to provide some of the discrete I/O functionality available on P1 - P3 when these pins are used for incremental quadrature (ABZ) outputs (CFG_IOP = 2) or device calibration outputs (CFG_IOP = 3).

SBL_MTI 0x02(3:1)	**CFG_IOP** 0x03(1:0)	**ENCMD2** 0x0B(5)	**DIR_IO2** 0x0B(3)	**PRES_IO1** 0x0B(2)	**F_IO0** 0x75(0)	**MCL Function** Pin 10	**MDI Function** Pin 11
0	0	X	X	X	0	OUT0 Strong Low	IN0
0	0	X	X	X	1	OUT0 Strong High	IN0
0	1	X	X	X	X	Reserved (Do not use)	Reserved (Do not use)
0	2 or 3	0	0	0	0	OUT0 Strong Low	IN0
0	2 or 3	0	0	0	1	OUT0 Strong High	IN0
0	2 or 3	0	0	1	0	OUT0 Strong Low	Preset Input
0	2 or 3	0	0	1	1	OUT0 Strong High	Preset Input
0	2 or 3	0	1	0	0	OUT0 Strong Low	Code Direction Input
0	2 or 3	0	1	0	1	OUT0 Strong High	Code Direction Input
0	2 or 3	1	0	0	X	BiSS Output	IN0
0	2 or 3	1	0	1	X	BiSS Output	Preset Input
0	2 or 3	1	1	0	X	BiSS Output	Code Direction Input
0	2 or 3	X	1	1	X	Reserved (Do not use)	Reserved (Do not use)
1	X	X	X	X	X	MCL	MDI

Table 34: Digital I/O 0

To use MCL as a general-purpose discrete output, set SBL_MTI = 0 and CFG_IOP = 0 or set SBL_MTI = 0, CFG_IOP = 2 or 3, and ENCMD2 = 0. The state of MCL is then controlled by bit F_IO0 in the discrete output instruction register.

F_IO0	Address 0x75; bit 0
Value	Function
0	MCL Drives Strong Low (Force)
1	MCL Drives Strong High (Force)

Table 35: Discrete Output Instruction Register Bit F_IO0

To use MDI as as a general-purpose discrete input, set SBL_MTI = 0 and CFG_IOP = 0 or set SBL_MTI = 0, CFG_IOP = 2 or 3, DIR_IO2 = 0, and PRES_IO1 = 0. The state of pin 11 is then available as bit S_IO0 in the discrete input status register.

S_IO0	Address 0x71; bit 0
Value	Condition
0	MDI Low (Sense)
1	MDI High (Sense)

Table 36: Discrete Input Status Register Bit S_IO0

To use MDI as a dedicated position preset input, set SBL_MTI = 0, CFG_IOP = 2 or 3, PRES_IO1 = 1, and

DIR_IO2 = 0. A position preset sequence is then initiated when MDI is high.

PRES_IO1	Addr. 0x0B; bit 2
Value	Function
	Conditions: CFG_IOP = 2 or 3, SBL_MTI = 0, DIR_IO2 = 0
0	MDI not Dedicated Position Preset Input
1	MDI is Dedicated Position Preset Input

Table 37: Enable Preset Input P1: Controlling Pin MDI

Refer to POSITION OFFSET and PRESET (Zero Position) on page 55 for more information.

To use MDI as a dedicated code direction input, set SBL_MTI = 0, CFG_IOP = 2 or 3, DIR_IO2 = 1, and PRES_IO1 = 0. The positive code direction (increasing angle) is then controlled by the level at MDI and parameter DIR.

DIR_IO2	Addr. 0x0B; bit 3
Value	Function
	Conditions: CFG_IOP = 2 or 3, SBL_MTI = 0, PRES_IO1 = 1
0	MDI not Dedicated Code Direction Input
1	MDI is Dedicated Code Direction Input

Table 38: Enable Code Direction Input P2: Controlling Pin MDI

Refer to Code Direction (DIR) on page 21 for information on determining code direction using the dedicated code direction input and parameter DIR.

To use MCL as a BiSS-controlled output, set SBL_MTI = 0, CFG_IOP = 2 or 3, and ENCMD2 = 1. The level at MCL is then determined by BiSS commands.

ENCMD2	Addr. 0x0B; bit 5
Value	Function
	Conditions: CFG_IOP = 2 or 3, SBL_MTI = 0
0	MCL is General-Purpose Discrete Output
1	MCL is BiSS Command Controlled Output
Note:	Pin level is low following power-on.

Table 39: BiSS Command 2 Enable: Controlling Pin MCL

When ENCMD2 = 0, MCL functions as general-purpose discrete output 0. When ENCMD2 = 1, an addressed BiSS command with CMD = 2 sets MCL high and a BiSS broadcast command with CMD = 2 resets MCL low. Refer to SERIAL INTERFACE: BiSS MODE on page 37 for more information.

Incremental Quadrature (ABZ) Outputs

To use the digital I/O port as incremental quadrature (ABZ) outputs, set CFG_IOP = 2. Pins P1 - P3 then output standard encoder quadrature signals.

	CFG_IOP = 2
Pin	Function
P1	Channel A Output
P2	Channel B Output
P3	Channel Z Output

Table 40: Digital I/O Port as Incremental Quadrature Outputs

Figure 17 shows the incremental quadrature outputs for positive code direction.

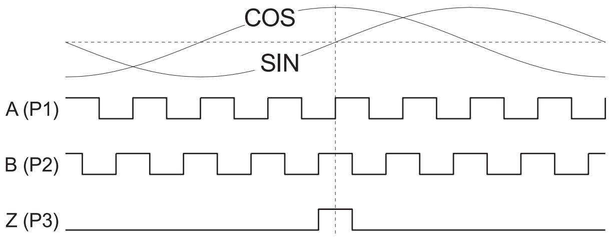

Figure 17: Incremental output

Channel B leads channel A for positive rotation as defined by parameter DIR or a configured code direction input. The Z output is centered around the iC-MHM's zero position and is two quadrature states (180°) wide. Figure 17 shows the case where OFFS_ST = 0x0000. Refer to POSITION OFFSET and PRESET (Zero Position) on page 55 for more information on setting the iC-MHM's zero position and parameter OFFS_ST.

The resolution of the ABZ signals is limited to 12 bit and can be set via RESO_ST = 4 and higher refer to Table 15 on page 21.

If the multiturn is used (RESO_MT ≠ 0), the Z output is active at the zero position only when the iC-MHM's internal multiturn counter overflows or underflows. If the multiturn is not used (RESO_MT = 0), the Z output is active at the zero position during every revolution of the magnet.

STATUS REGISTERS

The iC-MHM provides four status registers which are used to indicate errors in the device, the state of the general-purpose pins, the current gain in use by the automatic amplitude control for the Hall signals, and the chip revision.

Error

The error status register indicates the status of eight error conditions in the iC-MHM.

Error	Address 0x70	
Bit	Name	Description
0	ERR_CFG	Configuration Data CRC Error
1	ERR_OFFS	Position Offset CRC Error
2	ERR_POS	Absolute Position Not Available
3	ERR_EXT	External Error
4	ERR_AMIN	Minimum Amplitude Error
5	ERR_AMAX	Maximum Amplitude Error
6	ERR_MTI	Multiturn Interface Error
7	ERR_MT*	Multiturn Position Error
Note	* Error is latched until Reset or Preset command.	

Table 41: Error Status Register

ERR_CFG = 1 indicates that the configuration data checksum (CRC_CFG) does not match the checksum of the current configuration registers in RAM. Refer to STARTUP AND OPERATION on page 57 for more information.

ERR_OFFS = 1 indicates that the position offset data checksum (CRC_OFFS) does not match the checksum of the current position offset registers in RAM. Refer to STARTUP AND OPERATION on page 57 for more information.

ERR_POS = 1 indicates that an attempt was made to read the current position during startup or a position preset sequence when the current position is not yet known.

ERR_EXT = 1 indicates that the NERR pin has been pulled low by an external device.

ERR_AMIN = 1 indicates that the Hall signal amplitude is too low. Refer to SIGNAL CONDITIONING on page 18 for more information.

ERR_AMAX = 1 indicates that the Hall signal amplitude is too high. Refer to SIGNAL CONDITIONING on page 18 for more information.

ERR_MTI = 1 indicates a problem in the multiturn interface. Refer to MULTITURN INTERFACE on page 23 for more information.

ERR_MT = 1 indicates that the multiturn count read over the multiturn interface does not match the current value of the iC-MHM's multiturn counter. Refer to MULTITURN INTERFACE on page 23 for more information.

When any of the error bits are set, the error output is activated (pin NERR low), and the error bit in the BiSS SCD, SPI position read command response, and extended SSI frame are also activated (nERR = nE = 0).

Digital I/O Pin States

The digital I/O pin states indicates the pin level of the four general-purpose pins (in any case if input or output).

State	Address 0x71	
Bit	Name	Description
0	S_IO0	MDI: 0 = Low and 1 = High Level
1	S_IO1	P1: 0 = Low and 1 = High Level
2	S_IO2	P2: 0 = Low and 1 = High Level
3	S_IO3	P3: 0 = Low and 1 = High Level
4	-	Reserved
5	-	Reserved
6	-	Reserved
7	-	Reserved

Table 42: Digital I/O Pin States

Refer to DIGITAL I/O PORT on page 26 for more information on configuring the port as general-purpose discrete inputs.

GAIN

The Gain Status Register contains the current gain values used by the Hall sensor signal amplifiers.

Gain	Address 0x72	
Bits	Name	Description
5:0	GAINF	Current Fine Gain
7:6	GAINR	Current Coarse Gain Range

Table 43: Gain Status Register

Refer to SIGNAL CONDITIONING on page 18 for more information on GAINR and GAINF.

Chip Release (CHIP_REL)

The chip release status register contains a value which indicates the iC-MHM chip release (revision).

CHIP_REL	Address 0x73
Value	Chip release
n/a	iC-MHM Release X2
0x35	iC-MHM Release X5

Table 44: Chip Release Status Register

The CHIP_REL value is undefined for chip releases prior to X5.

INSTRUCTION REGISTERS

The iC-MHM provides three instruction registers which are used to initiate a position preset sequence, reset the device, set the state of the general-purpose discrete outputs (when configured), and set the gain values for the Hall signal amplifiers when the automatic amplitude control is not used.

Reset and Preset

Bits in this register allow initiating a position preset sequence or resetting the iC-MHM.

Reset and Preset	Address 0x74	
Bit	Name	Description
0	RESET	Device Reset
1	PRESET	Initiate Absolute Position Preset
2	-	Reserved
3	-	Reserved
4	-	Reserved
5	-	Reserved
6	-	Reserved
7	-	Reserved

Table 45: Reset, Preset Instruction Register

The reset instruction resets the device, but does not read the configuration data from the EEPROM (if connected). Refer to STARTUP AND OPERATION on page 57 for more information.

Refer to POSITION OFFSET AND PRESET (Zero Position) on page 55 for more information on the position preset sequence.

Writing to the reset and preset instruction register via BiSS can be blocked to prevent the reset and preset instructions from being executed.

INSPROT	Addr. 0x0B; bit 1
Value	Protection
0	Reset and Preset Not Protected (Writing using BiSS allowed)
1	Reset and Preset Protected (Writing using BiSS is not allowed)

Table 46: Instruction Register Protection

Discrete Output

The discrete output instruction register allows changing the state (output level) of the four general-purpose discrete outputs (when configured).

Output	Address 0x75	
Bit	Name	Description
0	F_IO0	MCL: 0 = Low and 1 = High Level
1	F_IO1	P1: 0 = Low and 1 = High Level
2	F_IO2	P2: 0 = Low and 1 = High Level
3	F_IO3	P3: 0 = Low and 1 = High Level
4	-	Reserved
5	-	Reserved
6	-	Reserved
7	-	Reserved
Note	All registers will be reset at power-on.	

Table 47: Discrete Output Instruction Register

Refer to DIGITAL I/O PORT on page 26 for more information on configuring the port as general-purpose discrete outputs.

Gain

The gain instruction register allows setting the gain values used by the Hall sensor signal amplifiers when the automatic amplitude control is not used (ENAC = 0). The gain values can be read out when the automatic amplitude control is used (ENAC = 1).

Gain	Address 0x76	
Bits	Name	Description
5:0	GAINF	Fine Gain
7:6	GAINR	Coarse Gain Range

Table 48: Hall Sensor Signal Amplifier Gain

Refer to SIGNAL CONDITIONING on page 18 for more information on GAINR and GAINF.

TEST MODE

Test Mode (TEST)
Test mode is used to measure the internal bandgap and reference voltages, and to set the bias current.

TEST	Address 0x07; bits 4:0
Value	Description
0x00	Normal Operation
0x01 ... 0x18	Reserved (Do not use)
0x19	Test Mode
0x1A ... 0x1F	Reserved (Do not use)

Table 49: Test Mode

In Test Mode (TEST = 0x19), the internal bandgap voltage is output on PCOS (pin 18), the internal reference voltage used for signal conditioning is output on PSIN (pin 4), and the internal bias current can be measured at NSIN (pin 3).

Refer to Elec. Char. item no. 401- 403 for more information on the voltage and current ranges. Refer to CALIBRATION on page 54 for more information on setting the bias current.

EEPROM AND I^{2}C INTERFACE (Multi-master)

The iC-MHM contains a dedicated I^{2}C interface (pins SCL and SDA) for use with an external serial EEPROM. This EEPROM is typically used in stand-alone applications for storage of configuration data (parameter values). The interface is multi-master, allowing the same EEPROM to be accessed by an external multiturn sensor (such as iC-PV or iC-MV) for storage of its own configuration data.

The external EEPROM is only accessible by the iC-MHM via the BiSS interface. In stand-alone applications using SSI or incremental outputs, the iC-MHM must be configured using BiSS and the parameter values stored in the EEPROM. Refer to SERIAL INTERFACE: BiSS Mode on page 37 and CONFIGURATION on page 52 for more information.

In embedded applications, the iC-MHM is typically configured using the SPI interface and parameter value storage is handled by the SPI master (host processor or microcontroller). Refer to SERIAL INTERFACE: SPI Mode on page 46 and CONFIGURATION on page 52 for more information. An external EEPROM connected to the iC-MHM's I^{2}C interface cannot be accessed using SPI.

Basic interface features

I2C Master Performance	
Protocol	Standard I^{2}C
Clock Rate (Output)	100 kHz max. (refer to Elec. Char. 714)
Addressing	11 bit: 8 bit register address plus 3 bit block selection
Multi-Master Capability	Yes

Table 50: I^{2}C interface performance

The I^{2}C master of iC-MHM addresses I^{2}C devices using an 8-bit register address plus 3 block selection bits as part of the I^{2}C slave address.

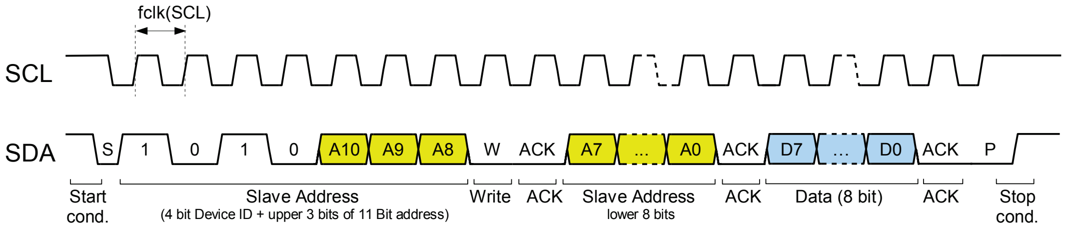

Figure 18: I^{2}C slave addressing for writing a single byte to the EEPROM.

If addressing a memory of 1 Kbit or 2 Kbit, the block selections bits are zero and thus the I^{2}C device address is 0x50 (for '1010 000' without the R/W bit), or 0xA0 respectively (for '1010 0000' with the R/W bit as zero).

EEPROM device requirements

EEPROM Device Requirements	
Supply Voltage	3.3 V to 5.5 V (respectively according to VDD)
Power-On Threshold	< 3.3 V (due to Elec.Char. 404)
Addressing	11 bit address max.
Device Address	0x50 ('1010 000' w/o R/W bit), 0xA0 ('1010 0000' with R/W = 0)
Page Buffer	Not required
Size Min.	1 Kbit (128x8 bit), type 24C01, for configuration data
Size Max.	16 Kbit (8x 256x8 bit), type 24C16 Size limited due to 11-bit slave addressing.

Table 51: EEPROM Device Requirements

It is not relevant if the EEPROM's internal page buffer is 8 or 16 bytes. EEPROMs beyond 16 Kbit can not be used as those require a 2 byte address.

ATTENTION: EEPROMs that ignore the block select or upper address bits in the control byte (such as the Microchip 24AA0x/24LC0xB) should not be used with the iC-MHM.
With these devices, writing to an address beyond the capacity of the EEPROM will overwrite stored iC-MHM configuration data.
EEPROMs that use the address pins as additional enable bits (such as the STMicroelectronics M24Cxx) should be used instead.
To avoid this problem altogether, use of a 16 Kbit EEPROM (which requires all 11 address bits) is recommended and also provides additional space for storage of OEM data.

ATTENTION: If further I^{2}C slave devices are operated on the same bus, higher device addresses may be occupied.

In stand-alone applications, configuration data for both the iC-MHM and external multiturn devices are stored in the EEPROM and protected by checksums.

Address Range	Description
0x00 ... 0x0F	Multiturn Configuration Data
0x10 ... 0x1B	iC-MHM Configuration Data
0x1C	iC-MHM Configuration Checksum
0x1D ... 0x22	iC-MHM Offset Data
0x23	iC-MHM Offset Checksum
0x24 ... 0x3F	Reserved (Must Be Zero)

Table 52: EEPROM Configuration Data Storage

Configuration data for an external multiturn device (such as iC-PV or iC-MV) is stored in EEPROM locations 0x00 - 0x0F. Refer to the datasheet of the appropriate device for details.

iC-MHM configuration data in RAM addresses 0x00 - 0x0C is stored in EEPROM locations 0x10 - 0x1C. This data includes the checksum stored at address 0x0C. Refer to REGISTER MAP: RAM on page 16 for more information.

iC-MHM absolute position offset values stored in RAM addresses 0x0D - 0x13 are stored in EEPROM locations 0x1D - 0x23. This data includes the checksum stored at address 0x23. Refer to REGISTER MAP: RAM on page 16 for more information.

At power up, the iC-MHM configuration in EEPROM addresses 0x10 - 0x23 is copied onto iC-MHM RAM addresses 0x00 - 0x13.

EEPROM addresses above 0x3F are used by the BiSS interface for storage of the position preset value and user data. Refer to SERIAL INTERFACE: BiSS Mode on page 37 for more information. The complete register layout of the EEPROM is shown in REGISTER MAP: EEPROM on page 35.

When writing to the EEPROM, a wait time of at least 4 ms must be allowed after each write. Alternatively, the same byte can be read back after it is written and the values compared. This comparison will fail if the EEPROM is busy with its internal write procedure. Several attempts may be required for the read value to equal the written value before the next location can be written.

REGISTER MAP: EEPROM

OVERVIEW								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Configuration (Bank 1)								
0x000 ... 0x00F	External Multiturn Sensor Configuration Data (iC-MV, iC-PV, etc.)							
0x010 ... 0x01C	iC-MHM Configuration Data							
0x01D ... 0x023	iC-MHM Offset Data							
0x024 ... 0x03F	Reserved (must be 0x00)							
BiSS Defined Standard Register								
0x040	Unused							
0x041	BiSS EDS Bank (EDSBANK)							
0x042 0x043	BiSS Profile ID (PRO_ID)							
0x044 ... 0x047	BiSS Device Serial Number (SER_NO)							
Output Values After Preset (Zero Position)								
0x048	PSET_MT(31:24)							
0x049	PSET_MT(23:16)							
0x04A	PSET_MT(15:8)							
0x04B	PSET_MT(7:0)							
0x04C	PSET_ST(15:8)							
0x04D	PSET_ST(7:0)							
0x04E	CRC_PSET(7:0)							
0x04F	Reserved (must be 0x00)							
User Data								
0x050 ... 0x06F	User Data							
0x070 ... 0x077	Unused							
BiSS Identifier								
0x078 ... 0x07D	BiSS Device Identifier (DEV_ID)							
0x07E ... 0x07F	BiSS Device Manufacturer Identifier (MFG_ID)							
Bank 2 - 13								
0x080 ... 0x37F	EDS							
Bank 14 - 31								
0x380 ... 0x7FF	USER							

Table 53: Register layout

SERIAL INTERFACE: General

The iC-MHM contains a serial interface that can be configured to use differential RS422, single-ended TTL, or LVDS (Low Voltage Differential Signaling) signal levels as shown in Table 54.

RTX_MODE	Addr. 0x03; bit 4:3	
Value	Input Levels	Output Levels
0	TTL (Single-ended)	RS422 (Differential)
1	TTL (Single-ended)	TTL (Single-ended)
2	LVDS (Differential)	LVDS (Differential)
3	RS422 (Differential)	RS422 (Differential)

Table 54: Serial Interface Configuration

TTL I/O is single-ended. This means that if RTX_MODE = 0, pins NMA and NSLI are not used and should be left unconnected. If RTX_MODE = 1, pins NMAO, NMA, NSLI, and NSLO are not used and should be left unconnected. LVDS and RS422 I/O are differential and thus all serial interface pins are used.

With TTL level inputs (RTX_MODE = 0 or 1), the slave input (pin SLI) has an internal pull-down resistor of 50 kΩ (Elec. Char. item no. 902). An external pull-down resistor (R1) with a value between 10 kΩ and 50 kΩ, as shown in Figure 19, may be necessary in noisy environments.

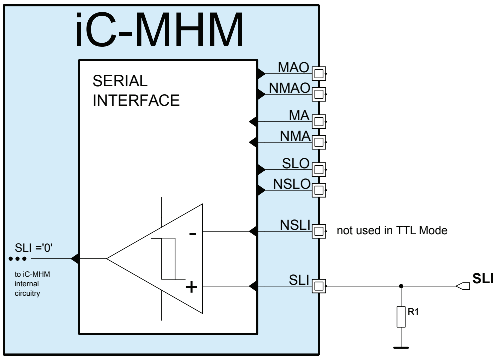

Figure 19: Optional External Pull-down Resistor for TTL Input Levels

With RS422 inputs (RTX_MODE = 3, the slave inputs (pins SLI and NSLI) require external biasing resistors as shown in Figure 20.

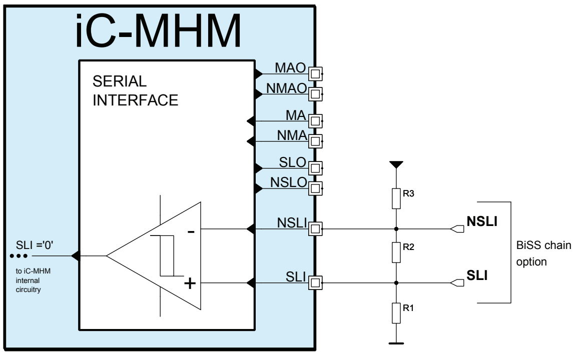

Figure 20: Required External Biasing for RS422 Input Levels

In general, $R1 = R3 \leq (0.5 * R2 * (VDD/Vt()diff - 1))$.

For example, if VDD = 4.5 V (worst case) and Vt()diff = 300 mV (Elec. Char. item no. 929), and R2 = 120 Ω, then $R1 = R3 \leq 840\Omega$.

If an error occurs during startup, the serial interface configuration defaults to TTL inputs and RS422 outputs (RTX_MODE = 0). Refer to STARTUP AND OPERATION on page 57 for more information.

The required configuration for SPI communication with the iC-Haus MB3U-I^2C Adapter is TTL inputs (RTX_MODE = 0 or 1).

The serial interface must be configured to use the BiSS, SSI, or SPI protocol as detailed in the following sections.

SERIAL INTERFACE: BiSS Mode

The BiSS interface is an open-source differential, serial, bidirectional communications interface used for absolute position and configuration data transmission. In BiSS mode, the iC-MHM is a BiSS slave and must be connected to a BiSS master for proper operation. For a detailed description of the BiSS Interface, please refer to www.biss-interface.com.
The serial interface is configured for BiSS mode by disabling SSI mode ENSSI = 0 and requires
DISBiSS = 0.

ENSSI	Address 0x03; bit 7
Value	Serial Mode
0	BiSS C
1	SSI

Table 55: BiSS/SSI Protocol Selection

DISBISS	Addr. 0x07; bit 5
Value	Description
0	BiSS Enabled MISO (SLO) Driven High When NCS Inactive
1	BiSS Disabled MISO (SLO) in Tristate (High Z) When NCS Inactive

Table 56: Disable BiSS Interface

The BiSS serial protocol used by the iC-MHM is shown in Figure 21.

After every BiSS cycle, the integrity of the configuration and offset data is verified using a CRC. If either CRC fails, the appropriate error bit in the error status register is set, the error output is activated (pin NERR low), and the BiSS error bit is activated (nERR = 0) for the next cycle. Refer to STATUS REGISTERS on page 30 for more information.

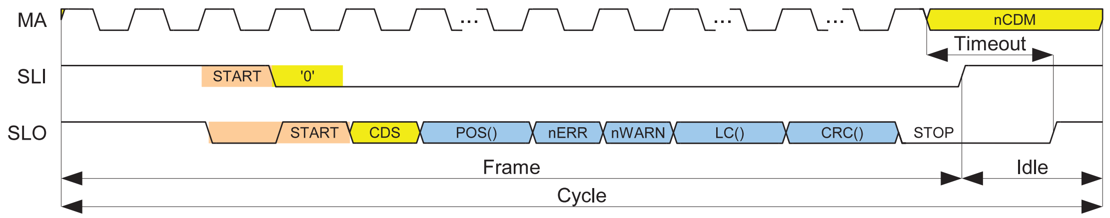

Figure 21: BiSS Protocol

BiSS Single Cycle Data (SCD)

The Single Cycle Data (SCD) produced by the iC-MHM, shown in blue in Figure 21, contains the multiturn position (turns count) followed by the singleturn position (magnet angle), an error bit, a warning bit, an optional sign-of-life counter value, and a CRC value. All values are transmitted MSB first in the order shown in Table 57.

Single Cycle Data (SCD)	
Bit Length	Description
0 - 32	Multiturn Position (Turns Count - OFFS_MT)
12 or 16	Singleturn Position (Magnet Angle - OFFS_ST)
1	Error Bit nERR (Active Low)
1	Warning Bit nWARN (Active Low)
0 or 6	Optional Sign-of-Life Counter (BiSS SCD Cycle Count)
6 or 16	CRC Polynomial (Inverted)

Table 57: iC-MHM BiSS Single Cycle Data

Refer to POSITION OFFSET AND PRESET (Zero Position) on page 55 for more information on the position offset parameters OFFS_MT and OFFS_ST.

The bit length of the multiturn count in the BiSS SCD is set using parameter MT12.

MT12	Address 0x03; bit 2	
Value	Multiturn Bit Length	Conditions
0	As Defined by RESO_MT	
1	0	RESO_MT = 0
1	12	RESO_MT = 1, 2, or 3
1	24	RESO_MT = 4, 5, or 6
1	32	RESO_MT = 7

Table 58: Multiturn Bit Length

When using BiSS Encoder Profile BP3, set MT12 = 0. In this case, the multiturn count bit length is set by parameter RESO_MT. Refer to MULTITURN INTERFACE on page 23 for more information on RESO_MT.

When using BiSS Encoder Profile BP1, set MT12 = 1. In this case, the multiturn position bit length still depends on RESO_MT, but is always fixed at 0, 12, 24, or 32. If the multiturn resolution (in bits) is less than one of these values, the multiturn count value is right-justified in the multiturn count field and the unused MSBs are set to zero.

For example, if RESO_MT = 5, the multiturn count is a 20-bit value in a 24-bit field. In this case, bits 19:0 contain the multiturn count while bits 23:20 are zero. Refer to MULTITURN INTERFACE on page 23 for more information on RESO_MT.

The singleturn position bit length depends on the interpolator resolution as set by parameter RESO_ST, but is always fixed at 12 or 16 bits. If the singleturn resolution (in bits) is less than one of these values, the singleturn position value is left-justified in the singleturn position field and the unused LSBs are set to zero.

For example, if RESO_ST = 6, the singleturn position (angle) is a 10-bit value in a 12-bit field. In this case, bits 11:2 contain the singleturn position while bits 1:0 are zero. Refer to INTERPOLATOR on page 21 for more information on RESO_ST.

The active-low BiSS error bit, nERR, is activated when any of the error bits in the error status register is active. Refer to STATUS REGISTERS on page 30 for more information.

The active-low BiSS warning bit, nWARN, is activated if magnet rotation speed is excessive. Refer to INTERPOLATOR on page 21 for more information on maximum rotation speeds.

In safety applications, a sign-of-life counter (life counter) value can be transmitted after the BiSS warning bit in the SCD.

ENLC	Address 0x0A; bit 6	
Value	CRC HEX Code	Description
0	0x43	Sign-of-Life Counter Disabled. CRC Polynomial: $X^6 + X^1 + X^0$
1	0x190D9	16-Bit Sign-of-Life Counter Value. CRC Polynomial: $X^{16} + X^{15} + X^{12} + X^7 + X^6 + X^4 + X^3 + X^0$

Table 59: Sign-of-Life Counter Enable

If the sign-of-life counter is enabled (ENLC = 1), a 6-bit count value (0 - 63) is transmitted last in the SCD. Its reset value of zero is never output as it is bypassed during normal operation.

LC	
Code	Value
0x00	Initial value after power-on, reset and preset
0x01	Value on first request for new position data and follow-up value on the maximum
...	...
0x3F	Max. value

Table 60: Sign-of-life counter

The count value is incremented after each new BiSS cycle. If the sign-of-life counter is disabled (ENLC = 0), no additional bits are transmitted and the CRC code immediately follows the nWARN bit in the SCD.

The Cyclic Redundancy Check value (CRC) is transmitted in its inverted state last in the SCD. If the sign-of-life counter is disabled (ENLC = 0) a 6-bit CRC code is transmitted; if the sign-of-life counter is enabled (ENLC = 1), a 16-bit CRC value is transmitted.

The starting value of the checksum calculation is determined by CRCS. The CRC is calculated using the selected CRC start value and the polynomial shown in Table 59 based on ENLC.

CRCS	Address 0x0A; bits 5:0
Value	Function
0x00	Default CRC Start Value (BiSS Encoder Profile BP1 and BP3)
0x01 ... 0x3F	Unique CRC Start Value Used By All Slaves on the BiSS Channel

Table 61: CRC Start Value

Adaptive Timeout

The iC-MHM can provide a fixed or adaptive BiSS timeout depending on the setting of parameter NTOA. For fastest communication speed, it is recommended to use the adaptive timeout.

NTOA	Address 0x07; bit 6
Value	Description
0	Adaptive Timeout
1	Fixed Timeout

Table 62: Adaptive Timeout

If NTOA = 1, a fixed nominal timeout of 20 µs (with a 14 MHz system clock) is used (refer to Elec. Char. item no. 501 and 904).

If NTOA = 0, the iC-MHM adapts the BiSS timeout length based on the period of the BiSS MA clock, T_{MA}, and its internal sampling frequency, $1/T_{CLK}$, to ensure fastest communication. In operation, the iC-MHM measures 1.5 periods of MA (from the first falling to the second rising edge) of each BiSS frame and calculates an adaptive timeout value of

$$T_{\mathrm{CLK}} = \frac{4}{3 \ast fsys}$$

Where fsys is the system clock frequency (refer to Elec. Char. item no. 501 and 904).

Timeout	Condition	Min.	Max.
t_{out}	$T_{CLK} \leq 1.5 \ast T_{MA}$	$1.5 \ast T_{MA}$	$1.5 \ast T_{MA} + 3.0 \ast T_{CLK}$
	$T_{CLK} \geq 1.5 \ast T_{MA}$	$1.0 \ast T_{CLK}$	$1.5 \ast T_{MA} + 3.0 \ast T_{CLK}$

Table 63: Adaptive Adaptive Timeout Calculations

For more information on the BiSS adaptive timeout, refer to BiSS application note AN23 at www.biss-interface.com.

BiSS Control Communication

The control Communication uses the CDM and CDS bits of several consecutives BiSS frames for protected reading and writing of the register of a slave and the protected and confirmed sending of commands to selected or all slaves. The CDS bit is transmitted after the start bit at SLO and the CDM is transmitted as the inverse of the MA level during the BiSS timeout.

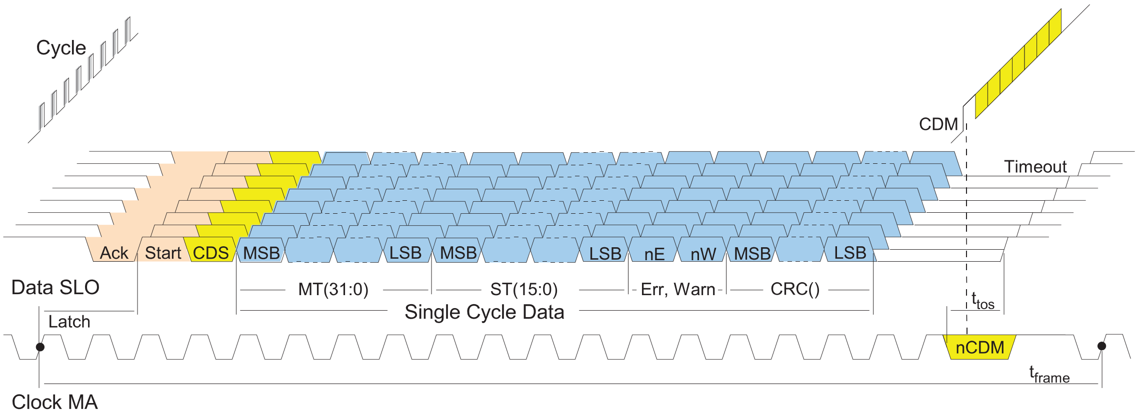

Figure 22: BiSS Protocol Showing Control Communication

The iC-MHM implements various BiSS commands.

BiSS Commands			
CMD	Broadcast	Addressed	Condition
0	Deactivate SCD	Activate SCD	ENCMD01 = 1
1	Activate Control Communication	Deactivate Control Communication	ENCMD01 = 1
2	BiSS Discrete Output Low	BiSS Discrete Output High	ENCMD2 = 1
3	n.a.	Preset	ENCMD3 = 1

Table 64: BiSS Commands

The BiSS commands 0 and 1 are required for bus establishment and can be enabled with ENCMD01 = 1.

ENCMD01	Addr. 0x0B; bit 6
Value	Function
0	BiSS Commands 0 and 1 disabled
1	BiSS Commands 0 and 1 enabled

Table 65: BiSS Command 01 Enable

If P3 is configured as a BiSS command controlled output (CFG_IOP = 0 and ENCMD2 = 1), an addressed BiSS command with CMD = 2 sets P3 high. A BiSS broadcast command with CMD = 2 resets P3 low.

If the MCL output is configured as a BiSS command controlled output (SBL_MTI = 0, CFG_IOP = 2 or 3, and ENCMD2 = 1, an addressed BiSS command with CMD = 2 sets MCL high. A BiSS broadcast command with CMD = 2 resets MCL low.

Refer to DIGITAL I/O PORT on page 26 for more information on defining the BiSS command controlled output.

ENCMD2	Addr. 0x0B; bit 5
Value	Function
	Conditions: CFG_IOP = 0
0	P3 is General-Purpose Discrete I/O
1	P3 is BiSS Command Controlled Output
	Conditions: CFG_IOP = 2 or 3, SBL_MTI = 0
0	MCL is General-Purpose Discrete I/O
1	MCL is BiSS Command Controlled Output

Table 66: BiSS Command 2 Enable: Controlling Pins P3 and MCL

An addressed BiSS command with CMD = 2 sets pin 7 high. A BiSS broadcast command with CMD = 2 resets pin 7 low. Refer to SERIAL INTERFACE: BiSS MODE on page 37 for more information.

A BiSS addressed command with CMD = 3 can be configured to initiate a position preset sequence using parameter ENCMD3.

ENCMD3	Address 0x08; bit 4
Value	Function
0	BiSS Command 3 Disabled
1	BiSS Command 3 Enabled

Table 67: BiSS Command 3 Enable

If ENCMD3 = 1, a BiSS addressed command with CMD = 3 initiates a position preset sequence. Refer to POSITION OFFSET and PRESET (Zero Position) on page 55 for more information.

BiSS access to certain registers in the iC-MHM RAM and its external EEPROM can be restricted using parameters REGPROT and INSPROT.

REGPROT	Addr. 0x0B; bit 0
Value	Protection
0	Disabled (All Registers Accessible)
1	Enabled (Refer to Table 70)

Table 68: BiSS Register Protection

INSPROT	Addr. 0x0B; bit 1
Value	Protection
0	Reset and Preset Not Protected (Writing using BiSS allowed)
1	Reset and Preset Protected (Writing using BiSS is not allowed)

Table 69: Instruction Register Protection

BiSS Register Address, Content, and Protection					
BANK Number	RAM Address	Register Content	EEPROM Address	REGPROT	
				0	1
0	0x00 - 0x13	iC-MHM Configuration	RAM Only	R/W	None
	0x14 - 0x3F	Not Available		None	None
1	0x00 - 0x0F	MT Device Config.	0x000 - 0x00F	R/W	None
	0x10 - 0x23	iC-MHM Configuration	0x010 - 0x023	R/W	None
	0x24 - 0x3F	Reserved	0x024 - 0x03F	R/W	None
2 - 13	0x00 - 0x3F	EDS	0x080 - 0x37F	R/W	R
14 - 31	0x00 - 0x3F	USER	0x380 - 0x7FF	R/W	R/W
X	0x40	Bank Selection	Unused	R/W	R/W
	0x41	EDS Bank	0x041	R/W	R
	0x42 - 0x43	BiSS Profile ID	0x042 - 0x043	R/W	R
	0x44 - 0x47	Serial Number	0x044 - 0x047	R/W	R
	0x48 - 0x4F	Preset	0x048 - 0x04F	R/W	R/W
	0x50 - 0x6F	USER	0x050 - 0x06F	R/W	R/W
	0x70 - 0x73	Status Registers	Unused	R	R
	0x74 - 0x77	Instruction Registers	Unused	W	W
	0x78 - 0x7F	BiSS ID	0x078 - 0x07F	R/W	R
32 - 255	0x00 - 0x3F	I2C Slave	-	R/W	None

Table 70: BiSS Register Address, Content, and Protection

BiSS Register Access
Figure 23 and 24 show the iC-MHM registers that are accessible via BiSS.

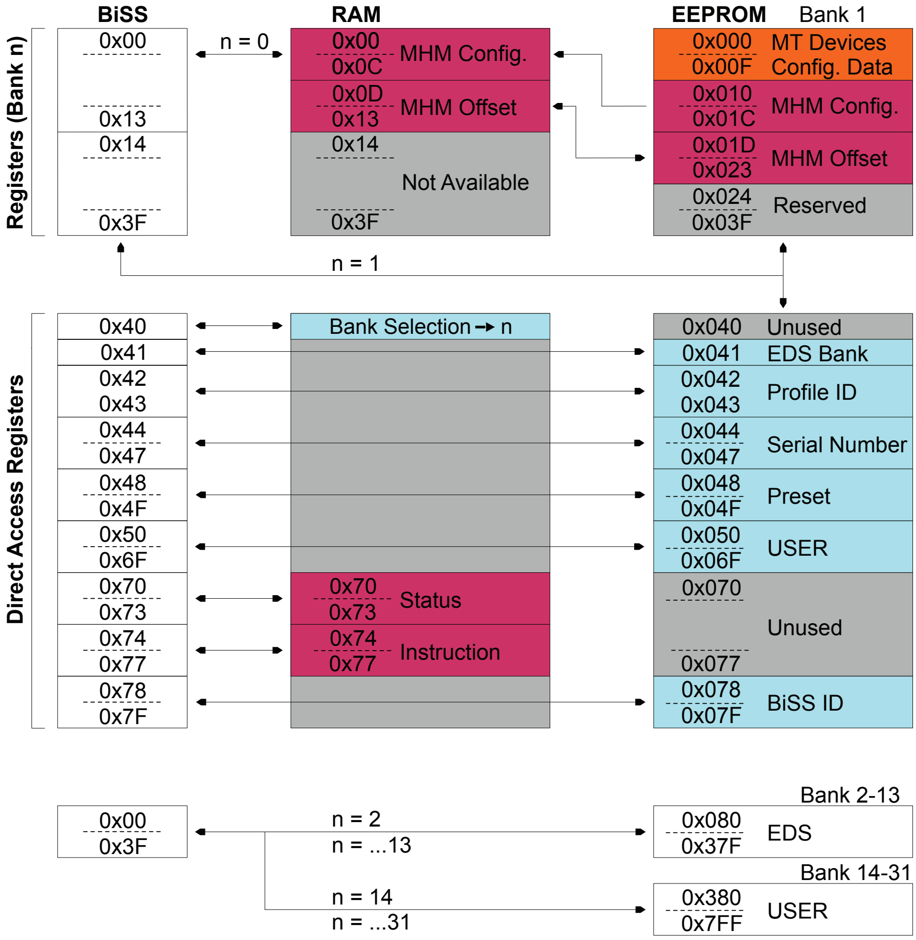

Figure 23: iC-MHM BiSS Registers and Addressing

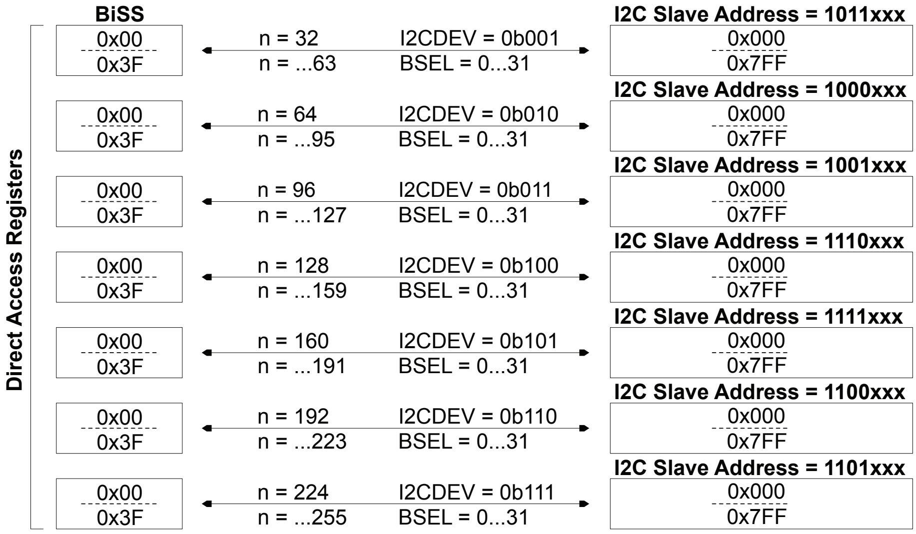

Figure 24: External Devices ID

The BSEL register is used to switch to other memory banks on the external EEPROM. After an iC-MHM power-on, bank 0 is selected, which mirrors the internal registers of iC-MHM. If BSEL points at a higher memory bank, the addresses 0x00 - 0x3F are mapped and aim at higher EEPROM registers.

BSEL	Addr. 0x40; bit 4...0	R/W
Code	Hex	Memory bank addressed by BiSS Addr(5:0): 0x00...0x3F
00000	0x0	Bank 0*
00001	0x1	Bank 1*
00010	0x2	Bank 2
...	...	...
11111	0x1F	Bank 31
Note	*) If I2CDEV = 0b000, refer to the defined BiSS mapping shown in Figure 23.	

Table 71: Bank Selection

I2CDEV	Addr. 0x40; bit 7...5	R/W
Code	I^{2}C Slave Address*	Device ID
	Bank 0 to 31:	
000	0b 1010 xxxxx xxxxxx	0x50, 0xA0 for EEPROM refer to Table 51
	Bank 32 to 255:	
001	0b 1011 xxx xx xxxxxx	
010	0b 1000 xxx xx xxxxxx	
011	0b 1001 xxx xx xxxxxx	
100	0b 1110 xxx xx xxxxxx	
101	0b 1111 xxx xx xxxxxx	
110	0b 1100 xxx xx xxxxxx	0x61, 0xC2 for iC-PVL
111	0b 1101 xxx xx xxxxxx	
Note	*) Device ID (4 bit) plus register address (11 bit): xxx xx is represented by BSEL(4:0) and xxxxxx by BiSS Addr(5:0).	

Table 72: I^{2}C Device ID

SERIAL INTERFACE: SSI Mode

The SSI interface is an industry-standard differential serial communications interface used for absolute position transmission.

The serial interface is configured for SSI mode by enabling SSI mode (ENSSI = 1) and requires DISBiSS = 0.

ENSSI	Address 0x03; bit 7
Value	Serial Mode
0	BiSS C
1	SSI

Table 73: BiSS/SSI Protocol Selection

DISBISS	Addr. 0x07; bit 5
Value	Description
0	BiSS Enabled MISO (SLO) Driven High When NCS Inactive
1	BiSS Disabled MISO (SLO) in Tristate (High Z) When NCS Inactive

Table 74: Disable BiSS Interface

In SSI mode (standard or extended), absolute position (multiturn count plus singleturn position) may be transmitted in either natural binary or Gray code depending on parameter BIN_SSI.

BIN_SSI	Address 0x03; bit 5
Value	Numeric Format
0x0	Gray Code
0x1	Natural Binary

Table 75: SSI Numeric Format

Absolute position values are always transmitted MSB first regardless of the numeric format.

The bit length of the multiturn count in is set using parameter MT12.

MT12	Address 0x03; bit 2	
Value	Multiturn Bit Length	Conditions
0	As Defined by RESO_MT	
1	0	RESO_MT = 0
1	12	RESO_MT = 1, 2, or 3
1	24	RESO_MT = 4, 5, or 6
1	32	RESO_MT = 7

Table 76: Multiturn Bit Length

If MT12 = 0, the multiturn bit length is set by parameter RESO_MT. Refer to MULTITURN INTERFACE on page 23 for more information on RESO_MT.

If MT12 = 1, the multiturn bit length still depends on RESO_MT, but is always fixed at 0, 12, 24, or 32. If the multiturn resolution (in bits) is less than one of these values, the multiturn count value is right-justified in the multiturn field and the unused MSBs are set to zero.

For example, if RESO_MT = 5, the multiturn count is a 20-bit value in a 24-bit field. In this case, bits 19:0 contain the multiturn count while bits 23:20 are zero. Refer to MULTITURN INTERFACE on page 23 for more information on RESO_MT.

The iC-MHM can provide a fixed or adaptive timeout depending on the setting of parameter NTOA.

NTOA	Address 0x07; bit 6
Value	Description
0	Adaptive Timeout (not recommended in SSI mode)
1	Fixed Timeout

Table 77: Adaptive Timeout

If NTOA = 1, a fixed nominal timeout of 20 µs (with a 14 MHz system clock) is used (refer to Elec. Char. item no. 501 and 904). Use of an adaptive timeout in SSI mode is not recommended.

The SSI interface can also operate in ring mode by connecting SLO on the last slave in the SSI chain to SLI on the first slave. This causes each SSI frame to be transmitted twice. By checking the repeated position data for equality, transmission errors can be detected.

After every SSI cycle, the integrity of the configuration and offset data is verified using a CRC. If either CRC fails, the appropriate error bit in the error status register is set, the error output is activated (pin NERR low), and the extended SSI protocol error bit is activated (nE = 0) for the next cycle. Refer to STATUS REGISTERS on page 30 for more information.

In SSI mode, one of two protocols, standard or extended, may be selected using parameter EXT_SSI.

EXT_SSI	Address 0x03; bit 6
Value	Protocol
0	Standard SSI Protocol
1	Extended SSI Protocol

Table 78: SSI Protocol

Standard SSI protocol transmits only multiturn count and singleturn position. In addition, the singleturn resolution is limited to 13 bits or less.

Extended SSI protocol transmits multiturn count, singleturn position at any resolution, error and warning bits, and an optional sign-of-life counter value.

Standard SSI Protocol

Standard SSI protocol (ENSSI = 1 and EXT_SSI = 0) provides selectable multiturn bit lengths and fixed 13-bit singleturn bit length.

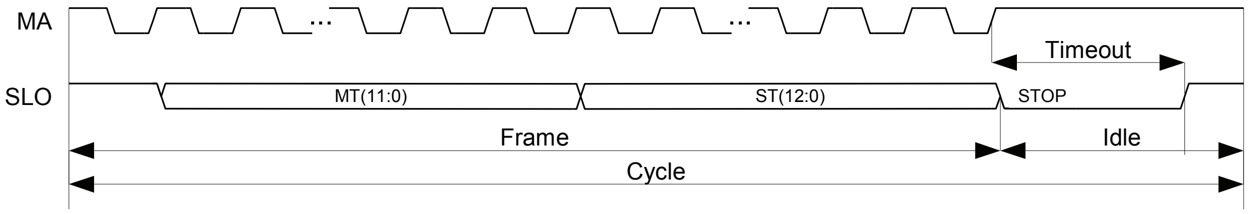

Figure 25: Standard SSI Protocol

The multiturn count (MT) is transmitted first, followed by the 13-bit singleturn position (ST) and a timeout. All values are transmitted MSB first in the order shown in Table 79.

Standard SSI Protocol Frame	
Bit Length	Description
0 - 32	Multiturn Position (Turns Count - OFFS_MT)
13	Singleturn Position (Magnet Angle - OFFS_ST)

Table 79: Standard SSI Protocol Frame

Refer to POSITION OFFSET AND PRESET (Zero Position) on page 55 for more information on the position offset parameters OFFS_MT and OFFS_ST.

A constant high level on SLO indicates that one or more of the error bits in the error status register is active. Refer to STATUS REGISTERS on page 30 for more information.

The singleturn bit length is fixed at 13, but the singleturn resolution depends on the interpolator resolution as set by parameter RESO_ST. If the singleturn resolution (in bits) is less than 13, the singleturn position value is left-justified in the singleturn position field and the unused LSBs are set to zero.

For example, if RESO_ST = 6, the singleturn position (angle) is a 10-bit value in a 13-bit field. In this case, bits 12:3 contain the singleturn position while bits 2:0 are zero.

Singleturn resolutions greater than 13 bits (RESO_ST < 3) may not be used in standard SSI mode. Refer to INTERPOLATOR on page 21 for more information on RESO_ST.

Extended SSI Protocol

Extended SSI protocol (ENSSI = 1 and EXT_SSI = 1) provides selectable multiturn bit length, selectable singleturn bit length, error and warning bits, and an optional sign-of-life counter value.

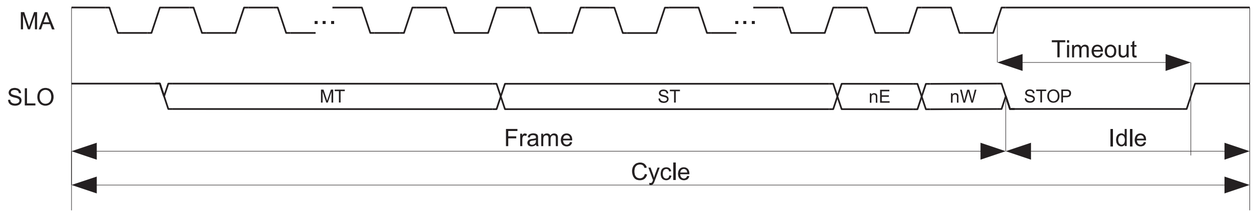

Figure 26: Extended SSI Protocol

The multiturn count (MT) is transmitted first, followed by the singleturn position (ST), an error bit, a warning bit, and an optional sign-of-life counter value. All values are transmitted MSB first in the order shown in Table 80.

Extended SSI Protocol Frame	
Bit Length	Description
0 - 32	Multiturn Position (Turns Count - OFFS_MT)
12 or 16	Singleturn Position (Magnet Angle - OFFS_ST)
1	Error Bit nE (Active Low)
1	Warning Bit nW (Active Low)
0 or 6	Optional Sign-of-Life Counter (SSI Cycle Count)

Table 80: Extended SSI Protocol Frame

Refer to POSITION OFFSET AND PRESET (Zero Position) on page 55 for more information on the position offset parameters OFFS_MT and OFFS_ST.

The singleturn bit length depends on the interpolator resolution as set by parameter RESO_ST, but is always fixed at 12 or 16 bits. If the singleturn resolution (in bits) is less than one of these values, the singleturn position value is left-justified in the singleturn position field and the unused LSBs are set to zero.

For example, if RESO_ST = 6, the singleturn position (angle) is a 10-bit value in a 12-bit field. In this case, bits 9:0 contain the singleturn position while bits 11:10 are zero. Refer to INTERPOLATOR on page 21 for more information on RESO_ST.

The active-low error bit, nE, is activated when any of the error bits in the error status register is active. Refer to STATUS REGISTERS on page 30 for more information.

The active-low warning bit, nW, is activated if magnet rotation speed is excessive. Refer to INTERPOLATOR on page 21 for more information on maximum rotation speeds.

In safety applications, a sign-of-life counter (life counter) value can be transmitted after the warning bit in the SSI frame.

ENLC	Address 0x0A; bit 6
Value	Description
0	Sign-of-Life Counter Disabled
1	6-Bit Sign-of-Life Counter Value

Table 81: Sign-of-Life Counter Enable

If the sign-of-life counter is enabled (ENLC = 1), a 6-bit count value (0 - 63) is transmitted last in the SSI frame.

Its reset value of zero is never output as it is bypassed during normal operation.

LC	
Code	Value
0x00	Initial value after power-on, reset and preset
0x01	Value on first request for new position data and follow-up value on the maximum
...	...
0x3F	Max. value

Table 82: Sign-of-life counter

The count value is incremented after each new BiSS cycle. If the sign-of-life counter is disabled (ENLC = 0), no additional bits are transmitted and the CRC code immediately follows the nWARN bit in the SCD.

SERIAL INTERFACE: SPI Mode

General Protocol Description

The SPI interface in the iC-MHM is a SPI slave and supports SPI modes 0 and 3, meaning that the idle state of SCLK (MA) can be 0 or 1. Data is always accepted on the rising edge of SCLK and the idle state of MISO (SLO) is 1. As shown in Figure 27, a falling edge on NCS initiates an SPI transaction causing the MOSI signal (SLI) to be fed through to MISO (SLO). Data is sent byte by byte with the MSB (most significant bit) first.

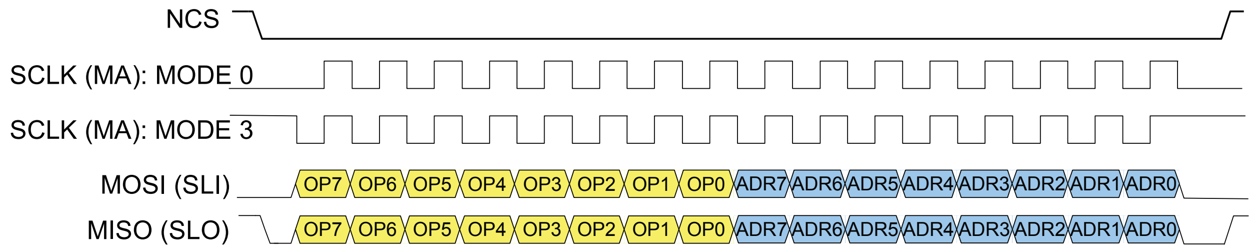

Figure 27: SPI Transmission

When SPI mode is not selected (NCS high), the serial interface is in BiSS or SSI mode (depending on the setting of parameter ENSSI) and MISO is driven high.

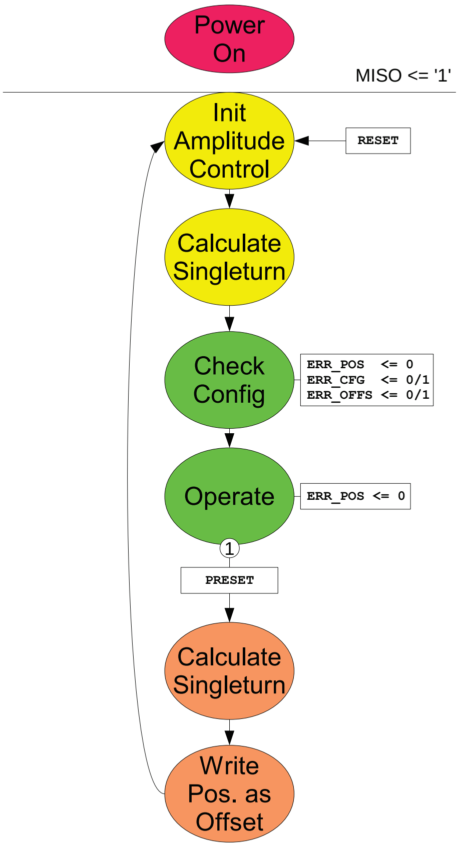

Figure 28: SPI Startup

To prevent any side effects it is recommended to disable BiSS by setting parameter DISBiSS = 1. Further with this configuration MISO is in tristate (high Z) and clock signals on MA are ignored when NCS is not active. This allows bussing multiple iC-MHMs to a single SPI master. Refer to Bussing and Chaining Multiple iC-MHMs on page 50 for more information.

DISBISS	Addr. 0x07; bit 5
Value	Description
0	BiSS Enabled MISO (SLO) Driven High When NCS Inactive
1	BiSS Disabled MISO (SLO) in Tristate (High Z) When NCS Inactive

Table 83: Disable BiSS Interface

Opcodes

Each SPI transaction begins with a 1-byte opcode (operation code or command) sent by the SPI master. As shown in Table 84, the opcode determines whether configuration (register) or sensor (position) data is accessed.

OPCODE	
Code	Description
0xB0	Activate
0xA6	Position Read
0x8A	Register Read (Continuous)
0xCF	Register Write (Continuous)
0x9C	Read Status
0xD9	Write Instruction
0x97	Register Read (Single)
0xD2	Register Write (Single)
0xAD	Read Register Status/Data

Table 84: Operation Codes

These opcodes are explained following.

Activate

The Activate opcode (0xB0) turns the register and sensor data channels in the iC-MHM on and off individually. This command causes the iC-MHM to reset its RACTIVE (register data channel) and PACTIVE (sensor data channel) bits, turning both channels off, and resets the Fail, Valid, Busy, and Dismiss bits in the SPI status byte (refer to Table 90 on page 50). The RACTIVE and PACTIVE bits in the data byte following the opcode then activate one or both channels for subsequent transactions.

RACTIVE	
Code	Description
0	Register communication deactivated
1	Register communication activated*)
Note	*) default after startup

Table 85: RACTIVE

PACTIVE	
Code	Description
0	Sensor data channel deactivated
1	Sensor data channel activated*)
Note	*) default after startup

Table 86: PACTIVE

With only one iC-MHM slave (one register and one sensor data channel), the RACTIVE and PACTIVE bits are bits 1 and 0 respectively in the data byte following the Activate command as shown in Figure 29.

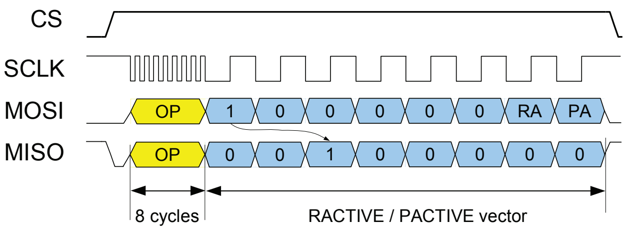

Figure 29: RACTIVE and PACTIVE (one slave)

If RACTIVE = 1, the register data channel is activated and communication with iC-MHM registers is possible. If PACTIVE = 1, the sensor data channel is activated and position (multiturn count and angle) information can be read. Both channels can be active at the same time. After startup, both the register data channel (RACTIVE = 1) and the sensor data channel are enabled (PACTIVE = 1).

Note: It is not possible for the SPI master to read back the state of the RACTIVE or PACTIVE bits to determine which data channels are active in the iC-MHM. It is only possible for it to turn both channels off and then activate each or both as required using the Activate command.

If RACTIVE = 1, the Register Read, Register Write, Register Read (Continuous), Register Write (Continuous), Register Status, Read Status, and Write Instruction commands (opcodes) operate normally, as explained following. If RACTIVE = 0, these commands are not executed and, if attempted, set the error bit in the SPI status byte (Table 90 on page 50).

Likewise, if PACTIVE = 1, the Position Read opcode operates normally, as explained following. If PACTIVE = 0, this command is not executed and, if attempted, sets the error bit in the SPI status byte (Table 90 on page 50). All of these commands, however, are still passed through to MISO.

Position Read

The Position Read command (0xA6) is used to read the absolute position data from the iC-MHM.

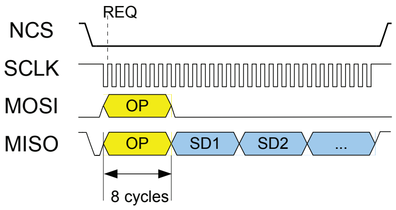

Figure 30: Position Read

As shown in Figure 30, the iC-MHM latches its position data on the first rising edge of SCLK when NCS is low (REQ).

The sensor data channel must be activated (PACTIVE = 1) for proper operation of this command, otherwise the error bit in the SPI status byte is set. If invalid data is detected in the shift register, the error bit in the SPI status byte (Table 90 on page 50) is set.

The Position Read command data contains the multiturn position (turns count) followed by the singleturn position (angle), an error bit, and a warning bit. All values are byte-aligned and transmitted MSB first in the order shown in Table 87.

Position Data Format	
Byte Length	Description
0 - 4	Multiturn Position (Turns Count - OFFS_MT)
2	Singleturn Position (Magnet Angle - OFFS_ST)
1	nERR, nWARN, 000000

Table 87: Position Data Format

Refer to POSITION OFFSET AND PRESET (Zero Position) on page 55 for more information on the position offset parameters OFFS_MT and OFFS_ST.

The number of multiturn bytes in the position data is determined by parameter RESO_MT.

RESO_MT	Address 0x01; bits 2:0	
Value	Resolution (Bits)	Byte Length
0	0	0
1	Not Permissible	-
2	8	1
3	Not Permissible	-
4	16	2
5	Not Permissible	-
6	24	3
7	32	4

Table 88: Multiturn Resolution (SPI)

Only certain multiturn resolutions can by used in SPI mode, as shown above. In all cases, the number of bits supplied by the external multiturn counter must match the RESO_MT value. Refer to MULTITURN INTERFACE on page 23 for more information. If the multiturn counter is not needed, set RESO_MT = 0.

Singleturn position (angle) is always transmitted using two bytes. If the interpolator resolution as set by parameter RESO_ST is less than 16 bits, the singleturn position value is left-justified in the singleturn position field and the unused LSBs are set to zero.

For example, if RESO_ST = 6, the singleturn position (angle) is a 10-bit value in a 16-bit field. In this case, bits 15:6 contain the singleturn position while bits 5:0 are zero. Refer to INTERPOLATOR on page 21 for more information on RESO_ST.

The active-low error bit, nERR, is activated when any of the error bits in the error status register is active. Refer to STATUS REGISTERS on page 30 for more information.

The active-low warning bit, nWARN, is activated if magnet rotation speed is excessive. Refer to INTERPOLATOR on page 21 for more information on maximum rotation speeds.

Register Access

Table 89 shows the register mapping used for SPI.

Note: An access to an external EEPROM is not possible. Using OPCODEs Register Read (Single) and Register Write (Single) is not recommended.

Register Data	
Address	Content
0x00 ... 0x13	RAM
0x14 ... 0x6F	not used
0x70 ... 0x73	Status Messages
0x74 ... 0x77	Instruction Register

Table 89: Register Access

Register Read (Continuous)

The Register Read (Continuous) command (0x8A) reads data from a contiguous block of one or more RAM addresses starting at a specified address.

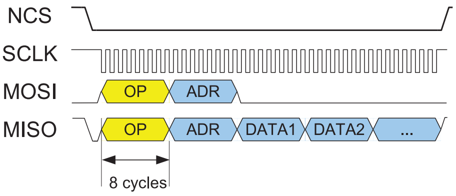

Figure 31: Register Read (Continuous)

The master transmits the read register opcode (0x8A) followed by the starting address of the block of addresses to read (ADR) on MOSI. The iC-MHM immediately outputs the opcode and address on MISO followed by the data from the register at address ADR (DATA1). As long as NCS stays active (low), data from the the next register (address ADR + 1) is then output (DATA2). Data from subsequent registers continues to be output as long as NCS remains low.

The register data channel must be activated (RACTIVE = 1) for proper operation of this command, otherwise the error bit in the SPI status byte is set. If an error occurs during a register read (invalid address, invalid data, etc.), the fail bit in the SPI status byte is set, the address counter is no longer incremented, and the data returned is invalid. Refer to Table 90 on page 50 for more information.

Register Write (Continuous)
The Register Write (Continuous) command (0xCF) writes data to a contiguous block of one or more RAM addresses starting at a specified address.

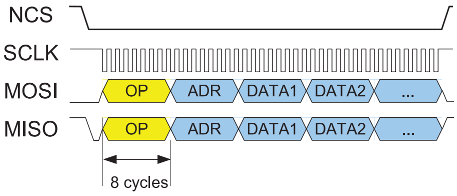

Figure 32: Register Write (Continuous)

The master transmits the write register opcode (0xCF) followed by the starting address of the block of addresses to write (ADR), followed by the data to write to the register at address ADR (DATA1), the data to write to the address at ADR + 1 (DATA2), etc. on MOSI. The iC-MHM immediately outputs the MOSI bits on MISO. Data continues to be written to subsequent registers as long as NCS stays active (low).

The register data channel must be activated (RACTIVE = 1) for proper operation of this command, otherwise the error bit in the SPI status byte is set. If an error occurs during a register write (invalid address, invalid data, etc.), the fail bit in the SPI status byte is set, the address counter is no longer incremented, and the data in not written. Refer to Table 90 on page 50 for more information.

Read Status
The Read Status command directly reads the iC-MHM status registers at address 0x70 - 0x73.

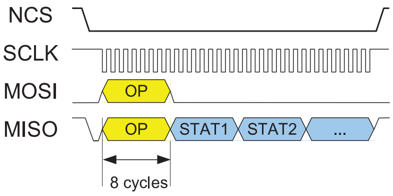

Figure 33: Read Status

The master transmits the Read Status opcode (0x9C) on MOSI. The iC-MHM immediately outputs the opcode on MISO followed by the data from the status registers starting at address 0x70 (STAT1). As long as NCS stays active (low), data from the the next status register is then output (STAT2). Data from subsequent registers continues to be output as long as NCS remains low. Refer to STATUS REGISTERS on page 30 for more information.

This command is similar to the Read Register (Continuous) command except that the starting address of the status registers does not need to be specified.

The register data channel must be activated (RACTIVE = 1) for proper operation of this command, otherwise the error bit in the SPI status byte is set. If an error occurs during a read status command (invalid address, invalid data, etc.), the fail bit in the SPI status byte is set, the address counter is no longer incremented, and the data returned is invalid. Refer to Table 90 on page 50 for more information.

Write Instruction
The Write Instruction command writes values directly to the iC-MHM instruction registers.

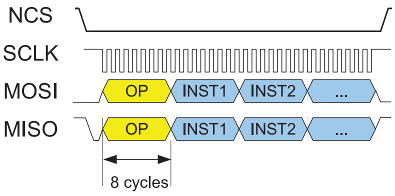

Figure 34: Write Instruction

The master transmits the Write Instruction opcode (0xD9) on MOSI, followed by the data for the instruction registers starting at address 0x74 (INST1). The iC-MHM immediately outputs the opcode and data on MISO. As long as NCS stays active (low), data for the next instruction register can be written (INST2). Data for subsequent registers can be written as long as NCS remains low. Refer to INSTRUCTION REGISTERS on page 32 for more information.

This command is similar to the Write Register (Continuous) command except that the starting address of the instruction registers does not need to be specified.

The register data channel must be activated (RACTIVE = 1) for proper operation of this command, otherwise the error bit in the SPI status byte is set. If an error occurs during a Write Instruction command (invalid address, invalid data, etc.), the fail bit in the SPI Status byte is set, the address counter is no longer incremented, and the instruction register is not written. Refer to Table 90 on page 50 for more information.

Register Read (Single)
The Register Read command (0x97) reads data from the register at the specified address. Refer to REGISTER MAP: RAM on page 16 for register addresses.

In operation, the SPI master transmits the read register opcode (0x79) followed by the address of the register to read on MOSI. The iC-MHM immediately outputs the opcode and address on MISO followed by the data from the register at the specified address.

The register data channel must be activated (RACTIVE = 1) for proper operation of this command, otherwise the error bit in the SPI status byte is set. If an error occurs during a register read (invalid address, invalid data, etc.), the fail bit in the SPI status byte is set and the data returned is invalid. Refer to Table 90 on page 50 for more information.

Register Write (Single)
The Register Write command (0xD2) writes data to the register at the specified address. Refer to REGISTER MAP: RAM on page 16 for register addresses.

In operation, the master transmits the write register opcode (0xD2) followed by the address of the register to write, followed by the data to write to the register on MOSI. The iC-MHM immediately outputs the MOSI bits on MISO.

The register data channel must be activated (RACTIVE = 1) for proper operation of this command, otherwise the Error bit in the SPI Status byte is set. If an error occurs during a register write (invalid address, invalid data, etc.), the Fail bit in the SPI Status byte is set and the data in not written. Refer to Table 90 on page 50 for more information.

Read Register Status/Data
The Read Register Status/Data command (0xAD) returns the SPI status byte which indicates the status of the last register transaction or data transmission.

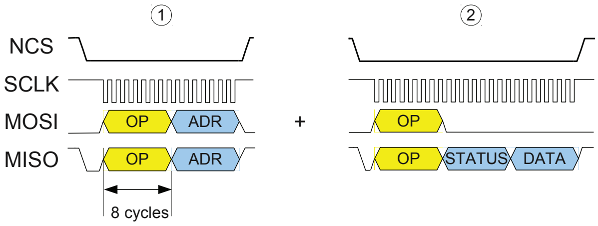

Figure 35: Read Register (single): set the read address (1) + command Register Status/Data to read-out data (2)

As shown in Figure 35, the SPI status byte is returned immediately following the opcode (STATUS) and is followed by a data byte (DATA).

Table 90 shows the SPI status byte bits.

STATUS		
Bit	Name	Description
7	Error	Invalid opcode
6:4	-	Reserved
3	Dismiss	Illegal Address
2	Fail	Data request failed
1	Busy	Slave busy
0	Valid	Data valid

Table 90: SPI Status Byte

Status bits are updated with every register access, except error, which indicates the status of the *last* command (opcode).

If the Read Register Status command immediately follows a Read Register command, the DATA byte returned by the Read Register Status command is the same as that returned by the previous Read Register command. If the Read Register Status command immediately follows a Write Register command, the DATA byte returned by the Read Register Status command is the data that was written by the previous Write Register command. With all other commands, the DATA byte is not defined.

Bussing and Chaining Multiple iC-MHMs
Multiple iC-MHMs can be bussed or chained to a single SPI master. Figure 36 shows two iC-MHMs in a chained configuration.

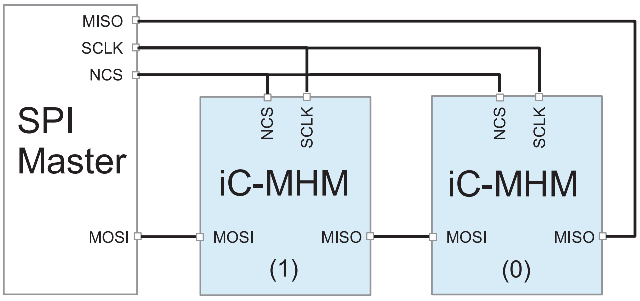

Figure 36: Chaining Multiple iC-MHMs

In this configuration, the MISO (SLO) output of each iC-MHM is chained to the MOSI (SLI) input of the next device in the chain. The SPI master must activate the desired channel(s) in a specific slave device to communicate with it. The required RACTIVE and PACTIVE bits for each slave are packed into the bytes following the Activate opcode, as shown in Figure 37.

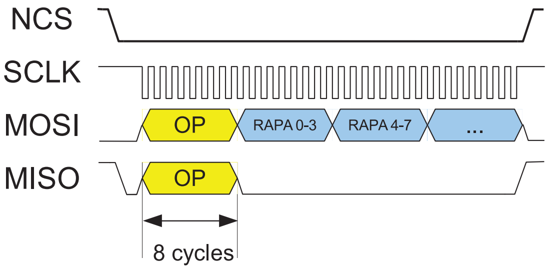

Figure 37: Activate Command For Multiple Slaves

For example, Figure 38 shows MOSI and MISO for an Activate command for one and two chained slaves.

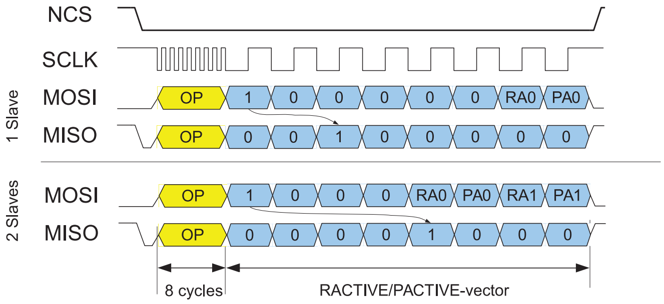

Figure 38: Activate Command For One and Two Slaves

Each slave outputs two zeros on MISO followed by the six most significant bits of MOSI and reads its RACTIVE and PACTIVE bits from bits 1 and 0 respectively of the RACTIVE/PACTIVE vector on MOSI. In this way, the RACTIVE/PACTIVE bits for the next slave in the chain are moved into bits 1 and 0 for the next slave.

The SPI master can determine the number of data channels in the chain by sending a 1 as bit 7 after the opcode in the Activate command. It then counts the number of zeros it receives on MISO before receiving the 1 back. The number of zeroes preceding the returned 1 is the number of data channels in the chain.

Figure 39 shows two iC-MHMs in a bussed configuration.

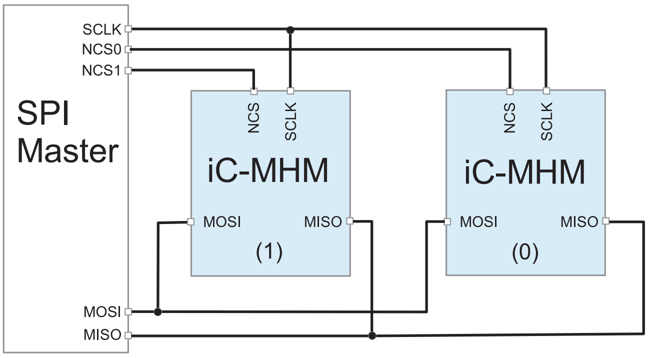

Figure 39: Bussing Multiple iC-MHMs

In this configuration, the SPI master communicates with each iC-MHM individually by activating the appropriate chip select (NCS) output.

CONFIGURATION

Before use, the iC-MHM must be configured for the intended application. Configuration consists of writing values for all the configuration parameters (refer to CONFIGURATION PARAMETERS on page 15) using the serial interface in BiSS or SPI mode and optionally storing the configuration data and checksums in an attached EEPROM for use on subsequent start ups.

The configuration is protected by its own checksum.

CRC_CFG	Addr. Address 0x0C;
Name	Description
0x00 ... 0xFF	Checksum for address range 0x00 to 0x0B; CRC polynomial 0x11D $x^8 + x^4 + x^3 + x^2 + 1$ (CRC-8) start value 0x02

Table 91: Configuration Data Checksum

Initial Configuration

The first time the iC-MHM is powered up, either with an un-programmed EEPROM or no EEPROM, configuration fails. This activates the error output (pin NERR low), and drives SLO high to indicate the error. At this point, the configuration parameters are all zero and the iC-MHM must be configured via the serial interface in BiSS or SPI mode. At least a minimum configuration must be done and the chip reset to clear the error output and release SLO to restore full BiSS bidirectional communication.

After a configuration failure due to an un-programmed EEPROM, no EEPROM, or a configuration or offset CRC failure, the iC-MHM serial port is in the following state:

Serial interface: TTL/RS-422 I/O (RTX_MODE = 0)
Multiturn feedthrough mode disabled (GET_MTI = 0)
BiSS enabled (DISBISS = 0)
SSI disabled (ENSSI = 0)
Register protection disabled (REGPROT = 0)
Command protection disabled (INSPROT = 0)

In BiSS mode, bidirectional communication is not possible at this point because SLO is driven high and SLI is ignored. Thus, the initial configuration must be written "blind" as no data is sent back from the iC-MHM. For initial configuration using BiSS mode communication, the iC-MHM is always slave 0.

Since each BiSS cycle transmits only a single CDM bit, it can be reduced to four clock cycles plus the timeout. The following Figures show such a single BiSS cycle with CDM = 0 and CDM = 1, and a four BiSS cycle extract for a CDM sequence of 0b0010.

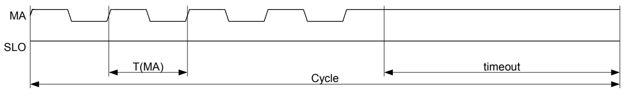

Figure 40: BiSS Cycle with CDM = 0

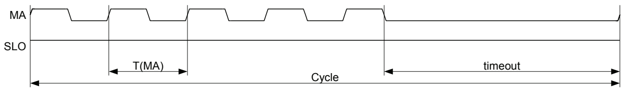

Figure 41: BiSS Cycle with CDM = 1

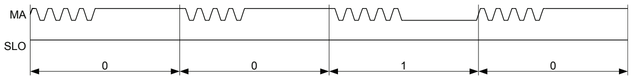

Figure 42: BiSS Cycle Extract for CDM Sequence 0b0010

To enable full bidirectional BiSS communication after a configuration failure due to an un-programmed EEPROM, no EEPROM, or a configuration or offset CRC failure, the BiSS interface must be initialized with values for parameters RTX_MODE, GET_MTI, DISBISS, ENSSI, REGPROT, and INSPROT. This means that at a minimum, registers 0x02, 0x03, 0x07, and 0x0B must be initialized.

A single BiSS register write requires 14 BiSS cycles with CDM = 0 followed by 32 cycles of BiSS C register communication data. Following is an example BiSS sequence to reset registers 0x02, 0x03, 0x07, and 0x0B and then reset the iC-MHM (0x74 = 0x01).

```
"00000000000000"
"1 1 000 0000010 0000 0 1 1 00000000 1111 0"
"00000000000000"
"1 1 000 0000011 0011 0 1 1 00000000 1111 0"
"00000000000000"
"1 1 000 0000111 1111 0 1 1 00000000 1111 0"
"00000000000000"
"1 1 000 0001011 1000 0 1 1 00000000 1111 0"
"00000000000000"
"1 1 000 1110100 0010 0 1 1 00000001 1100 0"
```

Refer to the BiSS Interface Protocol Description (C-Mode) at www.biss-interface.com for more information on BiSS register communication.

BiSS Mode Configuration

After writing the communication configuration and resetting the chip as explained above, ERR_CFG = 1, ERR_OFFS = 1, the error output is still active (pin NERR low), and the error bit in the BiSS SCD, SPI position read command response, and extended SSI frame are still active (nERROR = nE = 0) since the CRC tests fail because the configuration and offset checksums (CRC_CFG and CRC_OFFS, respectively) have not been configured. However, SLO is released and the remainder of the configuration parameters can be written using full bidirectional BiSS communication while ignoring the errors.

Once all the configuration parameter values have been written, the configuration and offset checksums (CRC_CFG and CRC_OFFS, respectively) must be calculated and stored in RAM. Please use therefore CRC-Polynomial = 100011101 and start value = 2. A sample C++ CRC checksum calculation routine is shown following.

Example of CRC Calculation Routine

```
unsigned char Reg[20] = {0x44, 0x47, 0x10, 0x1A,
    0x80, 0x00, 0x10, 0x00, 0x03, 0x80, 0x00,
    0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00,
    0x00, 0x00};
int iCRCPoly = 0x11D; // CRC-Polynomial 100011101
unsigned char ucDataStream = 0;
unsigned char ucCRC;

// Calculate Config-CRC //
ucCRC = 2; // startvalue !!!
for (int iReg = 0 ; iReg<12; iReg ++) {
  ucDataStream = Reg[iReg];
  for (int i =0; i <=7; i ++) {
    if ( (ucCRC & 0x80) != (ucDataStream & 0x80))
      ucCRC = (ucCRC << 1 ) ^ iCRCPoly ;
    else
      ucCRC = (ucCRC << 1 ) ;
    ucDataStream = ucDataStream << 1 ;
  }
}
Reg[12] = ucCRC;

// Calculate Offset-CRC //
ucCRC = 2; // startvalue !!!
for (int iReg = 13 ; iReg<19; iReg ++) {
  ucDataStream = Reg[iReg];
  for (int i =0; i <=7; i ++) {
    if ( (ucCRC & 0x80) != (ucDataStream & 0x80))
      ucCRC = (ucCRC << 1 ) ^ iCRCPoly ;
    else
      ucCRC = (ucCRC << 1 ) ;
    ucDataStream = ucDataStream << 1 ;
  }
}
Reg[19] = ucCRC;
```

With the checksums stored, the iC-MHM has to be reset by writing Address (0x74 = 1).

If an EEPROM is connected to the iC-MHM (refer to EEPROM AND I^{2}C INTERFACE on page 33), the complete configuration (including checksums) must be written to it for use on subsequent start ups. Write the configuration data in RAM addresses 0x00 - 0x13 to EEPROM addresses 0x10 - 0x23 byte by byte using BiSS register write commands. Refer to the BiSS Interface Protocol Description (C-Mode) at www.biss-interface.com for more information on BiSS register communication.

If a position preset command or enabled preset input P1 is required by the application, a value for the preset position and its checksum must also be written to the EEPROM as part of iC-MHM configuration. Write the desired preset position and its checksum to EEPROM addresses 0x48 - 0x4E byte by byte using BiSS register write commands. Refer to POSITION OFFSET AND PRESET (Zero Position) on page 55 for more information.

When writing to the EEPROM, a wait time of at least 4 ms must be allowed after each write. Alternatively, the same byte can be read back after it is written and the values compared. This comparison will fail if the EEPROM is busy with its internal write procedure. Several attempts may be required for the read value to equal the written value before the next location can be written.

SPI Mode Configuration

In SPI mode, use Register Write (Continuous) command to write all configuration parameters and then reset the iC-MHM. Refer to SERIAL INTERFACE: SPI Mode on page 46 for more information.

CALIBRATION

Complete calibration of the iC-MHM requires setting the bias current, centering the magnet, and adjusting the signal conditioning parameters to provide the lowest distortion sine and cosine signals from the Hall sensors. Calibration should be performed after configuration and in the order given following.

Gain Calibration

Calibrate the Hall sensor sine and cosine signal gain by setting GAINR = 3, GAINF = 0, and ENAC = 1. Reset the iC-MHM (0x74 = 1) for these values to take effect. This enables the automatic amplitude control to maintain the differential sine and cosine amplitudes at 1V. Refer to SIGNAL CONDITIONING on page 18 for more information.

Bias Current Calibration (CIBM)

The internal bias current is calibrated using test mode and parameter CIBM.

CIBM	Address 0x06; bits 3:0
Value	Description
0x08	50%
0x09 ... 0x0F	56.25% ... 93.75%
0x00 (±0)	100%
0x01 ... 0x07	106.25% ... 143.75%

Table 92: Bias Current Calibration

Enable test mode (TEST = 0x19) and measure the bias current between NSIN (pin 3) and GNDS (pin 16). Adjust CIBM until the current is as close to 200 µA as possible. All internal current sources are then calibrated.

After setting the bias current, disable test mode by setting TEST = 0.

Centering the Magnet

The magnet should be centered on the iC-MHM for lowest angular error and jitter. If it is possible to adjust the magnet position relative to the iC-MHM, the centering can be optimized by equalizing the amplitudes of the four analog outputs PSIN, NSIN, PCOS, and NCOS. With the magnet rotating, move it (or the iC-MHM) along the PSIN/NSIN diagonal of the iC-MHM (refer to Figure 9 on page 17) until the amplitudes of PSIN (pin 4) and NSIN (pin 3) are equal. Then, move the magnet or the iC-MHM along the PCOS/NCOS diagonal until the amplitudes of PCOS (pin 18) and NCOS (pin 19) are equal. Iteration may be required for optimum results.

Offset and Gain Correction Cosine Calibration

The sine and cosine offset correction values VOSS and VOSC, respectively, and the gain correction cosine, GCC, can be calibrated automatically or manually. Automatic calibration is performed using the calibration tab in the free iC-MHM GUI software (http://www.ichaus.com/MHM). Manual calibration is performed by configuring the digital I/O port for calibration signal outputs (CFG_IOP = 3) and adjusting the parameters as explained below.

When configured for calibration signal outputs (CFG_IOP = 3), the digital I/O port provides the following signals at P1 - P3 (pins 5 - 7, respectively) when the magnet is rotated continuously.

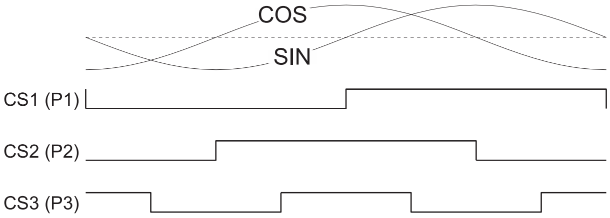

Figure 43: Calibration Signals

Adjust VOSS until the duty cycle of the CS_IO1 output (pin 5) is as close to 50% as possible. Then adjust VOSC until the duty cycle of the CS_IO2 output (pin 6) is as close to 50% as possible. Finally, adjust GCC until the duty cycle of the CS_IO3 output (pin 6) is as close to 50% as possible.

Harmonic Calibration

The harmonic calibration parameter, HARMCAL, can be set using the free iC-MHM GUI software (http://www.ichaus.com/MHM) or by using the iC-Haus SinCosYzer II Encoder Signal Analyzer (http://www.ichaus.com/SinCosYzer 2) to measure the angular error.

POSITION OFFSET AND PRESET (Zero Position)

To allow aligning the multiturn absolute position of the iC-MHM with the connected mechanical system, an electrical offset is provided. In operation, the offset value is subtracted from the measured (actual) position to generate the current position available via the serial interface in BiSS, SSI, or SPI format. Thus, the position offset allows defining the zero position of the iC-MHM to match that of the external mechanical system.

Position Offset (OFFS_MT and OFFS_ST)

The 48-bit position offset consists of a 32-bit multiturn and a 16-bit singleturn position offset. These values are stored in six registers as shown in Table 93.

OFFSET	Addresses 0x0D - 0x12	
Address	Name	Description
0x0D	OFFS_MT	Multiturn Offset Bits 31:24
0x0E	OFFS_MT	Multiturn Offset Bits 23:16
0x0F	OFFS_MT	Multiturn Offset Bits 15:8
0x10	OFFS_MT	Multiturn Offset Bits 7:0
0x11	OFFS_ST	Singleturn Offset Bits 15:8
0x12	OFFS_ST	Singleturn Offset Bits 7:0

Table 93: Position Offset

The position offset is protected by its own checksum.

CRC_OFFS	Addr. 0x13;
Name	Description
0x00 ... 0xFF	Checksum for address range 0x0D to 0x12; CRC polynomial 0x11D $x^8 + x^4 + x^3 + x^2 + 1$ (CRC-8) start value 0x02

Table 94: Position Offset Checksum

The position offset and checksum are calculated by the iC-MHM during the position preset sequence. In embedded applications using SPI communication without an external EEPROM, the position offset can also be calculated by the host processor or microcontroller during configuration. Refer to CONFIGURATION on page 52 for more information. The position offset checksum is not used with SPI mode communication.

Preset Position

In stand-alone systems using BiSS or SSI communication and an external EEPROM, the 48-bit preset position defines the location of the zero position of the iC-MHM relative to the external mechanical system. The preset position consists of a 32-bit multiturn and a 16-bit singleturn preset position stored in six EEPROM locations as shown in Table 95.

PRESET	EEPROM Addresses 0x48 - 0x4D	
Address	Name	Description
0x48	PSET_MT	Multiturn Preset Position Bits 31:24
0x49	PSET_MT	Multiturn Preset Position Bits 23:16
0x4A	PSET_MT	Multiturn Preset Position Bits 15:8
0x4B	PSET_MT	Multiturn Preset Position Bits 7:0
0x4C	PSET_ST	Singleturn Preset Position Bits 15:8
0x4D	PSET_ST	Singleturn Preset Position Bits 7:0

Table 95: Preset Position

The preset position is protected by its own checksum.

CRC_PSET	Addr. EEPROM 0x4E;
Name	Description
0x00 ... 0xFF	Checksum for address range 0x48 to 0x4D; CRC polynomial 0x11D $x^8 + x^4 + x^3 + x^2 + 1$ (CRC-8) start value 0x02

Table 96: Preset Position Checksum

The preset position must be calculated and stored in the external EEPROM during iC-MHM configuration. Refer to CONFIGURATION on page 52 for more information. Applications without an external EEPROM cannot use a non-zero preset position.

Position Preset Sequence

A position preset sequence is initiated in response to a position preset instruction (0x74 = 2), BiSS command 3, or activation of the dedicated preset input (if configured). The position preset sequence first performs a CRC on the preset position value in the external EEPROM. If the CRC passes or if there is no external EEPROM, the position preset sequence continues. If the CRC fails, the iC-MHM is reset.

The iC-MHM next calculates the position offset (OFFS_MT and OFFS_ST) necessary to make the current position (available via the serial interface in BiSS, SSI, or SPI format) equal to the preset position stored in the external EEPROM. This new position offset and its checksum (CRC_OFFS) are then stored in the external EEPROM for use in subsequent start ups. Finally, the iC-MHM is reset.

If no external EEPROM is present, the position preset sequence still proceeds as explained above, but a preset position of zero is used and the new position offset is only stored in RAM.

For example, many stand-alone applications use a preset position of zero so that a preset instruction or the enabled preset input P1 is effectively a zero instruction or input. In this case, initiating a position preset sequence causes the current actual position to be the zero position.

A flowchart of the position preset sequence is shown in Figure 44 in the STARTUP AND OPERATION section.

STARTUP AND OPERATION

Startup
As shown in red in Figure 44, after power on, the iC-MHM attempts to read the configuration and offset data from an external EEPROM via the I^2C multi-master interface. During this period, the error output is active (NERR = 0) and SLO is driven high to indicate that serial port communication is not possible. If a properly configured EEPROM is present, the EEPROM data is read into RAM and two CRCs are done to verify the configuration and offset data.

If no EEPROM is present or a CRC fails, two more attempts to read the EEPROM are made. After the third failed attempt, the iC-MHM goes into an idle state with the error output activated (NERR = 0) and SLO driven high to indicate the error. In this case, the iC-MHM must be configured or re-configured as explained in CONFIGURATION on page 52.

If the CRCs pass, the configuration and offset data are valid and SLO is released, allowing communication via the serial port.

Startup proceeds as shown in yellow in Figure 44. First, the automatic amplitude control is started if enabled (ENAC = 1) and the singleturn position (magnet angle) is calculated. Then, if the multiturn interface is enabled (SBL_MTI > 0), the multiturn data is read from the external multiturn sensor and synchronized with the singleturn data. This process repeats indefinitely if a multiturn error occurs. Refer to MULTITURN INTERFACE on page 23 for more information.

During this phase of startup, absolute position is not yet available. If requested, a zero value is returned. In addition, the error and warning bits in the BiSS SCD, SPI position read command response, and extended SSI frame are active (nERR = nWARN = nE = nW = 0).

If there are no errors, the error output is de-activated (NERR = 1), the error and warning bits in the BiSS SCD, SPI position read command response, and extended SSI frame are de-activated (nERR = nWARN = nE = nW = 1), and the iC-MHM is ready for normal operation. Refer to STATUS REGISTERS on page 30 for more information on errors.

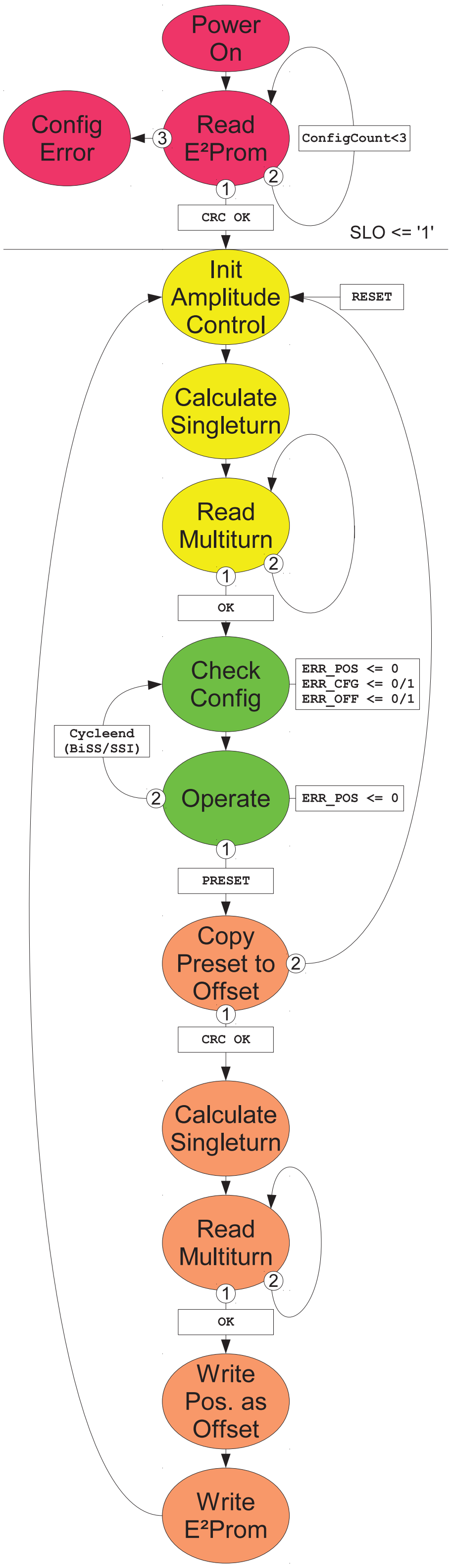

Figure 44: State Diagram

Operation

As shown in green in Figure 44, during normal operation, the singleturn position (angle) and multiturn count is constantly updated and available over the serial interface and the incremental outputs (if enabled). The internal multiturn count is also verified against the external multiturn sensor on a periodic basis. If the counts disagree, ERR_MT in the error status register is set, the error output is activated (NERR = 0), and the error bit in the BiSS SCD, SPI position read command response, and extended SSI frame are activated (nERR = nE = 0).

After every BiSS or SSI cycle, the validity of the configuration parameters and offset data in RAM is verified using CRCs. If either CRC fails, the appropriate error bit in the error status register is set, the error output is activated (NERR = 0), and the error bit in the BiSS SCD, SPI position read command response, and extended SSI frame are activated (nERR = nE = 0). Refer to STATUS REGISTERS on page 30 for more information.

Position Preset Sequence

The position preset sequence is shown in orange in Figure 44. In response to a preset instruction (0x74 = 2), BiSS command 3, or the dedicated preset input (if configured), new position offset values are calculated based on the position preset values in EEPROM and the current absolute position of the magnet. A CRC is done on the preset values and the chip is reset if the CRC fails. Refer to POSITION OFFSET AND PRESET (Zero Position) on page 55 for more information.

During the absolute position preset sequence, the position is not available. If requested, a zero value is returned. In addition, the error and warning bits in the BiSS SCD, SPI position read command response, and extended SSI frame are active (nERR = nWARN = nE = nW = 0).

APPLICATION EXAMPLE 1: Multiturn Encoder Using iC-PV

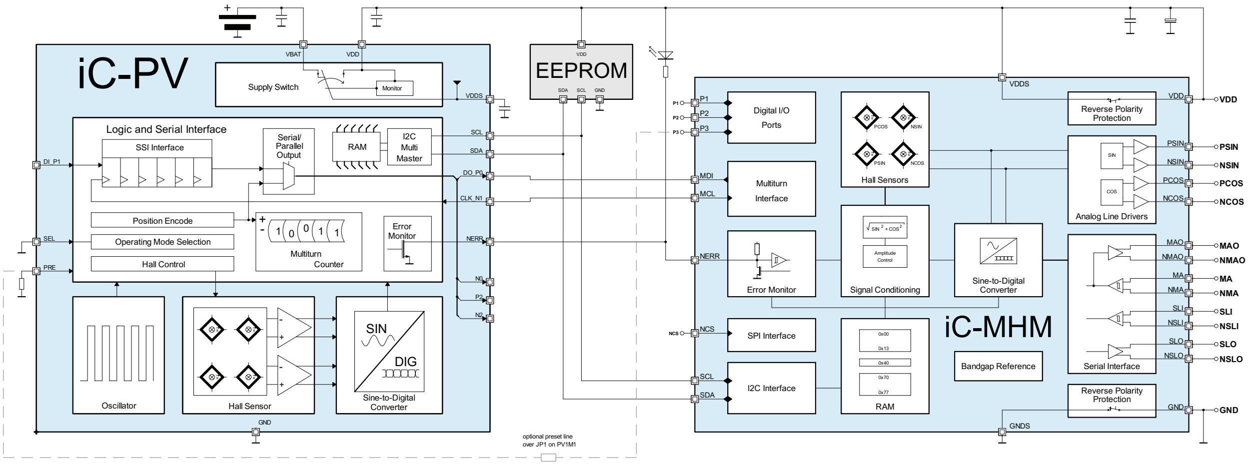

Figure 45: Magnetic Absolute Encoder with Battery-Buffered Multiturn Sensor.
Both devices share a single EEPROM configured via the iC-MHM BiSS interface.
Reverse polarity protection not used.

Note: Circuit examples are provided for illustration of principle. Additional components required for a successful application may be omitted for clarity.

APPLICATION EXAMPLE 2: Multiturn Encoder Using iC-MV

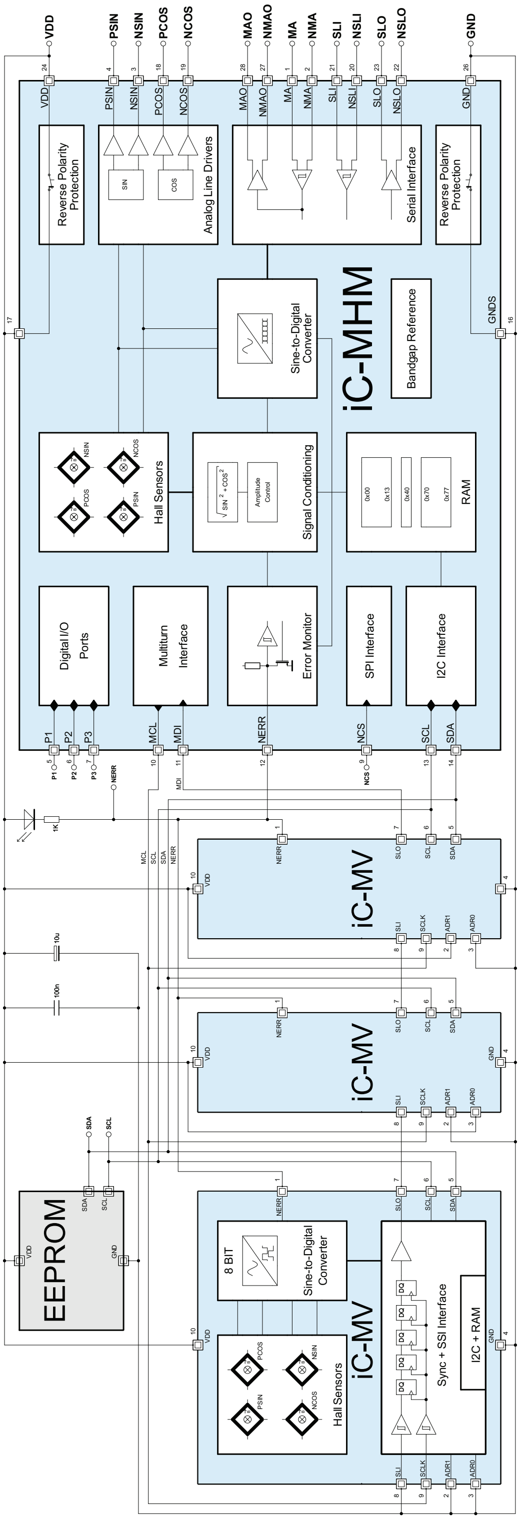

Figure 46: Multiturn Encoder Using Three iC-MVs with iC-MHM.
All devices share a single EEPROM configured via the iC-MHM BiSS interface.

Note: Circuit examples are provided for illustration of principle. Additional components required for a successful application may be omitted for clarity.

DESIGN REVIEW: Notes on Chip Functions

iC-MHM X2		
No.	Function, Parameter/Code	Description and Application Hints
1	DIR	Averaging Filtering functionality requires DIR = 0 (normal rotation) for configuration.
2	Parameters: NTOA, CHIP_REL, I2CDEV, BSEL, ENCMD01	Function not implemented.

Table 97: Notes on chip functions regarding iC-MHM chip release X2.

iC-MHM X5		
No.	Function, Parameter/Code	Description and Application Hints
		No further notes at time of printing.

Table 98: Notes on chip functions regarding iC-MHM chip release X5.

REVISION HISTORY

Rel.	**Rel. Date***	**Chapter**	**Modification**	**Page**
A1	2013-11-25	All	Initial release	All

Rel.	**Rel. Date***	**Chapter**	**Modification**	**Page**
B1	2014-10-11	All	Global update	All

Rel.	**Rel. Date***	**Chapter**	**Modification**	**Page**
B2	2015-04-17	DESIGN REVIEW	Design Review correction	36

Rel.	**Rel. Date***	**Chapter**	**Modification**	**Page**
C1	2016-12-16	All	Global update	
		ELECTRICAL CHARACTERISTICS	Items No. 713, 905: typ. value changed Item No. 904: characteristics for fixed (adaptive) timeout Item No. 925: min. and max. value changed Item No. 926: min. value changed Item No. 931: moved from I107, I121, I209 to 910, 921, 931 Figure 2 added	9 - 11
		OPERATING REQUIREMENTS	Items No. I105, I108, I109, I110,I112 and I202: min. value changed Figure 6 and 7 updated	12 - 13
		OVERVOLTAGE PROTECTION	New chapter added	14
		INSTRUCTION REGISTERS	New chapter added	32
		TEST MODE	New chapter added	33

		CONFIGURATION PARAMETERS	New parameter NTOA, CHIP_REL, I2CDEV, BSEL and ENCMD01 added Re-named parameter: **Signal Conditioning** GAING → GAINR **Interpolator** R_ST → RESO_ST CFGFLT → AVGFILT ROT → DIR MTD → TLF **Multiturn Interface** F_MTI → CF_MTI R_MT → RESO_MT GET_MT → GET_MTI **Digital I/O Port** CFGDIO → CFG_IOP P0 → F_IO0 and S_IO0 P1 → F_IO1 and S_IO1 P2 → F_IO2 and S_IO2 P3 → F_IO3 and S_IO3 ENPRES_P → PRES_IO1 ENROT_P → DIR_IO2 ENINST_2 → ENCMD2 **Status Registers** ERR_OFF → ERR_OFFS ERR_ST → ERR_POS **Instruction Registers** COMPROT → INSPROT **Serial Interface: General** CFGIF → RTX_MODE **Serial Interface: BiSS Mode** CRC_ID → CRCS ENPRES_I → ENCMD3 **Serial Interface: SSI Mode** EXTSSI → EXT_SSI BINSSI → BIN_SSI **Position Offset and Preset** OFFSET_MT → OFFS_MT OFFSET_ST → OFFS_ST CRC_OFF → CRC_OFFS PRESET_MT → PSET_MT PRESET_ST → PSET_ST CRC_PRST → CRC_PSET	15 ff
		HALL SENSORS: Principle of Operation	Figure 9, 11 and 12 added	17
		INTERPOLATOR	Table 15 extended to influence of RESO_ST und AVGFILT	23
		DIGITAL I/O PORT	Table 22, 26, 30 and 34 added	26 - 28
		EEPROM AND I^{2}C INTERFACE (Multi-master)	Figure 18 and Table 50, 51, 52 added	33 - 34
		SERIAL INTERFACE: General	Figure 19, 20 added	36
		SERIAL INTERFACE: BiSS Mode	Figure 21 and 22 reworked, Figure 23 and 24 added. Table 64 and 70 reworked, Table 62, 71 and 72 added.	41 - 42
		SERIAL INTERFACE: SSI Mode	Standard and extended SSI protocol description added.	44
		ORDERING INFORMATION	Plug-in adapter iC-MHM iCSY MHM3M added	63

Rel.	Rel. Date*	Chapter	Modification	Page
D1	2017-05-15	ABSOLUTE MAXIMUM RATINGS	Items No. G003 and G004 added Item No. G005: max. value changed	7
		REVERSE POLARITY PROTECTION	Note added	14

Rel.	Rel. Date*	Chapter	Modification	Page
D2	2018-06-22	ELECTRICAL CHARACTERISTICS	Item No. 403: conditions changed CIBM = 0x0 → 0x8 and CIBM = 0xF → 0x7	8
		REVERSE POLARITY PROTECTION	Additional note added	14
		OVERVOLTAGE PROTECTION	Figure 8 supplemented with a diode	15
		SERIAL INTERFACE: BiSS Mode	Table 64 reworked	39
		APPLICATION EXAMPLE	Figure 44 and Figure 45 reworked	59 - 60

Rel.	Rel. Date*	Chapter	Modification	Page
E1	2022-01-05	ELECTRICAL CHARACTERISTICS	Item No. 305: max. value changed	8
		DESCRIPTION	Note box added	2
		OPERATING REQUIREMENTS: Serial Interface (SPI)	Item No. I212 and I213 added	13
		INTERPOLATOR	Table 13 reworked and description for AVGFILT ≠ 0 added Correction of the second calculation of the TLF parameter.	22
		DIGITAL I/O PORT	Resolution of the ABZ signals is limited to 12 bit	29
		SERIAL INTERFACE: SPI Mode	Figure 28 added	46

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* Release Date format: *YYYY-MM-DD*

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ORDERING INFORMATION

Type	Package	Order Designation
iC-MHM	28-pin QFN, 5 mm x 5 mm x 0.9 mm, RoHS compliant	iC-MHM QFN28-5x5
MHM1D Evaluation board		iC-MHM EVAL MHM1D
MHM3M Plug-in adapter	DIL28 Plug-in Adapter with iC-MHM	iC-MHM iCSY MHM3M

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