iC-NV, iC-NVH

6-Bit Sin/D Flash Converter

FEATURES

- Fast flash converter
- Integrated glitch filter; minimum transition distance can be set using the optional resistor
- Selectable resolution of up to 64 steps per cycle and up to 16-fold interpolation
- Integrated instrumentation amplifiers with adjustable gain
- Direct connection of sensor bridges, no external components required
- 200 kHz input frequency with the highest resolution
- Incremental A QUAD B output of up to 3.2 MHz
- Reversed A/B phase selectable
- Index signal processing with 1/4 T gating (**iC-NV**), or with 1/2 T gating (**iC-NVH**)
- Sensor bridge calibration supportable by analog/digital test signals
- Low power consumption from single 5V supply
- TTL- /CMOS-compatible outputs
- Inputs and outputs protected against destruction by ESD

APPLICATIONS

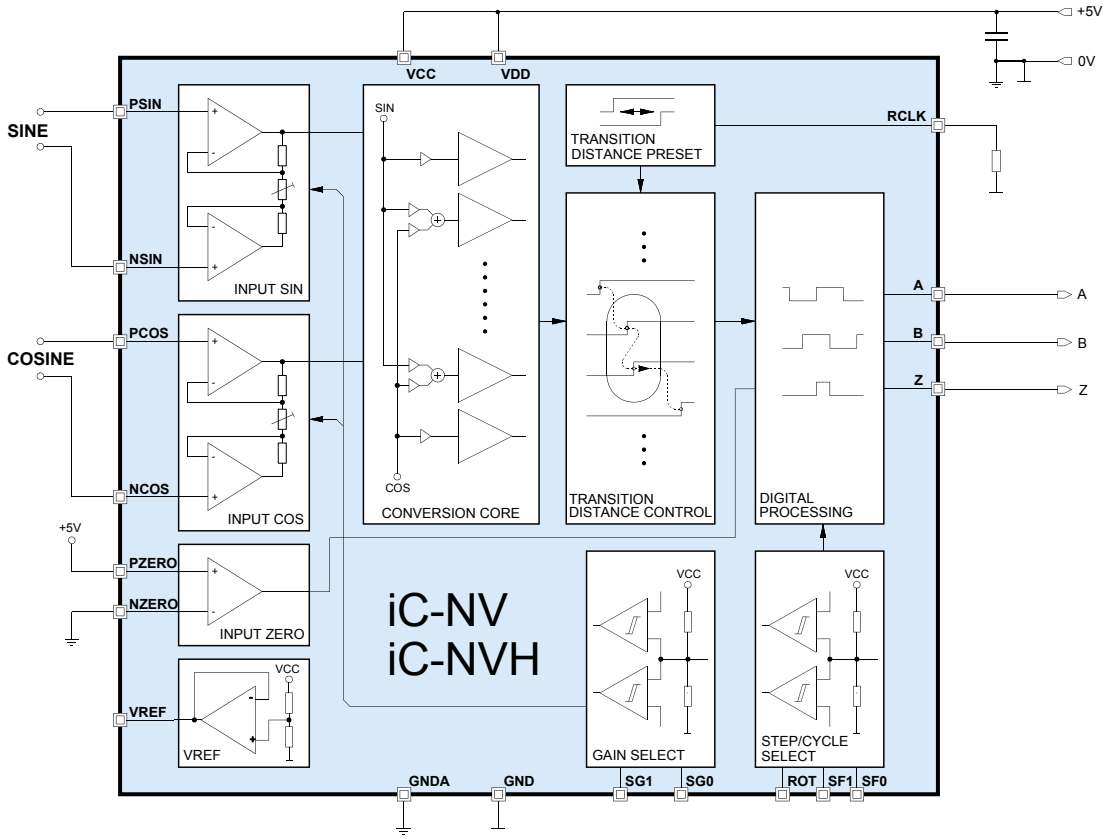
- Angle interpolation from orthogonal sinusoidal input signals
- Linear and rotary encoders
- MR sensor systems

PACKAGES

TSSOP20

RoHS compliant

BLOCK DIAGRAM



DESCRIPTION

iC-NV is a monolithic A/D converter which produces two digital A/B incremental signals phase-shifted at 90° from two sinusoidal input signals, also phase-shifted at 90°.

The converter operates on the flash principle with fast single comparators. The back-end signal processing circuit includes a no-delay glitch filter which can be set so that only clearly countable incremental signals are generated. The minimum transition distance for outputs A and B can be set via an external resistor and adapted to suit the application on hand. For static input signals hysteresis prevents the switching of the outputs.

By programming the pins the interpolator can be set to nine different resolutions between 4 and 64 angle steps per cycle; multiplication values of between 1 and 16 are possible for the frequency. The phase relation between the sine/cosine input signals and the A/B incremental signals generated can be selected here.

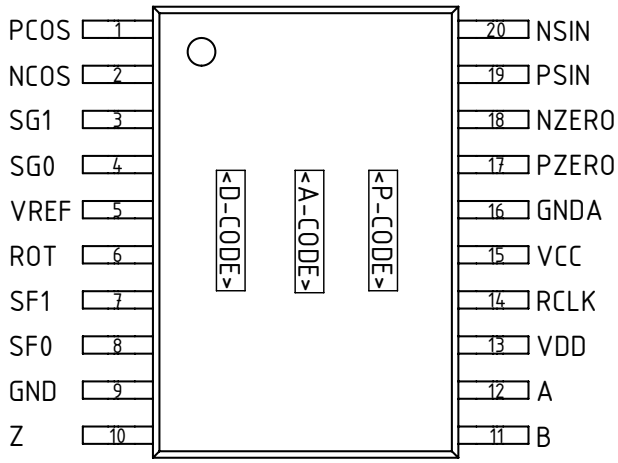
The device also incorporates an index signal processing circuit which generates a digital zero pulse at Z dependent on the analog sine/cosine input signals and the enable input ZERO. Alternatively, the converter MSB can also be output at Z for synchronization purposes in an absolute measuring system.

The input amplifiers are configured as instrumentation amplifiers and permit sensor bridges to be directly connected without the need for external resistors. The input amplification has nine selectable settings which have been graded to suit standard sensor signals of between approx. 10 mVpk and 1 Vpk. If external calibration of the sensor bridge is required, e.g. with regard to offset, various test functions can be activated. By this the amplified analog input signals come available at the outputs, for instance.

CONTENTS

PACKAGING INFORMATION

PIN CONFIGURATION TSSOP20 4.4mm (top view)



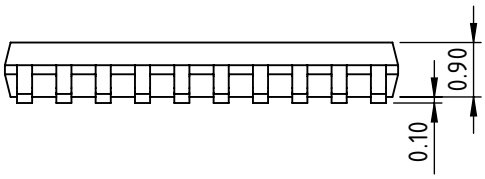
PIN FUNCTIONS

No.	Name	Function
1	PCOS	Input Cosine +
2	NCOS	Input Cosine -
3	SG1	Gain Select Input
4	SG0	Gain Select Input
5	VREF	Reference Voltage Output
6	ROT	A/B Phase Selection, Test Signal S6 Input/Output
7	SF1	Resolution Selection, Test Signal S5 Input/Output
8	SF0	Resolution Selection, Test Signal S4 Input/Output
9	GND	Ground (digital)
10	Z (MSB)	Index Signal Output Z (MSB Output when ROT= open), Test Signal S3 Input/Output
11	B	Incremental Output B, Test Signal S2 Input/Output
12	A	Incremental Output A, Test Signal S1 Input/Output
13	VDD	+5 V Supply Voltage (digital)
14	RCLK	Min. Transition Distance Preset Input (use is optional; can be wired to VCC)
15	VCC [1]	+5 V Supply Voltage (analog)
16	GNDA [1]	Ground (analog)
17	PZERO	Index Signal Enable Input +
18	NZERO	Index Signal Enable Input -
19	PSIN	Input Sine +
20	NSIN	Input Sine -

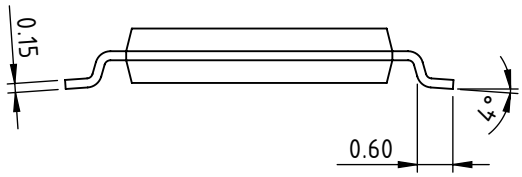
IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes), <D-CODE> = date code (subject to changes);
[1] External connections linking VCC to VDD and GND to GNDA are required.

PACKAGE DIMENSIONS

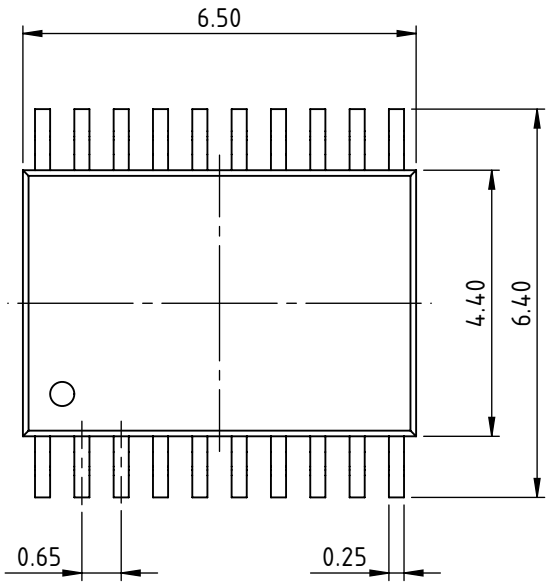
SIDE



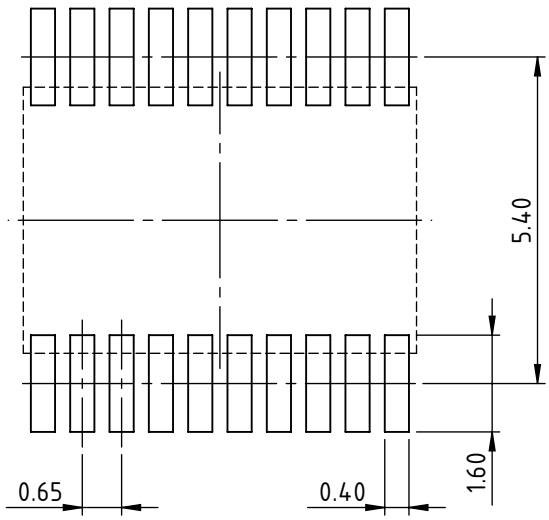
FRONT



TOP



RECOMMENDED PCB-FOOTPRINT



All dimensions given in mm.
Tolerances of form and position according to JEDEC MO-153

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ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VCC	Voltage at VCC		-0.3	6	V
G002	VDD	Voltage at VDD		-0.3	6	V
G003	V()	Voltage at NSIN, PSIN, NCOS, PCOS, NZERO, PZERO, SG1, SG0, RCLK SF1, SF0, ROT, A, B, Z	V() < VCC + 0.3 V V() < VDD + 0.3 V	-0.3	6	V
G004	Imx(VCC)	Current in VCC		-50	50	mA
G005	Imx(GNDA)	Current in GNDA		-50	50	mA
G006	Imx(VDD)	Current in VDD		-50	50	mA
G007	Imx(GND)	Current in GND		-50	50	mA
G008	Imx()	Current in NSIN, PSIN, NCOS, PCOS, NZERO, PZERO, SG1, SG0, VREF, RCLK, SF1, SF0, ROT, A, B, Z		-10	10	mA
G009	Ilu()	Pulse Current in all pins (Latch-up strength)	pulse duration < 10 µs	-100	100	mA
G010	Vd()	ESD Susceptibility at all pins	100 pF discharged through 1.5 kΩ		2	kV
G011	Tj	Junction Temperature		-40	150	°C

THERMAL DATA

Operating Conditions: VCC = VDD = 5 V ±10 %

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range	 TSSOP20 ET -40/125	-25 -40		85 125	°C °C
T02	Ts	Storage Temperature Range		-40		165	°C

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VCC = VDD = 5 V ± 10 %, Tj = -40...125 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VCC, VDD	Permissible Supply Voltage		4.5		5.5	V
002	I(VCC)	Supply Current in VCC	fin() = 200 kHz; A, B, Z open			15	mA
003	I(VDD)	Supply Current in VDD	fin() = 200 kHz; A, B, Z open			5	mA
004	Von	Power-On Reset Threshold		2		3.8	V
005	Voff	Power-Down Reset Threshold		1		2.2	V
006	Vhys	Power-On Reset Hysteresis		0.4		1.8	V
007	Vc()hi	Clamp Voltage hi at NSIN, PSIN, NCOS, PCOS, NZERO, PZERO, SG1, SG0, ROT, SF1, SF0, VREF, RCLK	Vc()hi = V()- VCC; I() = 1 mA, other pins open	0.3		1.6	V
008	Vc()lo	Clamp Voltage lo at NSIN, PSIN, NCOS, PCOS, NZERO, PZERO, SG1, SG0, ROT, SF1, SF0, VREF, RCLK, A, B, Z	I() = -1 mA, other pins open	-1.5		-0.3	V
009	Vc()hi	Clamp Voltage hi at A, B, Z	Vc()hi = V() - VDD; I() = 1 mA, other pins open	0.3		1.6	V
Input Amplifiers NSIN, PSIN, NCOS, PCOS							
101	Vos()	Input Offset Voltage	Vin() see table gain select GAIN = 10...66 GAIN = 3...7.1	 -7 -10		 7 10	 mV mV
102	Iin()	Input Current	V() = 0 V...VCC	-50		50	nA
103	G()	Gain	GAIN following table gain select	95		101	%
104	Grel	Gain Ratio SIN/COS	GAIN following table gain select	98		102	%
105	fhc	Cut-off Frequency	GAIN = 66.667 GAIN = 3.03	0.5 2.3			MHz MHz
106	SR	Slew Rate	GAIN = 66.667 GAIN = 3.03	10 15			V/µs V/µs
Signal Processing: Converter Accuracy							
201	AAabs	Absolute Angle Accuracy	referred to 360° input signal, GAIN =3.03; VPin = 2...2.6 Vpp, VNin = 2.5 Vdc VPin = 1...1.3 Vpp, VNin = 2.5 Vdc	 -1 -2		 1 2	 DEG DEG
202	AArel	Relative Angle Accuracy	referred to period of A, B (see figure 7) GAIN = 3.03	 -10		 10	 %
VREF							
401	V(VREF)	Reference Voltage at VREF	I(VREF) = -1 mA...+1 mA	48		52	%VCC
Signal Processing: Transition Distance Control							
501	RCLK	Permissible Resistor at RCLK vs. GNDA	DIV = 1 (IPF = 10, 12, 16) DIV = 2 (IPF = 5, 8) DIV = 4 (IPF = 3, 4) DIV = 8 (IPF = 2) DIV = 16 (IPF = 1)	47 23 12 6 3		500 500 500 500 500	kΩ kΩ kΩ kΩ kΩ
502	DT()	Minimum Transition Distance	R(RCLK, GNDA) = 47 kΩ 1%; DIV = 1 (see figure 4) DIV = 16 (see figure 2)	 45 490		 78 1000	 ns ns
503	DT()	Minimum Transition Distance	V(RCLK) = VCC; DIV = 1 DIV = 16	 30 420		 78 1000	 ns ns
Zero Comparator							
701	Vos()	Input Offset Voltage	V() = Vcm()	-20		20	mV
702	Iin()	Input Current	V() = 0 V ... VCC	-50		50	nA
703	Vcm()	Common-Mode Input Volt. Range		1.4		VCC -1.5	V
704	Vdm()	Differential Input Voltage Range		0		VCC	V

ELECTRICAL CHARACTERISTICS

Operating Conditions: VCC = VDD = 5 V ± 10 %, Tj = -40...125 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Signal Processing: Inputs SG1, SG0, ROT, SF1, SF0							
801	Vt()hi	Input Threshold Voltage hi		60		78	%VCC
802	Vt()lo	Input Threshold Voltage lo		25		40	%VCC
803	V0()	Mid Level Voltage		43		57	%VCC
804	Ri()	Input Resistance		45	150	220	kΩ
Signal Processing: Outputs A, B, Z							
D01	Vs()hi	Saturation Voltage hi	Vs()hi = VDD - V(); I() = -4 mA			0.4	V
D02	Vs()lo	Saturation Voltage lo	I() = 4 mA			0.4	V
D03	tr()	Rise Time	CL() = 50 pF			60	ns
D04	tf()	Fall Time	CL() = 50 pF			60	ns

ELECTRICAL CHARACTERISTICS: Diagrams

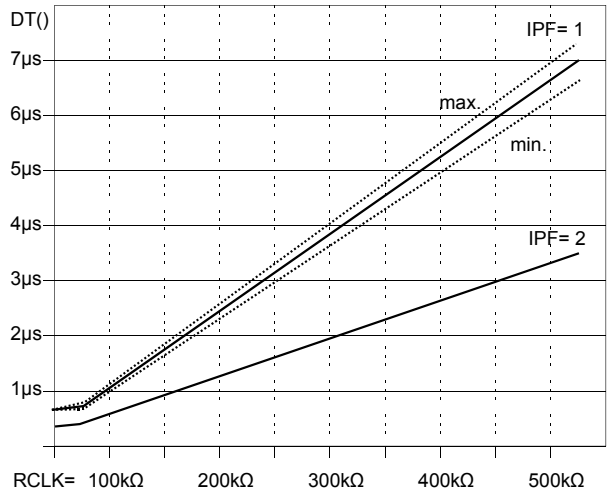


Figure 1: Adjusting the minimum transition distance via resistor RCLK (given typical at 5V, 27°C; for IPF= 1 within 5V ±10% and -40..+125°C ranges).

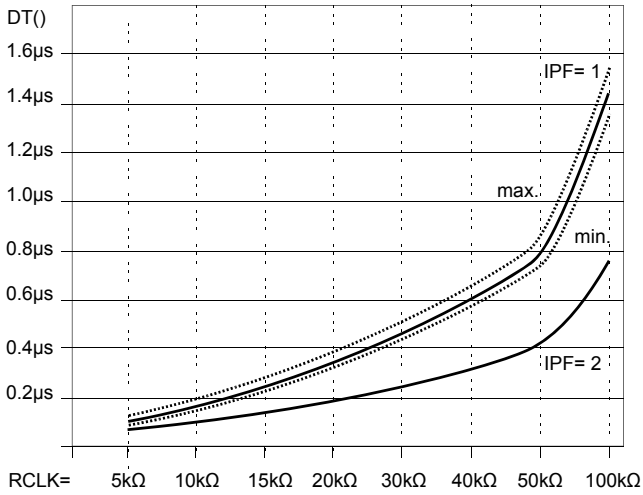


Figure 2: Similar to Figure 1; the minimum transition distance can be reduced by smaller resistors RCLK.

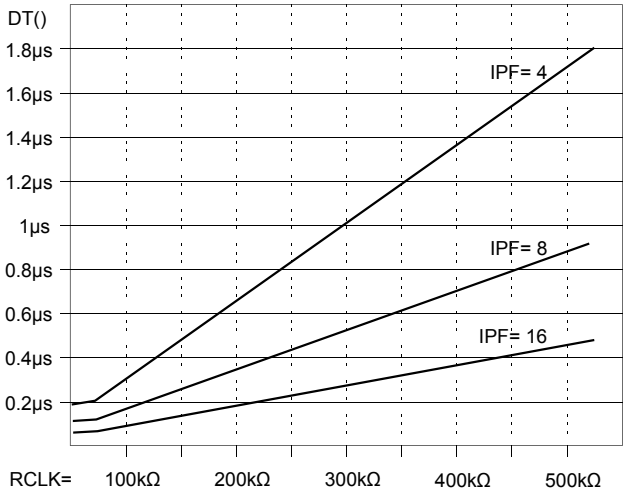


Figure 3: Adjusting the minimum transition distance via resistor RCLK.

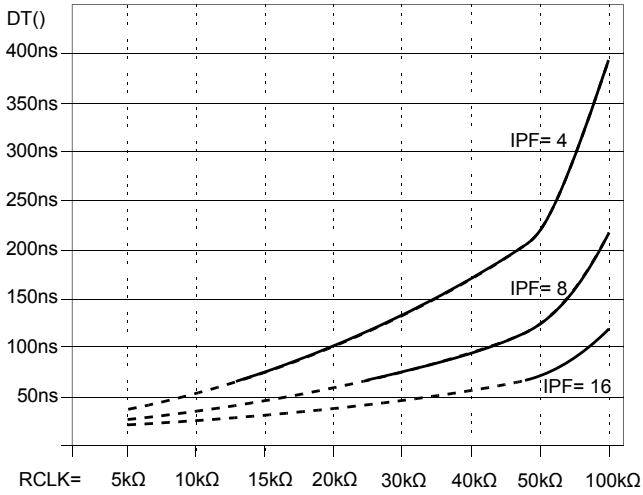


Figure 4: Similar to Figure 3; minimum transition distance for smaller RCLK resistor values.

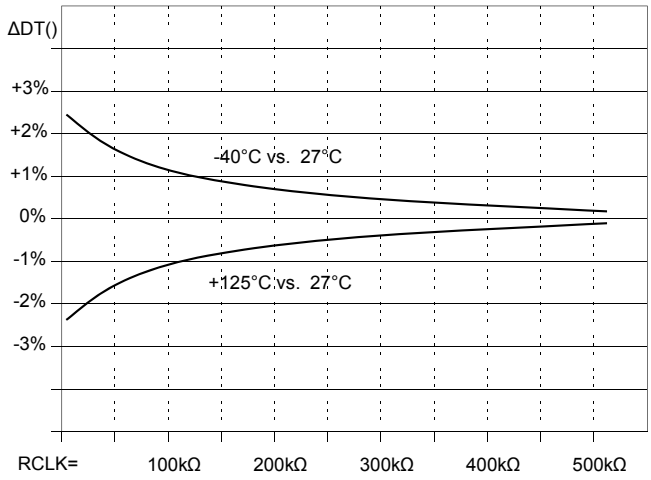


Figure 5: Temperature drift of the minimum transition distance versus 27°C (VDD= 5V).

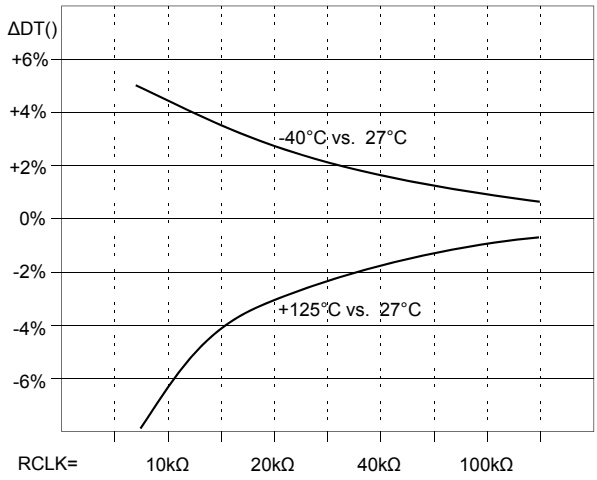


Figure 6: Temperature drift of the reduced minimum transition distance versus 27°C (VDD= 5V).

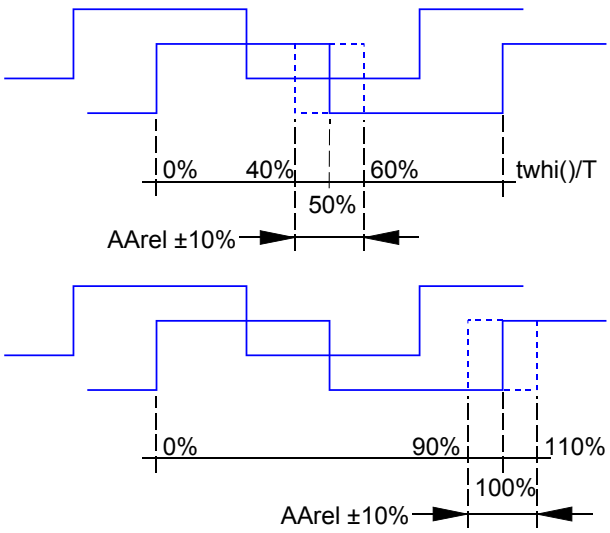


Figure 7: Definition of the relative angle accuracy.

DESCRIPTION OF FUNCTIONS

Input Amplifiers

Input stages SIN and COS are configured as instrumentation amplifiers. The gain is dependent on the amplitude of the input signal and set via pins SG0 and SG1 according to the following table. So that the DC level to be adjusted half of the supply voltage is available at VREF.

GAIN SELECT						
SG1	SG0	Gain	Sine/Cosine Input Signal Levels Vin()			
			Amplitude		Average value (DC)	
			differential	single ended	differential	single ended
hi	hi	66.667	up to 60 mVpp	up to 120 mVpp	0.7 V ... VCC – 1.2 V	0.7 V ... VCC – 1.2 V
hi	open	50.000	up to 80 mVpp	up to 160 mVpp	0.7 V ... VCC – 1.2 V	0.7 V ... VCC – 1.2 V
hi	lo	33.333	up to 120 mVpp	up to 240 mVpp	1.2 V ... VCC – 1.2 V	1.2 V ... VCC – 1.3 V
open	hi	20.000	up to 0.2 Vpp	up to 0.4 Vpp	1.2 V ... VCC – 1.2 V	1.2 V ... VCC – 1.3 V
open	open	14.300	up to 0.28 Vpp	up to 0.56 Vpp	0.7 V ... VCC – 1.3 V	0.8 V ... VCC – 1.4 V
open	lo	10.000	up to 0.4 Vpp	up to 0.8 Vpp	1.2 V ... VCC – 1.3 V	1.3 V ... VCC – 1.5 V
lo	hi	7.125	up to 0.56 Vpp	up to 1.1 Vpp	1.2 V ... VCC – 1.4 V	1.4 V ... VCC – 1.7 V
lo	open	4.000	up to 1 Vpp	up to 2 Vpp	1.2 V ... VCC – 1.6 V	1.6 V ... VCC – 2.1 V
lo	lo	3.030	up to 1.3 Vpp	up to 2.6 Vpp	1.2 V ... VCC – 1.7 V	1.8 V ... VCC – 2.4 V

Table 4: Input gain

Converter Core, Transition Distance Control

For each of the 64 comparator levels the sine/cosine input signals are calculated according to the theorem of addition and are fed into single comparators. This procedure guarantees a very high converter frequency yet also means that consecutive comparators can switch in a very short space of time in the event of input signal disturbances.

The comparator outputs are thus fed into a transition distance control unit. This monitors the temporal sequence of the switching operations in such a way that each event is delayed by the length of the settable minimum gap to the previous event. If no errors arise the transitions pass the control unit without a time delay. Synchronization with a fixed clock pulse does not occur.

The minimum transition distance is set via an external resistor positioned between RCLK and GNDA. Alternatively, pin RCLK can be shorted to VCC. Depending on the resolution maximum input frequencies of at least 200kHz are then guaranteed (see table of resolution).

Digital Processing Unit

The transition distance control unit is followed by the digital processing unit. This is where the transition events are converted into a pulse sequence for the incremental outputs A and B. The square-wave signals generated have a phase shift of +90° or -90°, depending on the direction of rotation. The phase relation between the sine/cosine input signals and the A/B output signals can be set using programming pin ROT.

Alternatively, the MSB of the converter can be output to Z when ROT is high. With the zero signal this changes to high and has the pulse length of half a cycle. This signal can be used to synchronize the high-order tracks of an absolute-value encoder device.

A/B OUTPUT PHASE SELECTION		
ROT	Input signals	Output signals A, B; Z
lo	positive; COS leading SIN	B leading A; Z
lo	negative; SIN leading COS	A leading B; Z
open	positive; COS leading SIN	B leading A; MSB
open	negative; SIN leading COS	A leading B; MSB
hi	positive; COS leading SIN	A leading B; Z
hi	negative; SIN leading COS	B leading A; Z

Table 5: Output phase

Resolution, frequency ranges

Nine different resolutions or interpolation factors (IPF) can be programmed via inputs SF0 and SF1. Resolutions 16, 12 and 10 are generated at the core of the converter itself. Resolutions of less than 10 are produced by division DIV in the digital processing unit. The minimum transition distance at outputs A and B corresponds to that of the transition distance control multiplied by the divisor of the digital processing unit.

The minimum output transition distance (maximum output frequency) should be adjusted to tarry with the overall system (bandwidth of the transfer medium, sampling rate of the counter). The maximum input frequency is determined by the transition distance control and the resolution of the converter core (16, 12 or 10). This frequency can be increased for resolutions of less than 10 with an external resistor at RCLK. The following table gives possible settings.

RESOLUTION					
SF1	**SF0**	**IPF**	**DIV** internal division	**fin_{MAX}**	**fin_{MAX}** for RCLK = VCC or RCLK = 47 kΩ
hi	hi	16	1	200 kHz, RCLK = 47 kΩ	200 kHz
hi	open	12	1	260 kHz, RCLK = 47 kΩ	260 kHz
hi	lo	10	1	320 kHz, RCLK = 47 kΩ	320 kHz
open	hi	8	2	400 kHz, RCLK = 23 kΩ	200 kHz
open	open	5	2	640 kHz, RCLK = 23 kΩ	320 kHz
open	lo	4	4	800 kHz, RCLK = 12 kΩ	200 kHz
lo	hi	3	4	1.04 MHz, RCLK = 12 kΩ	260 kHz
lo	open	2	8	1.6 MHz, RCLK = 6 kΩ	200 kHz
lo	lo	1	16	(3.2 MHz), RCLK = 3 kΩ	200 kHz

Table 6: Resolution

Hysteresis

iC-NV has an angular hysteresis which is independent of the input amplitude and phase. It prevents the outputs from switching when the inputs are static.

When the direction of rotation is reversed the integrated hysteresis circuit prompts the change in direction to be signaled at the outputs; the hysteresis causes a delay here. Figure 8 shows this effect for an interpolation factor of 8.

According to the resolution the hysteresis is set to a fixed value as listed in Table 7.

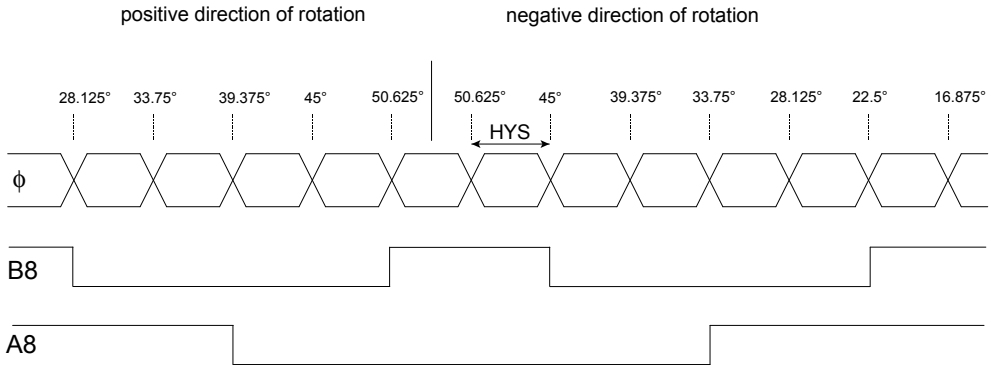


Figure 8: Effect of angle hysteresis

ANGLE HYSTERESIS									
Interpolation factor IPF	1	2	3	4	5	8	10	12	16
Hysteresis [deg]	5.625 °	5.625 °	7.5 °	5.625 °	9 °	5.625 °	9 °	7.5°	5.625 °
Referred to A/B period	1/64	1/32	1/16	1/16	1/8	1/8	1/4	1/4	1/4

Table 7: Hysteresis

Zero pulse
One zero pulse (index) is generated per cycle from the sine/cosine inputs. To be output to Z it must be enabled by the comparator at differential inputs PZERO and NZERO.

For iC-NV: The width of the zero pulse is **a quarter** of the length of the A and/or B signal output cycle. When **Z is high**, simultaneously **AB are high**.

For iC-NVH: The width of the zero pulse is **half** the length of the A and/or B signal output cycle. When **Z is high**, simultaneously **A is high**.

The position of the zero pulse dependent on the interpolation factor and the direction of rotation is given in the following tables.

INDEX WIDTH and POSITION of iC-NV			
IPF	Z Width	Z Position with positive direction of rotation	Z Position with negative direction of rotation
16	5.625 °	45 ° ... 50.625 °	39.375 ° ... 45 °
12	7.5 °	45 ° ... 52.5 °	37.5 ° ... 45 °
10	9 °	45 ° ... 54 °	36 ° ... 45 °
8	11.25 °	39.375 ° ... 50.625 °	33.75 ° ... 45 °
5	18 °	36 ° ... 54 °	27 ° ... 45 °
4	22.5 °	33.75 ° ... 56.25 °	28.125 ° ... 50.625 °
3	30 °	30 ° ... 60 °	22.5 ° ... 52.5 °
2	45 °	22.5 .. 67.5 °	16.875 ° ... 61.875 °
1	90 °	0 ° ... 90 °	354.375 ° ... 84.625 °

Table 8: Index width and position (iC-NV)

INDEX WIDTH and POSITION of iC-NVH			
IPF	Z Width	Z Position with positive direction of rotation	Z Position with negative direction of rotation
16	11.25 °	45 ° ... 56.25 °	39.375 ° ... 50.625 °
12	15 °	45 ° ... 60 °	37.5 ° ... 52.5 °
10	18 °	45 ° ... 63 °	36 ° ... 54 °
8	22.5 °	39.375 ° ... 61.875 °	33.75 ° ... 56.25 °
5	36 °	36 ° ... 72 °	27 ° ... 63 °
4	45 °	33.75 ° ... 78.75 °	28.125 ° ... 73.125 °
3	60 °	30 ° ... 90 °	22.5 ° ... 82.5 °
2	90 °	22.5 .. 112.5 °	16.875,° ... 106.875 °
1	180 °	0 ° ... 180 °	354.375 ° ... 174.625 °

Table 9: Index width and position (iC-NVH)

Oscilloscope diagrams

The following diagrams give the input and output signals for various directions of rotation and ROT settings for interpolation factors 1 and 16.

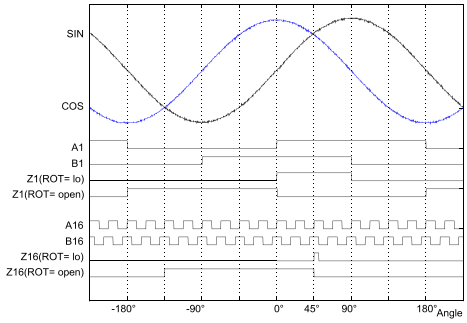


Figure 9: iC-NV: ROT= lo/open, COS leading SIN

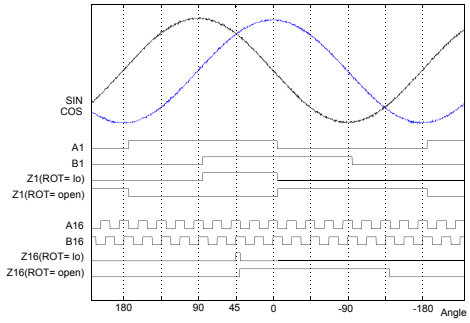


Figure 10: iC-NV: ROT= lo/open, SIN leading COS

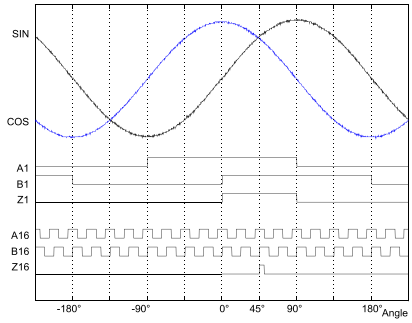


Figure 11: iC-NV: ROT= hi, COS leading SIN

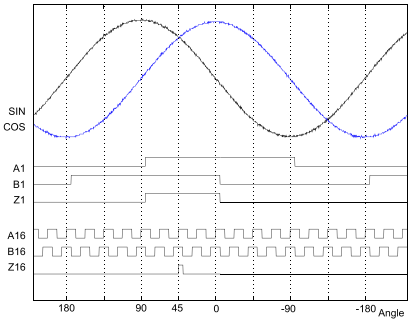


Figure 12: iC-NV: ROT= hi, SIN leading COS

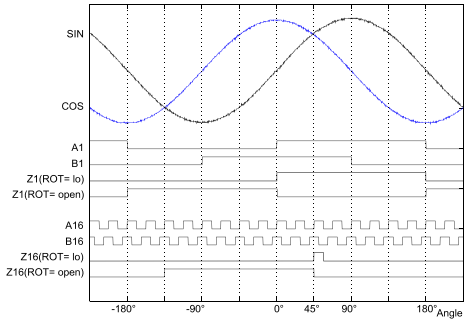


Figure 13: iC-NVH: ROT= lo/open, COS leading SIN

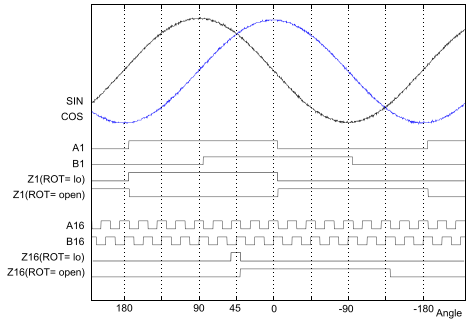


Figure 14: iC-NVH: ROT= lo/open, SIN leading COS

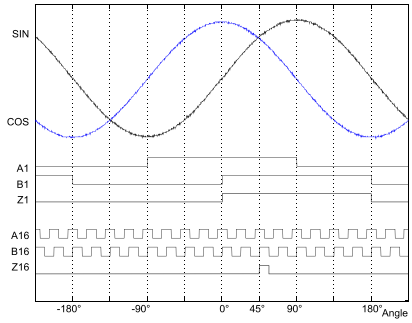


Figure 15: iC-NVH: ROT= hi, COS leading SIN

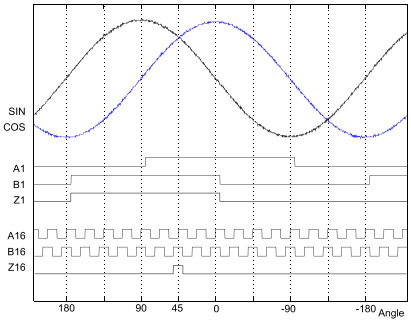


Figure 16: iC-NVH: ROT= hi, SIN leading COS

TEST FUNCTIONS

Device iC-NV features internal test functions which can be used to ease sensor bridge calibration procedures if such are required. To enable test operation, a threshold current of approx. 1 mA present at pin RCLK must be exceeded during power up. Subsequently, four different test modes are selectable starting with mode 3 set initially.

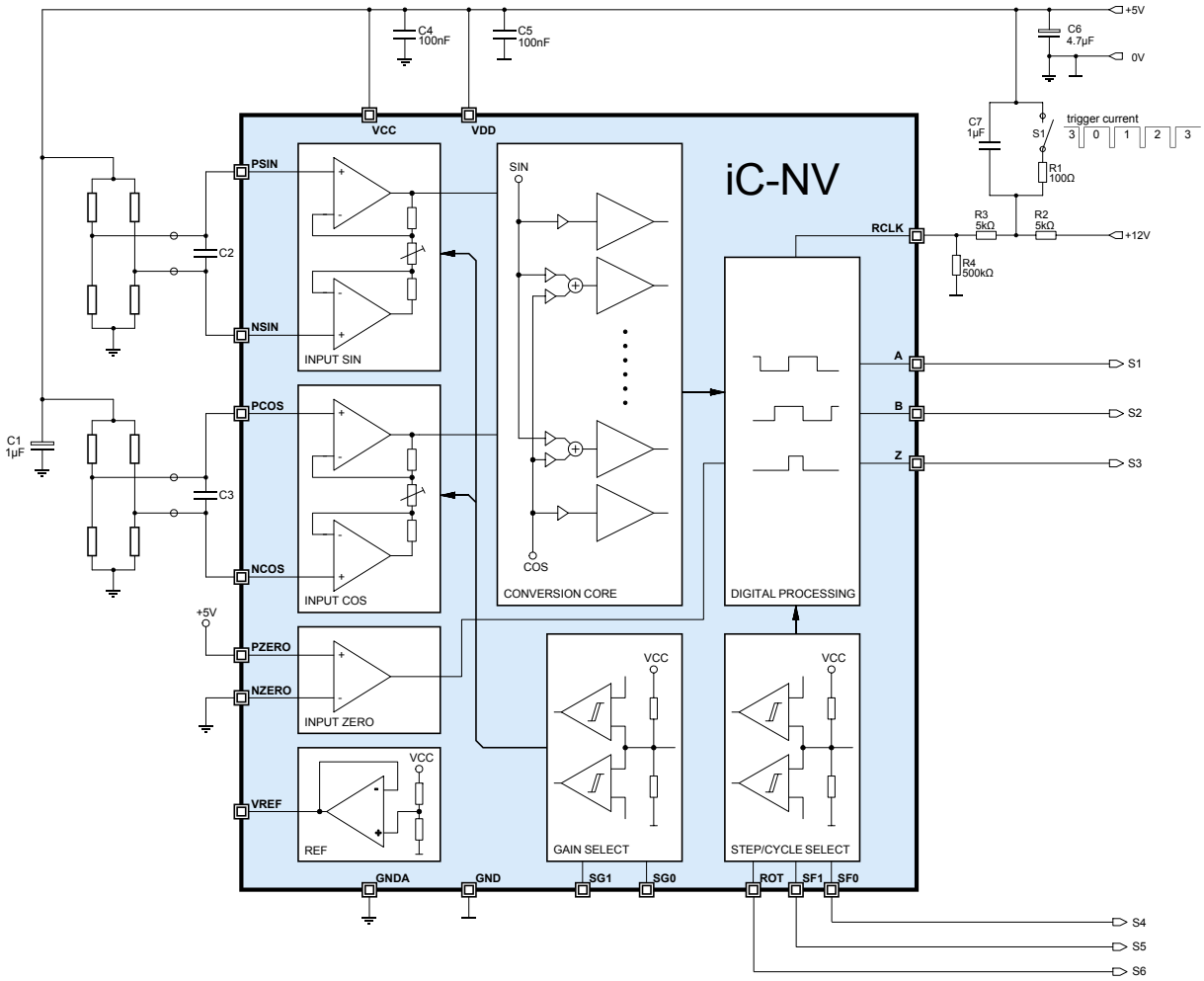


Figure 17: Activating test functions via pin RCLK.

Description of test signals

Test Signal	Description
Mode 3	
ZK	Un-gated index/zero comparator output
EXKA	All comparators EXOR-gated
SIN, NSIN, COS, NCOS	Amplifier outputs (signal valid with no load only)
Mode 0	
KA(0)	Comparator 0 ° – 180 ° → Duty cycle indicates offset of sine signal.
KA(16)	Comparator 90 ° – 270 ° → Duty cycle indicates offset of cosine signal.
KA(X) = KA(8) EXOR KA(24)	Comparator 45 ° – 225 ° → Duty cycle indicates amplitude ratio of sine/cosine signal. Offset calibration must be performed first.
Mode 1	
CLK, UP, DN	Control signals for external counters.
Mode 2	
NENOS, CLK, DALL	Test signals for iC-Haus device test.

Table 10: Test modes

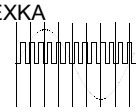
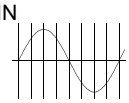
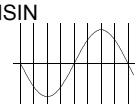
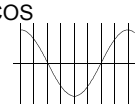
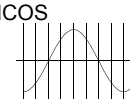
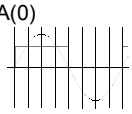
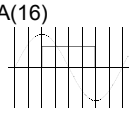
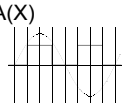
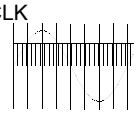
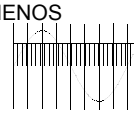
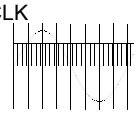
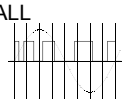
Test Mode	S1 (A)	S2 (B)	S3 (Z)	S4 (SF0)	S5 (SF1)	S6 (ROT)
Mode 3	ZK hi lo	EXKA 	SIN 	NSIN 	COS 	NCOS 
Mode 0	KA(0) 	KA(16) 	KA(X) 			
Mode 1	CLK 	UP hi lo	DN lo hi			
Mode 2	NENOS 	CLK 	DALL 			

Table 11: Illustration of output signals during test modes

APPLICATIONS INFORMATION

Principal Input Circuits

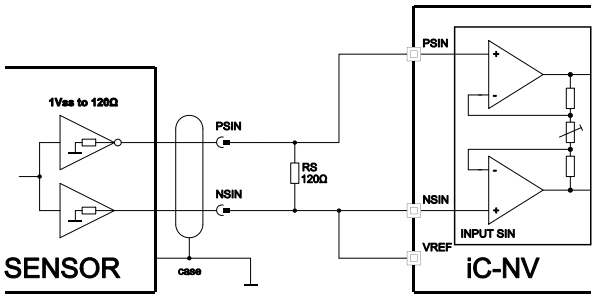


Figure 18: Input circuit for voltage signals of 1Vpp with no ground reference. When grounds are not separated the connection NSIN to VREF must be omitted.

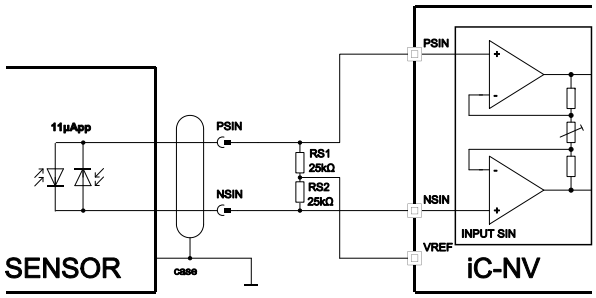


Figure 19: Input circuit for current signals of 11 µA. In this circuit offset adjustment is not possible.

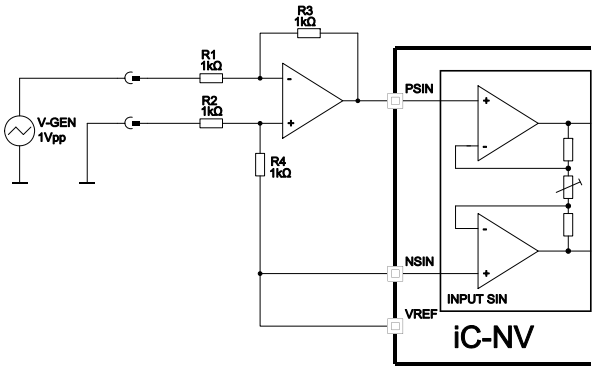


Figure 20: Input circuit for single-side voltage or current source signals with ground reference (adaptation via resistors R3, R4).

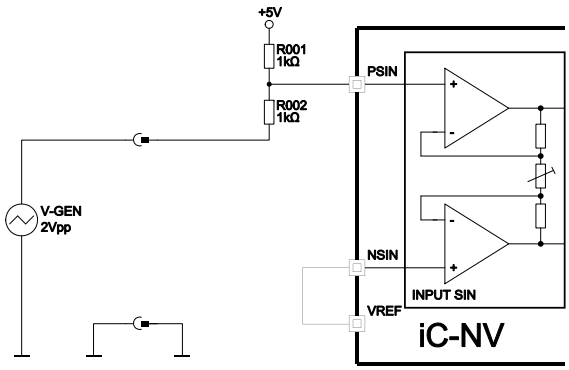


Figure 21: Simplified input wiring for single-side voltage signals with ground reference.

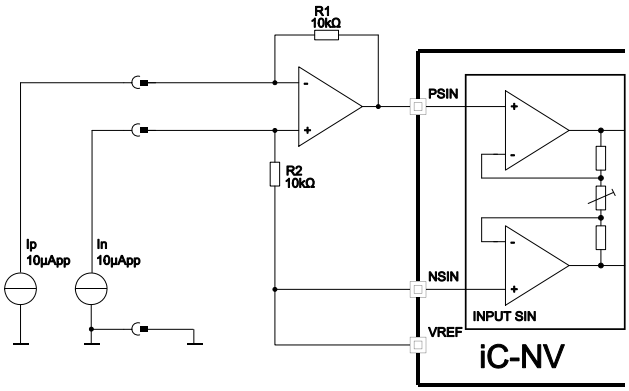


Figure 22: Input circuit for differential current sink sensor outputs, e.g. using Opto Encoder iC-WG.

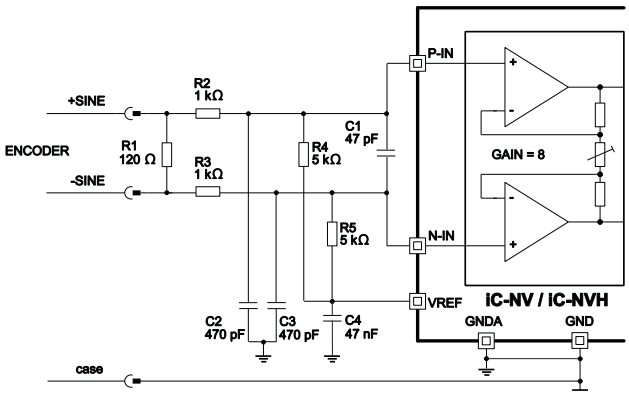


Figure 23: Input circuit for sine encoders (0.8 Vpp to 1.2 Vpp) with 120 Ω termination and low-pass filtering. R2/R3 serve as protection against ESD and transients, R4/R5 reduce the input signal to suit an input gain of 8.

Wiring photodiode arrays with common cathodes

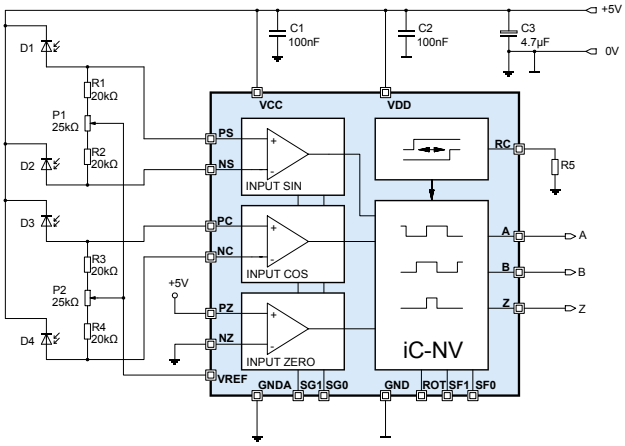


Figure 24: Wiring scheme with offset adjustment possibility; the resistor values must be selected with respect to the photo currents available (e.g. 65 kΩ for max. 16 µApk at GAIN = 3, or 1 µA at GAIN = 50 respectively).

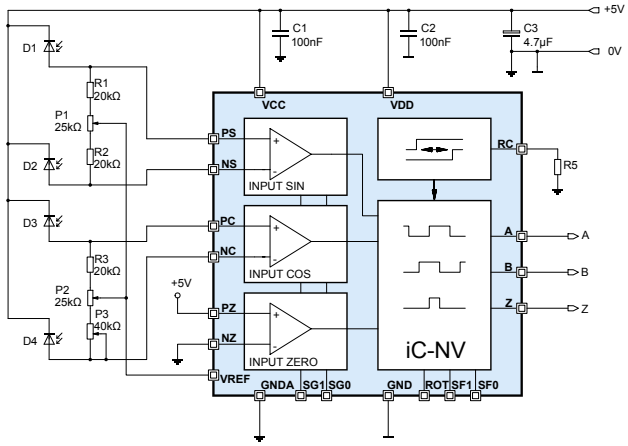


Figure 25: Additional adjustment possibility for amplitude differences; settings at P3 must be done first.

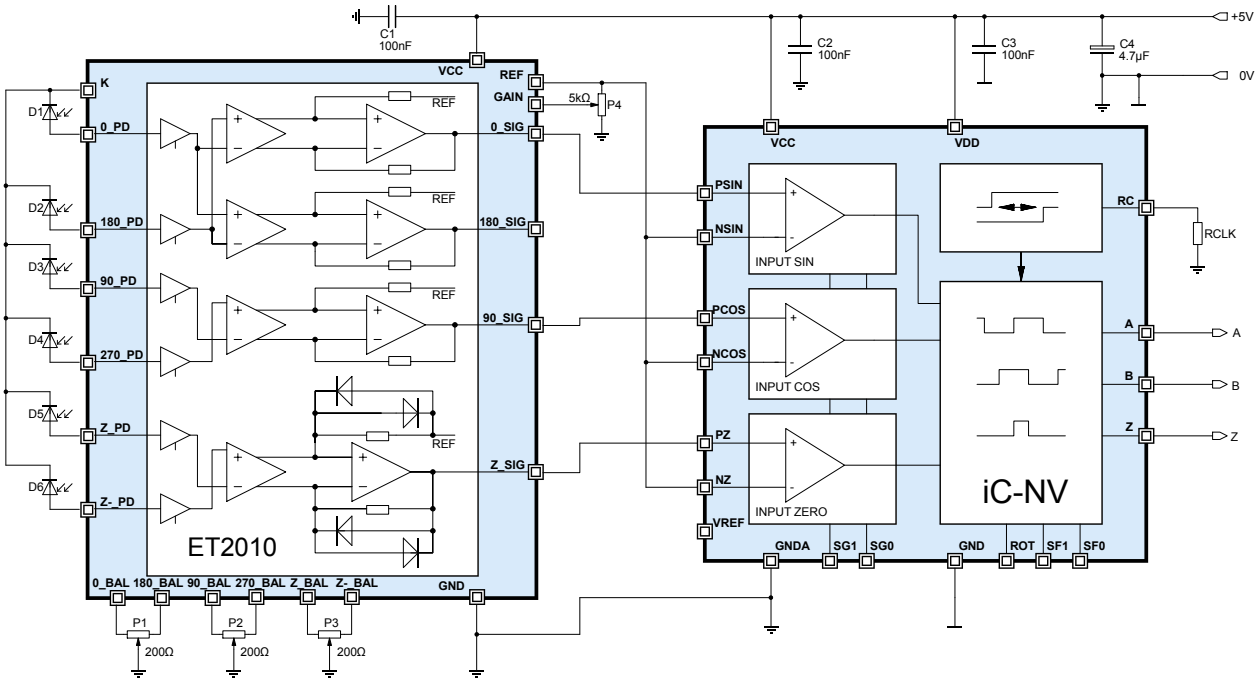


Figure 26: Photodiode scanning circuit using ET2010 pre-amp and adjustment device.

Wiring photodiode arrays with common anodes

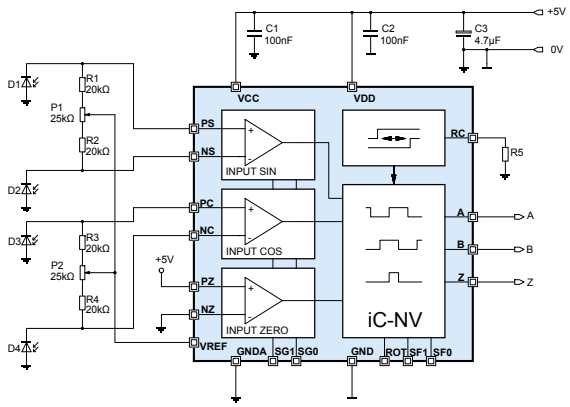


Figure 27: Wiring scheme with offset adjustment possibility; the resistor values must be selected with respect to the photo currents available (e.g. 65 kΩ for max. 16 µA pk at GAIN = 3, or 1 µA at GAIN = 50 respectively).

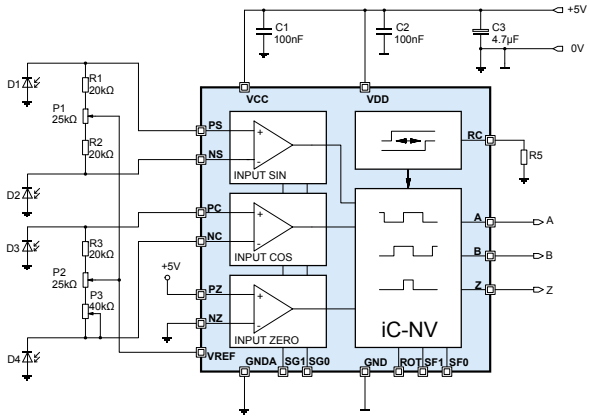


Figure 28: Additional adjustment possibility for amplitude differences; settings at P3 must be done first.

Wiring magneto-resistor bridge sensors

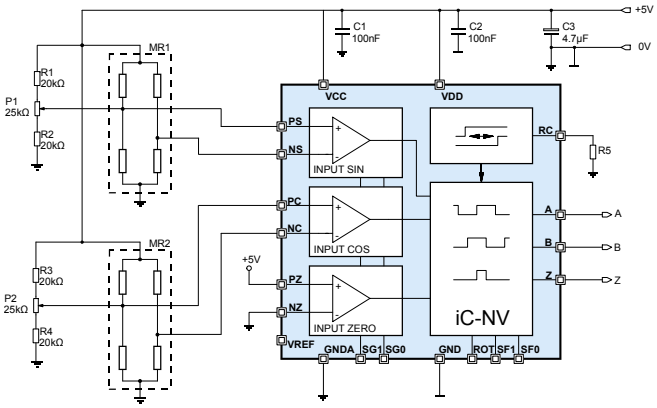


Figure 29: Wiring MR sensor bridges with offset adjustment possibility; setup pins remaining open can be linked to VREF to enhance interference immunity.

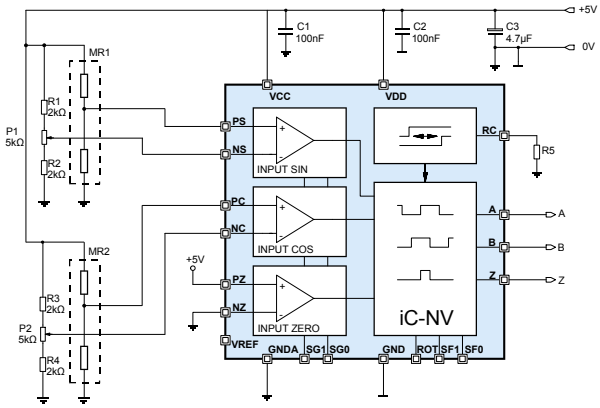


Figure 30: Wiring MR half-bridge sensors with offset adjustment possibility.

MR Sensor System Application Example

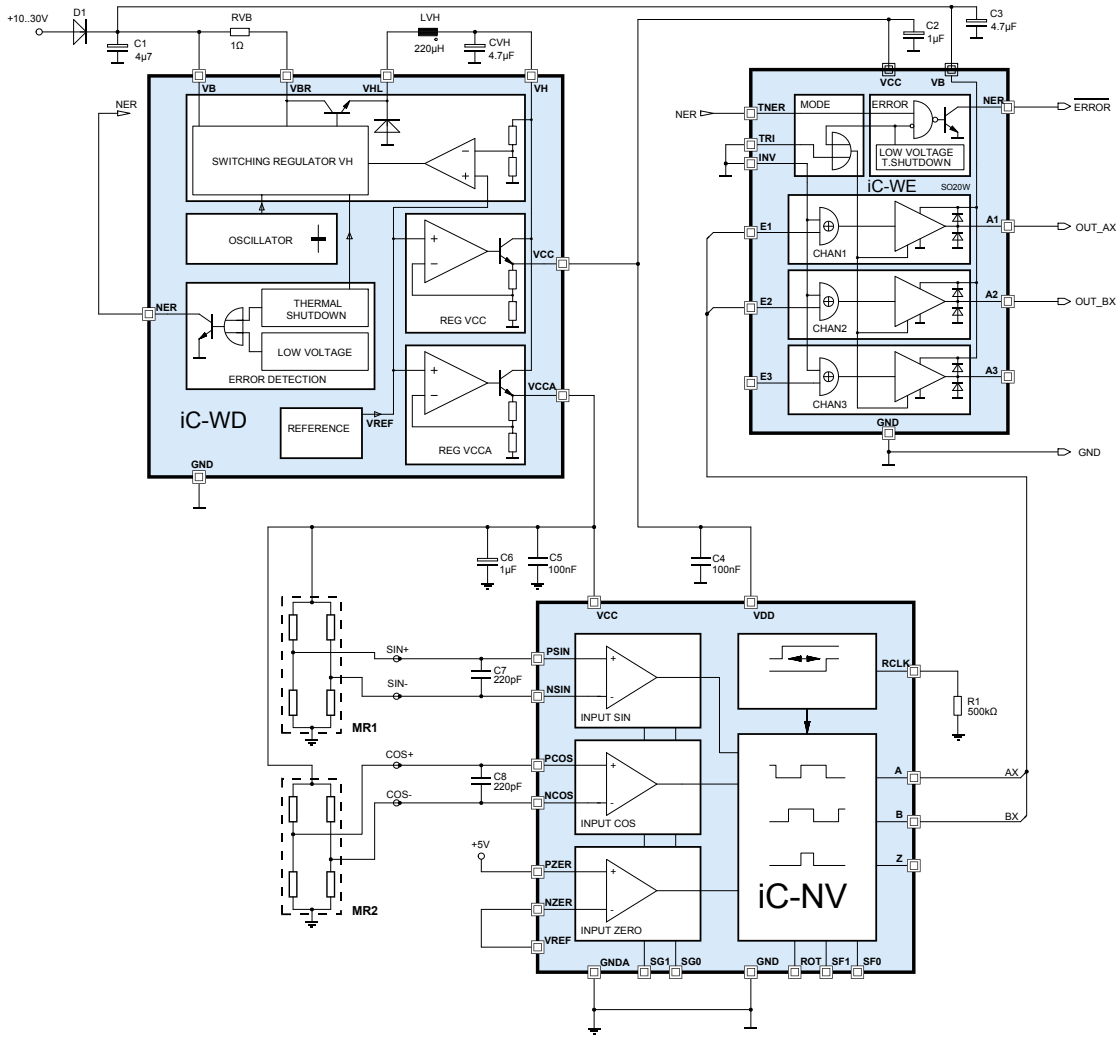


Figure 31: Complete MR sensor system for 24 V environment featuring low-noise switch-mode power supply linear regulator combo iC-WD and line driver iC-WE, enabling data transmission via 100 m cable length. The maximum output frequency is limited to approx. 280 kHz by R1 = 500 kΩ to comply with speed-limited external counters (pins SF1 and SF0 are open and select IPF = 5). C7/C8 can help to improve noise immunity additionally, for instance with motor applications.

EVALUATION BOARD

An evaluation board for iC-NV is available for test purposes. Figures 32, 33 and 34 show the wiring as well as the top and bottom layout of the test PCB.

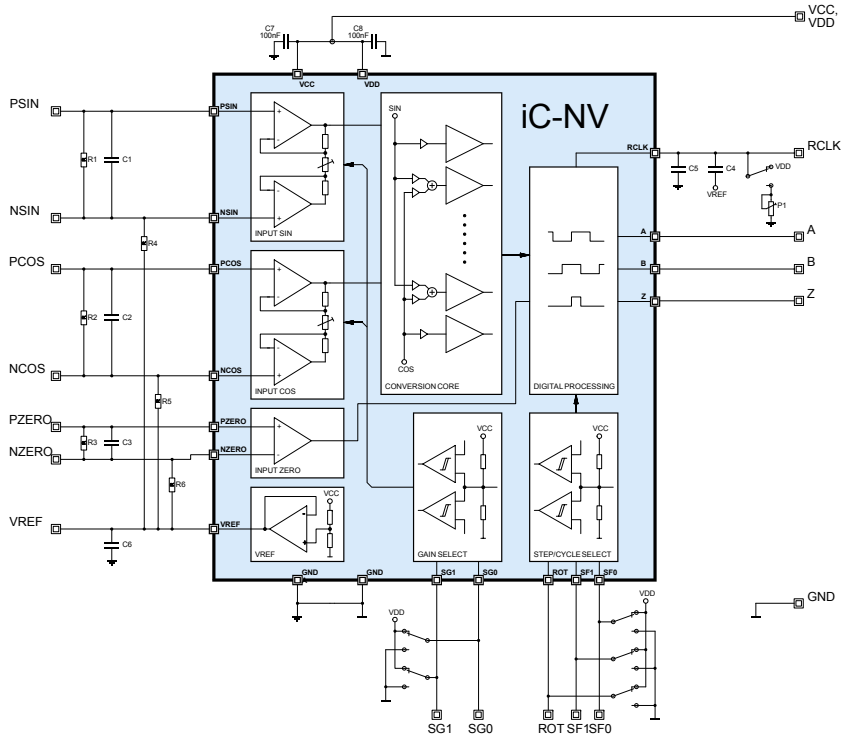


Figure 32: Circuit diagram of the evaluation board (pot P1 is not populated).

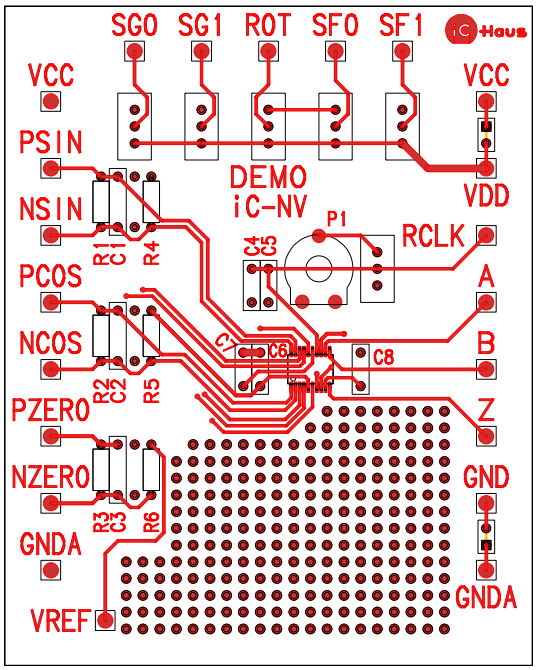


Figure 33: Evaluation board (component side)

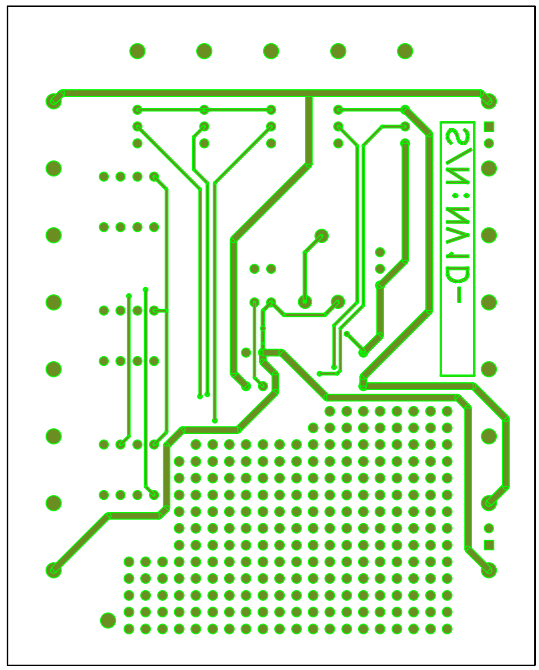


Figure 34: Evaluation board (bottom side

DESIGN REVIEW: Function Notes

iC-NV X1		
No.	Function, Parameter/Code	Description and Application Notes
		None at time of release.

Table 12: Notes on chip functions regarding iC-NV chip release X1.

iC-NVH 1		
No.	Function, Parameter/Code	Description and Application Notes
		None at time of release.

Table 13: Notes on chip functions regarding iC-NVH chip release 1.

REVISION HISTORY

Rel.	Rel. Date*	Chapter	Modification	Page
C1	2007-11-26		Release 2007	

Rel.	Rel. Date*	Chapter	Modification	Page
D1	2009-01-12	ABSOLUTE MAXIMUM RATINGS	Item G003: Symbol name Items G009, EG01: update of conditions Item TG2: max. storage temperature 150 °C	3
		DESCRIPTION OF FUNCTIONS	Table Index Position renamed to Index Position Column added for ZWIDTH Subtitle changed	9
		Disclaimer	Text update	12

Rel.	Rel. Date*	Chapter	Modification	Page
E1	2019-09-20	All	General update, inclusion of iC-NVH	all
		ABSOLUTE MAXIMUM RATINGS	G012 moved to Thermal Data T02	6
		DESCRIPTION OF FUNCTIONS	Section Hysteresis: description updated Section Zero Pulse: description added for iC-NVH (Z position values corrected) Section Oscilloscope Diagrams: figures added for iC-NVH	11, 12, 13
		APPLICATIONS INFORMATION	Figure 23 added	16
		DESIGN REVIEW: Function Notes	Section added	21

* Release Date format: *YYYY-MM-DD*

ORDERING INFORMATION

Type	Package	Options	Order Designation
iC-NV	20-pin TSSOP, 4.4 mm RoHS compliant	index length 90 ° (AB-gated to 1/4 T)	iC-NV TSSOP20
		operating temperature range -40 °C to +125 °C	iC-NV TSSOP20 ET -40/125
iC-NVH	20-pin TSSOP, 4.4 mm RoHS compliant	index length 180 ° (A-gated to 1/2 T)	iC-NVH TSSOP20
		operating temperature range -40 °C to +125 °C	iC-NVH TSSOP20 ET -40/125
Evaluation Board iC-NV	PCB, size approx. 80 mm x 100 mm		iC-NV EVAL NV1D

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E-Mail: dispo@ichaus.com

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