

# iC-MQ PROGRAMMABLE 9-BIT Sin/Cos INTERPOLATION IC WITH RS422 DRIVER



Rev F4, Page 1/46

## FEATURES

- ◆ Latency-free sine-to-digital conversion to 400 angle steps
- ◆ 500 kHz input frequency for interpolation factors of x1 and x2 (10 kHz for x100)
- ◆ Flexible pin assignment due to signal path multiplexers
- ◆ PGA inputs for differential and single-ended signals
- ◆ Variable input resistance for current/voltage conversion
- ◆ Signal conditioning for offset, amplitude and phase
- ◆ Controlled 50 mA current source for LED or MR sensor supply
- ◆ Fault-tolerant RS422 outputs with 50 mA sink/source drive current
- ◆ Preselectable minimum phase distance for spike-proof counter stimulus
- ◆ Zero signal conditioning and electronic index pulse generation
- ◆ Signal and operation monitoring with configurable alarm output, output shutdown and error storage
- ◆ I<sup>2</sup>C multimaster interface for in-circuit calibration and parameters (EEPROM)
- ◆ Adjustable overtemperature alarm and shutdown
- ◆ Supply from 4.3 to 5.5 V, operation from -25(-40) to +100 °C
- ◆ Reverse-polarity-proof including the sub-system

## APPLICATIONS

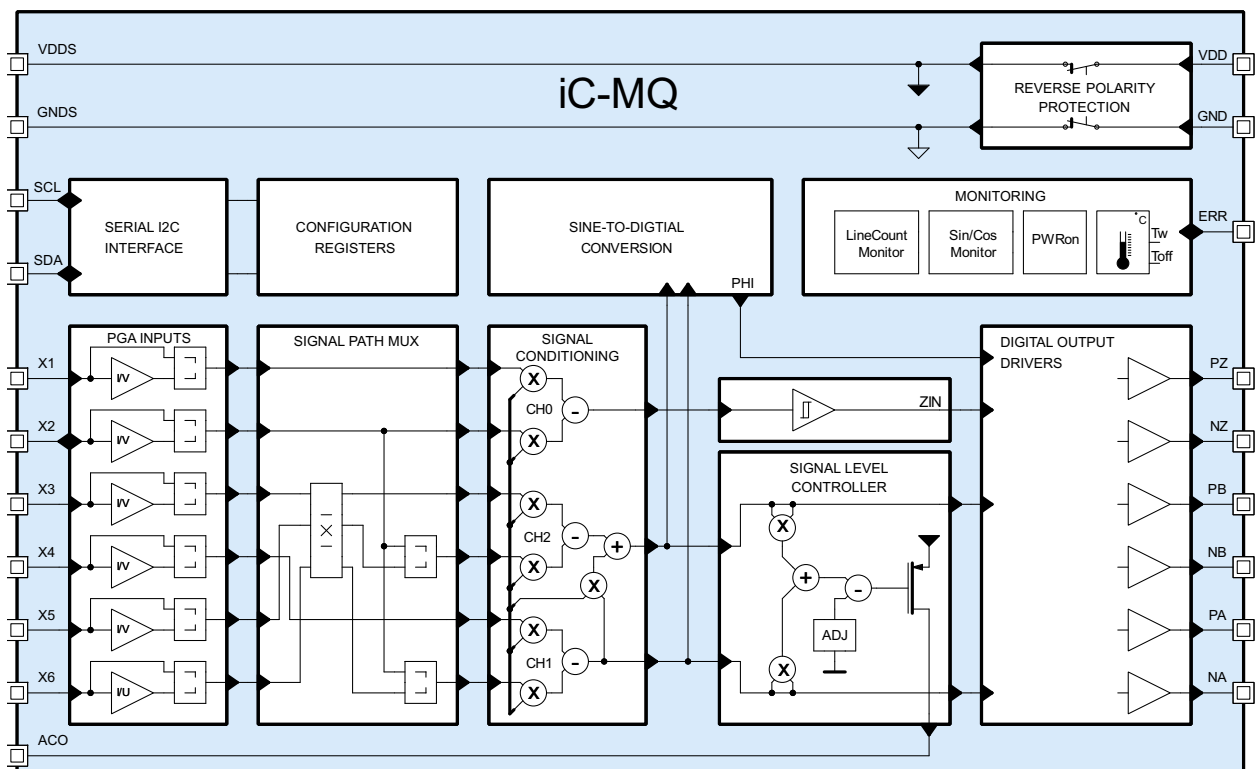
- ◆ Optical and magnetic position sensors
- ◆ Angle encoders
- ◆ Linear scales

## PACKAGES



TSSOP20  
RoHS compliant

## BLOCK DIAGRAM



## DESCRIPTION

Interpolator iC-MQ is a non-linear A/D converter which digitizes sine/cosine sensor signals using a count-safe tracking conversion principle with selectable resolution and hysteresis. The angle resolution per sine period can be set using SELRES; up to 400 angle steps are possible (see page 28).

The angle position is output incrementally by differential RS422 drivers as an encoder quadrature signal with a zero pulse or, if selected, as a counter signal for devices compatible with 74HC191 or 74HC193. The zero pulse is generated electronically when an enable has been set by the X1/X2 inputs. This pulse can be configured extensively: both in its relative position to the input signal with regard to the logic gating with A and/or B and in its width from 90° to 360° (1/4 to 1 T).

A preselectable minimum transition distance permits glitch-free output signals and prevents counting errors which in turn boosts the noise immunity of the position encoder.

Programmable instrumentation amplifiers with selectable gain levels allow differential or single-ended, referenced input signals; via input X2 the external reference can be used as reference voltage for the offset correction.

The modes of operation differentiate between high impedance (V modes) and low impedance (I modes). This adaptation of the iC to voltage or current signals enables MR sensor bridges or photosensors to be directly connected up to the device. The optical scanning of low resolution code discs is also supported by the reference function of input X2; these discs do not evaluate tracks differentially but in comparison with a reference photodiode.

The integrated signal conditioning unit allows signal amplitudes and offset voltages to be calibrated accurately and also any phase error between the sine and cosine signals to be corrected. The channel for the zero signal can be configured separately.

A control signal is generated from the conditioned signals which can track the transmitting LED of optical encoders via the integrated 50 mA driver stage (output ACO). If MR sensors are connected this driver stage can also track the power supply of the measuring bridges. By tracking the sensor energy supply any temperature and aging effects are compensated for, the input signals stabilized and the exact calibration of the input signals is maintained. This enables a

constant accuracy of the interpolation circuit across the entire operating temperature range.

When control limits are reached, these can be indicated at the maskable error pin ERR. Faults such as overdrive, wire breakage, short circuiting, dirt or aging, for example, are logged.

iC-MQ includes extensive self-test and system diagnosis functions which check whether the sensor is working properly or not. For all error events the user can select whether the fault be displayed at error pin ERR or the outputs shutdown. At the same time errors can be stored in the EEPROM to enable failures to be diagnosed at a later stage. For encoder applications the line count of the code disc, the sensor signal regarding signal level and frequency and the operating temperature can be monitored, for example, the latter using an adjustable on-chip sensor.

Display error pin ERR is bidirectional; a system fault recognized externally can be recorded and also registered in the error memory.

iC-MQ is protected against reverse polarity and offers its monitored supply voltage to the external circuit, thus extending the protection to the system (for load currents to 20 mA). Reverse polarity protection also covers the short-circuit-proof line drivers so that an unintentional faulty wiring during initial operation is tolerated.

On being activated the device configuration is loaded via the serial configuration interface from an external EEPROM and verified by a CRC. A microcontroller can also configure iC-MQ; the implemented interface is multimaster-competent and enables direct RAM access.

### General notice on application-specific programming

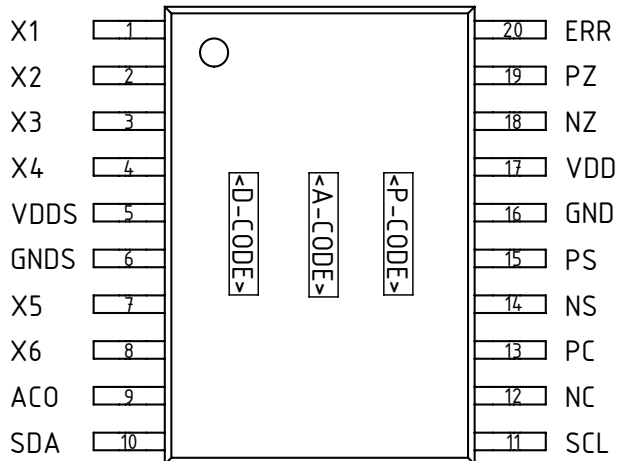
Parameters defined in the datasheet represent supplier's attentive tests and validations, but - by principle - do not imply any warranty or guarantee as to their accuracy, completeness or correctness under all application conditions. In particular, setup conditions, register settings and power-up have to be thoroughly validated by the user within his specific application environment and requirements (system responsibility).

For magnetic sensor systems: The chip's performance in application is impacted by system conditions like the quality of the magnetic target, field strength and stray fields, temperature and mechanical stress, sensor alignment and initial calibration. For optical sensor systems: The chip's performance in application is impacted by system conditions like the quality of the optical target, the illumination, temperature and mechanical stress, sensor alignment and initial calibration.

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**PACKAGING INFORMATION**

**PIN CONFIGURATION TSSOP20**



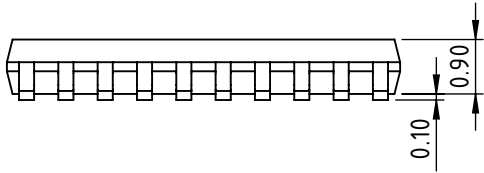
**PIN FUNCTIONS**

| No. | Name              | Function  |
|-----|-------------------|---|
| 1   | X1                | Signal Input 1 (Index +)  |
| 2   | X2                | Signal Input 2 (Index -)  |
| 3   | X3                | Signal Input 3  |
| 4   | X4                | Signal Input 4  |
| 5   | VDDS <sup>1</sup> | Switched Supply Output and Internal Analog Supply Voltage (reverse-polarity-proof, load 20 mA max.) |
| 6   | GNDS <sup>1</sup> | Switched Ground (reverse-polarity-proof)  |
| 7   | X5                | Signal Input 5  |
| 8   | X6                | Signal Input 6  |
| 9   | ACO               | Signal Level Controller, high-side current source output  |
| 10  | SDA               | Serial Configuration Interface, data line   |
| 11  | SCL               | Serial Configuration Interface, clock line  |
| 12  | NB                | Incremental Output B-   |
| 13  | PB                | Incremental Output B+   |
| 14  | NA                | Incremental Output A-   |
| 15  | PA                | Incremental Output A+   |
| 16  | GND               | Ground  |
| 17  | VDD               | +4.3...5.5 V Supply Voltage   |
| 18  | NZ                | Incremental Output Z-   |
| 19  | PZ                | Incremental Output Z+   |
| 20  | ERR               | Error Signal (In/Out) / Test Mode Trigger Input   |

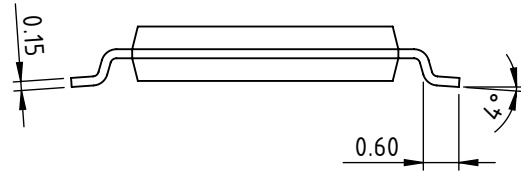
IC top marking: <P-CODE> = product code, <A-CODE> = assembly code (subject to changes), <D-CODE> = date code (subject to changes);  
<sup>1</sup> It is advisable to connect a bypass capacitor of about 100 nF (up to 1 µF max.) close to the chip's analog supply terminals.

**PACKAGE DIMENSIONS TSSOP20**

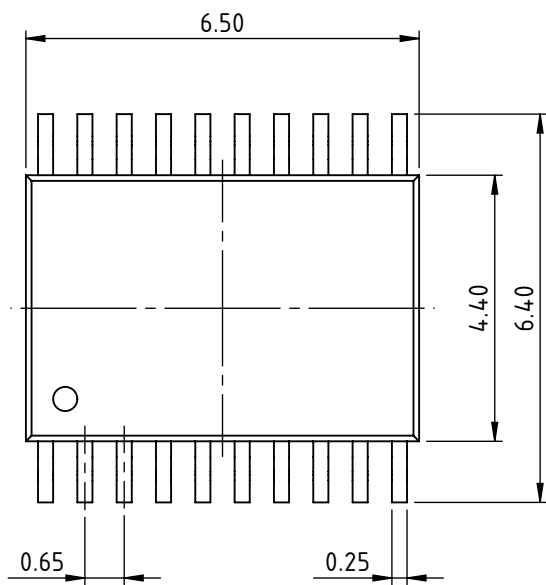
SIDE



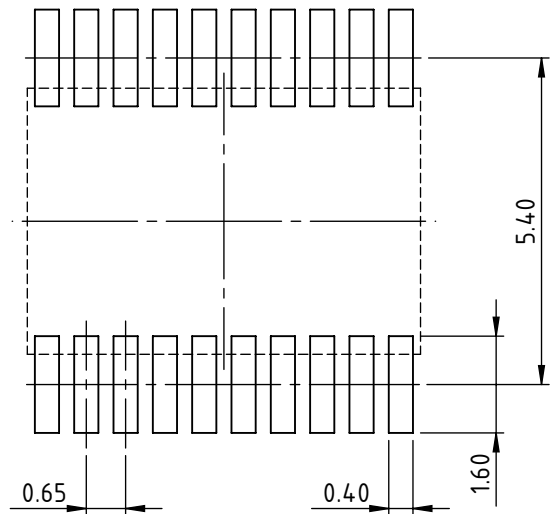
FRONT



TOP



RECOMMENDED PCB-FOOTPRINT



All dimensions given in mm.  
Tolerances of form and position according to JEDEC MO-153

### ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these ratings device damage may occur.

| Item No. | Symbol           | Parameter                                   | Conditions                           | Limits |                        | Unit |
|----------|------------------|---|--------------------------------------|--------|------------------------|------|
|          |                  |   |                                      | Min.   | Max.                   |      |
| G001     | V()              | Voltage at VDD, PA, NA, PB, NB, PZ, NZ, ACO |                                      | -6     | 6                      | V    |
| G002     | V()              | Voltage at ERR                              |                                      | -6     | 8                      | V    |
| G003     | V()              | Pin-Pin Voltage                             |                                      |        | 6                      | V    |
| G004     | V()              | Voltage at X1...X6, SCL, SDA                |                                      | -0.3   | V <sub>DDS</sub> + 0.3 | V    |
| G005     | I(VDD)           | Current in VDD                              |                                      | -20    | 400                    | mA   |
| G006     | I()              | Current in V <sub>DDS</sub> , GNDS          |                                      | -50    | 50                     | mA   |
| G007     | I()              | Current in X1...X6, SCL, SDA, ERR           |                                      | -20    | 20                     | mA   |
| G008     | I()              | Current in PA, NA, PB, NB, PZ, NZ           |                                      | -100   | 100                    | mA   |
| G009     | I(ACO)           | Current in ACO                              |                                      | -100   | 20                     | mA   |
| G010     | Vd()             | ESD Susceptibility at all pins              | HBM 100 pF discharged through 1.5 kΩ |        | 2                      | kV   |
| G011     | P <sub>tot</sub> | Permissible Power Dissipation               |                                      |        | 300                    | mW   |
| G012     | T <sub>J</sub>   | Junction Temperature                        |                                      | -40    | 150                    | °C   |
| G013     | T <sub>s</sub>   | Storage Temperature                         |                                      | -40    | 150                    | °C   |

### THERMAL DATA

| Item No. | Symbol            | Parameter   | Conditions | Limits |      |      | Unit |
|----------|-------------------|---|------------|--------|------|------|------|
|          |                   |   |            | Min.   | Typ. | Max. |      |
| T01      | T <sub>a</sub>    | Operating Ambient Temperature Range (extended range to -40 °C on request) |            | -25    |      | 100  | °C   |
| T02      | R <sub>thja</sub> | Thermal Resistance Chip to Ambient  |            |        | 80   |      | K/W  |

All voltages are referenced to pin GNDS unless otherwise stated.

All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

## ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 4.3...5.5 V, Tj = -40 °C...125 °C, IBN calibrated to 200 µA, unless otherwise stated

| Item No.  | Symbol    | Parameter                                      | Conditions   |                                |                                |                                | Unit                         |
|---|-----------|--|--|--------------------------------|--------------------------------|--------------------------------|------------------------------|
|   |           |  |  | Min.                           | Typ.                           | Max.                           |                              |
| <b>Total Device</b>   |           |  |  |                                |                                |                                |                              |
| 001   | V(VDD)    | Permissible Supply Voltage                     | Load current I(VDDS) to 10 mA<br>Load current I(VDDS) to 20 mA   | 4.3<br>4.5                     |                                | 5.5<br>5.5                     | V<br>V                       |
| 002   | I(VDD)    | Supply Current                                 | Tj = -40...125 °C, no load<br>Tj = 27 °C, no load  |                                | 12                             | 25                             | mA<br>mA                     |
| 003   | I(VDDS)   | Permissible Load Current VDDS                  |  | -20                            |                                | 0                              | mA                           |
| 004   | Vcz(hi)   | Clamp-Voltage hi at all pins                   |  |                                |                                | 11                             | V                            |
| 005   | Vc(hi)    | Clamp-Voltage hi at Inputs SCL, SDA            | Vc(hi) = V() - V(VDD), I() = 1 mA  | 0.4                            |                                | 1.5                            | V                            |
| 006   | Vc(hi)    | Clamp-Voltage hi at Inputs X1...X6             | Vc(hi) = V() - V(VDD), I() = 4 mA  | 0.3                            |                                | 1.2                            | V                            |
| 007   | Vc(lo)    | Clamp-Voltage lo at all pins                   | I() = -4 mA  | -1.2                           |                                | -0.3                           | V                            |
| 008   | Irev(VDD) | Reverse-Polarity Current VDD vs. GND           | V(VDD) = -5.5V...-4.3 V  | -1                             |                                | 1                              | mA                           |
| <b>Signal Conditioning, Inputs X1...X6 (CH1, CH2: i = 12, CH0: I = 0)</b> |           |  |  |                                |                                |                                |                              |
| 101   | Vin(sig)  | Permissible Input Voltage Range                | RINi() = 0x01<br>RINi() = 0x09   | 0.75<br>0                      |                                | VDDS<br>- 1.5<br>VDDS          | V<br>V                       |
| 102   | Iin(sig)  | Permissible Input Current Range                | RINi(0) = 0; BIASi = 0<br>RINi(0) = 0; BIASi = 1   | -300<br>10                     |                                | -10<br>300                     | µA<br>µA                     |
| 103   | Iin()     | Input Current                                  | RINi() = 0x01  | -10                            |                                | 10                             | µA                           |
| 104   | Rin()     | Input Resistance vs. VREFin                    | Tj = 27 °C;<br>RINi(3:0) = 0x09<br>RINi(3:0) = 0x00<br>RINi(3:0) = 0x02<br>RINi(3:0) = 0x04<br>RINi(3:0) = 0x06                            | 16<br>1.1<br>1.6<br>2.2<br>3.2 | 20<br>1.6<br>2.3<br>3.2<br>4.6 | 24<br>2.1<br>3.0<br>4.2<br>6.0 | kΩ<br>kΩ<br>kΩ<br>kΩ<br>kΩ   |
| 105   | TC(Rin)   | Temperature Coefficient of Rin                 |  |                                | 0.15                           |                                | %/K                          |
| 106   | VREFin()  | Reference Voltages VREFin0, VREFin12           | RINi(0) = 0, BIASi = 1<br>RINi(0) = 0, BIASi = 0   | 1.35<br>2.25                   | 1.5<br>2.5                     | 1.65<br>2.75                   | V<br>V                       |
| 107   | G0, G12   | Selectable Gain Factors                        | RINi(3) = 0, GRi and GFi = 0x0<br>RINi(3) = 0, GRi and GFi = max.<br><br>RINi(3) = 1, GRi and GFi = 0x0<br>RINi(3) = 1, GRi and GFi = max. |                                | 2<br>100<br><br>0.5<br>25      |                                |                              |
| 108   | Gdiff     | Relative Gain Ratio CH1 vs. CH2                | GF2 = 0x10, GF1 = 0x0<br>GF2 = 0x10, GF1 = 0x7F  |                                | 39<br>255                      |                                | %<br>%                       |
| 109   | ΔG        | Step Width Of Fine Gain Adjustment             | for CH0<br>for CH1<br>for CH2  |                                | 1.06<br>1.015<br>1.06          |                                |                              |
| 110   | INL(Gi)   | Integral Linearity Error of Gain Adjustment    |  | -1.06                          |                                | 1.06                           |                              |
| 111   | Vin()diff | Recommended Differential Input Voltage         | Vin()diff = V(PCHx) - V(NCHx);<br>RINi(3) = 0<br>RINi(3) = 1   | 10<br>40                       |                                | 500<br>2000                    | mVpp<br>mVpp                 |
| 112   | Vin(os)   | Input Offset Voltage                           | referred to side of input  |                                | 25                             |                                | µV                           |
| 113   | VOScal    | Offset Calibration Range                       | referenced to the selected source (VOS0 resp. VOS12), mode <i>Calibration 2</i> ;<br>ORi = 00<br>ORi = 01<br>ORi = 10<br>ORi = 11          |                                | ±100<br>±200<br>±600<br>±1200  |                                | %V()<br>%V()<br>%V()<br>%V() |
| 114   | ΔOF0      | CH0 Offset Calibration Step Width              | referenced to the selected source VOS0;<br>OR0 = 0x0   |                                | 3.2                            |                                | %                            |
| 115   | ΔOF12     | CH1/2 Offset Calibration Step Width            | referenced to the selected source VOS12;<br>OR12 = 0x0   |                                | 0.79                           |                                | %                            |
| 116   | INL(OFi)  | Integral Linearity Error of Offset Calibration | limited test coverage (guaranteed by design)   | -5                             |                                | 5                              | LSB                          |

**ELECTRICAL CHARACTERISTICS**

Operating Conditions: VDD = 4.3...5.5 V, Tj = -40 °C...125 °C, IBN calibrated to 200 µA, unless otherwise stated

| Item No.  | Symbol     | Parameter                                     | Conditions  | Min.                     | Typ.  | Max.                     | Unit                 |
|---|------------|---|---|--------------------------|-------|--------------------------|----------------------|
|   |            |   |   |                          |       |                          |                      |
| 117   | PHI12      | Phase Error Calibration Range                 | CH1 vs. CH2   |                          | ±20.2 |                          | °                    |
| 118   | ΔPHI12     | Phase Error Calibration Step Width            |   |                          | 0.63  |                          | °                    |
| 119   | INL(PHI12) | Integral Linearity Error of Phase Calibration | limited test coverage (guaranteed by design)  | -0.8                     |       | 0.8                      | °                    |
| 120   | fin()      | Permissible Maximum Input Freq.               | analog signal path;<br>with interpolation of x1, x2   | 200<br>500               |       |                          | kHz<br>kHz           |
| 121   | Vout(X2)   | Output Voltage at X2                          | BIASEX = 10, I(X2) = 0, referenced to VRE-Fin12   | 95                       | 100   | 105                      | %                    |
| 122   | Vin(X2)    | Permissible Input Voltage Range at X2         | BIASEX = 11   | 0.5                      |       | VDDS<br>- 2              | V                    |
| 123   | Rin(X2)    | Input Resistance at X2                        | BIASEX = 11, RIN0(3:0) = 0x01, RIN12(3:0) = 0x01  | 20                       | 27    | 35                       | kΩ                   |
| <b>Sine-To-Digital Conversion</b>                 |            |   |   |                          |       |                          |                      |
| 201   | AAabs      | Absolute Angle Accuracy                       | referenced to 360° input signal, ideal waveform, quasi static signals, adjusted signal conditioning, SELHYS = 0   |                          | 0.9   | 1.8                      | °                    |
| 202   | AArel      | Relative Angle Accuracy                       | referenced to output period T (see Fig. 1), ideal waveform, quasi static signals;<br>at 4 edges per period<br>at 100 edges per period<br>at 384 edges per period<br>at 400 edges per period |                          | <0.5  | 10<br>10<br>10<br>10     | %<br>%<br>%<br>%     |
| 203   | AAR        | Repeatability                                 | see 201; VDD = const., Tj = const.  |                          | 0.1   |                          | °                    |
| <b>Line Driver Outputs PA, NA, PB, NB, PZ, NZ</b> |            |   |   |                          |       |                          |                      |
| 501   | Vs()hi     | Saturation Voltage hi                         | Vs()hi = VDD - V();<br>SIK(1:0) = 00, I() = -1.2 mA<br>SIK(1:0) = 01, I() = -4 mA<br>SIK(1:0) = 10, I() = -20 mA<br>SIK(1:0) = 11, I() = -50 mA   |                          |       | 200<br>200<br>400<br>700 | mV<br>mV<br>mV<br>mV |
| 502   | Vs()lo     | Saturation Voltage lo                         | SIK(1:0) = 00, I() = 1.2 mA<br>SIK(1:0) = 01, I() = 4 mA<br>SIK(1:0) = 10, I() = 20 mA<br>SIK(1:0) = 11, I() = 50 mA  |                          |       | 200<br>200<br>400<br>700 | mV<br>mV<br>mV<br>mV |
| 503   | Isc()hi    | Short-Circuit Current hi                      | V() = 0 V;<br>SIK(1:0) = 00<br>SIK(1:0) = 01<br>SIK(1:0) = 10<br>SIK(1:0) = 11  | -4<br>-12<br>-60<br>-150 |       | -1.2<br>-4<br>-20<br>-50 | mA<br>mA<br>mA<br>mA |
| 504   | Isc()lo    | Short-Circuit Current lo                      | V() = VDD;<br>SIK(1:0) = 00<br>SIK(1:0) = 01<br>SIK(1:0) = 10<br>SIK(1:0) = 11  | 1.2<br>4<br>20<br>50     |       | 4<br>12<br>60<br>150     | mA<br>mA<br>mA<br>mA |
| 505   | tr()       | Rise Time                                     | RL = 100 Ω to GND;<br>SSR(1:0) = 00<br>SSR(1:0) = 01<br>SSR(1:0) = 10<br>SSR(1:0) = 11  | 5<br>5<br>20<br>50       |       | 20<br>40<br>140<br>350   | ns<br>ns<br>ns<br>ns |
| 506   | tf()       | Fall Time                                     | RL = 100 Ω to VDD;<br>SSR(1:0) = 00<br>SSR(1:0) = 01<br>SSR(1:0) = 10<br>SSR(1:0) = 11  | 5<br>5<br>30<br>50       |       | 20<br>40<br>140<br>350   | ns<br>ns<br>ns<br>ns |
| 507   | Iik()tri   | Leakage Current                               | TRIH1(1:0) = 11 (tristate)  |                          | 20    | 100                      | µA                   |
| 508   | Iik()rev   | Leakage Current                               | reversed supply voltage   |                          | 100   |                          | µA                   |
| 509   | Rin()cal   | Test Signal Source Impedance                  | Op. modes <i>Calibration 1, 2, 3</i>  |                          | 2.5   | 4                        | kΩ                   |
| 510   | I()cal     | Permissible Test Signal Load                  | Op. modes <i>Calibration 1, 2, 3</i>  | -3                       |       | 3                        | µA                   |



## ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 4.3...5.5 V, Tj = -40 °C...125 °C, IBN calibrated to 200 µA, unless otherwise stated

| Item No.  | Symbol           | Parameter  | Conditions   | Min.                      | Typ.       | Max.                    | Unit                 |
|---|------------------|--|--|---------------------------|------------|-------------------------|----------------------|
|   |                  |  |  |                           |            |                         |                      |
| 511   | tclk()lo         | Clock Signal Low-Pulse Duration for CP, CPD, CPU | Op. mode <i>Mode 191/193</i> ;<br>MTD = 0x0<br>MTD = 0x7   |                           | 110<br>800 |                         | ns<br>ns             |
| 512   | tw()hi           | Duty Cycle                                       | referenced to output period T, see Fig. 1  |                           | 50         |                         | %                    |
| 513   | t <sub>AB</sub>  | Phase Shift A vs. B                              | see Fig. 1   |                           | 25         |                         | %                    |
| 514   | t <sub>MTD</sub> | Minimum Phase Distance                           | edge to edge, see Fig. 1;<br>MTD = 0x0, IBN calibrated to 200 µA<br>MTD = 0x0, IBN calibrated to 220 µA  |                           | 220<br>200 |                         | ns<br>ns             |
| 515   | Δt()MTD          | Minimum Phase Distance Tolerance                 | nominal values in Table 54   | -18                       |            | 13.5                    | %                    |
| 516   | Δt()MTD          | Minimum Phase Distance Variation                 | variation versus VDD = 5 V, Tj = 27 °C due to VDD = 4.3...5.5 V or Tj = -40...125 °C   |                           | +/- 2      |                         | %                    |
| <b>Signal Level Controller ACO</b>                |                  |  |  |                           |            |                         |                      |
| 601   | Vs()hi           | Saturation Voltage hi                            | Vs()hi = VDD - V();<br>ADJ(8:0) = 0x11F, I(ACO) = -5 mA<br>ADJ(8:0) = 0x13F, I(ACO) = -10 mA<br>ADJ(8:0) = 0x15F, I(ACO) = -25 mA<br>ADJ(8:0) = 0x17F, I(ACO) = -50 mA |                           |            | 1<br>1<br>1<br>1.2      | V<br>V<br>V<br>V     |
| 602   | Isc()hi          | Short-Circuit Current hi                         | V() = 0 ... VDD - 1 V;<br>ADJ(8:0) = 0x11F<br>ADJ(8:0) = 0x13F<br>ADJ(8:0) = 0x15F<br>V() = 0 ... VDD - 1.2 V;<br>ADJ(8:0) = 0x17F                                     | -10<br>-20<br>-50<br>-100 |            | -5<br>-10<br>-25<br>-50 | mA<br>mA<br>mA<br>mA |
| 603   | It()min          | Control Range Monitoring 1: lower limit          | referenced to range ADJ(6:5)   |                           | 3          |                         | %Isc                 |
| 604   | It()max          | Control Range Monitoring 2: upper limit          | referenced to range ADJ(6:5)   |                           | 90         |                         | %Isc                 |
| 605   | Vt()min          | Signal Level Monitoring 1: lower limit           | referenced to Vscq()   |                           | 40         |                         | %Vpp                 |
| 606   | Vt()max          | Signal Level Monitoring 2: upper limit           | referenced to Vscq()   |                           | 130        |                         | %Vpp                 |
| 607   | Vin(ACO)         | Permissible Input Voltage for Offset-Tracking    | versus GNDS, VOS12 = 0x0   | 0                         |            | VDDS                    | V                    |
| <b>Bias Current Source and Reference Voltages</b> |                  |  |  |                           |            |                         |                      |
| 801   | IBN              | Bias Current Source                              | <i>Calibration 1</i> , I(NB) vs. VDDS;<br>CFGIBN = 0x0<br>CFGIBN = 0xF<br>IBN calibrated at Tj = 25 °C   | 110<br>180                | 200        | 370<br>220              | µA<br>µA<br>µA       |
| 802   | VBG              | Internal Bandgap Reference                       |  | 1.2                       | 1.25       | 1.3                     | V                    |
| 803   | VPAH             | Reference Voltage                                |  | 45                        | 50         | 55                      | %VDDS                |
| 804   | V05              | Reference Voltage V05                            |  | 450                       | 500        | 550                     | mV                   |
| 805   | V025             | Reference Voltage V025                           |  |                           | 50         |                         | %V05                 |
| <b>Power-Down-Reset</b>                           |                  |  |  |                           |            |                         |                      |
| 901   | VDDon            | Turn-on Threshold VDD, Power-Up-Enable           | increasing voltage at VDD  | 3.6                       | 4.0        | 4.3                     | V                    |
| 902   | VDDoff           | Turn-off Threshold VDD, Power-Down-Reset         | decreasing voltage at VDD  | 3.0                       | 3.5        | 3.8                     | V                    |
| 903   | VDDhys           | Hysteresis                                       |  | 0.4                       |            |                         | V                    |
| <b>Error Signal Input/Output, Pin ERR</b>         |                  |  |  |                           |            |                         |                      |
| B01   | Vs()lo           | Saturation Voltage lo                            | versus GND, I() = 4 mA   |                           |            | 0.4                     | V                    |
| B02   | Isc()lo          | Short-Circuit Current lo                         | versus GND, V(ERR) ≤ VDD   | 4                         | 5          | 8                       | mA                   |
| B03   | Isc()            | Low-Side Current Source For Data Output          | versus GND, V(ERR) > VTMon<br>L state<br>Z state   |                           | 2<br>0     |                         | mA<br>mA             |
| B04   | Vt()hi           | Input Threshold Voltage hi                       | versus GND   |                           |            | 2                       | V                    |
| B05   | Vt()lo           | Input Threshold Voltage lo                       | versus GND   | 0.8                       |            |                         | V                    |

## ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 4.3...5.5 V, Tj = -40 °C...125 °C, IBN calibrated to 200 µA, unless otherwise stated

| Item No.  | Symbol      | Parameter   | Conditions   | Min.              | Typ.                    | Max.                 | Unit                 |
|---|-------------|---|--|-------------------|-------------------------|----------------------|----------------------|
|   |             |   |  |                   |                         |                      |                      |
| B06   | Vt(hys)     | Input Hysteresis  | $Vt(hys) = Vt(hi) - Vt(lo)$  | 300               | 500                     |                      | mV                   |
| B07   | Ipu()       | Input-Pull-Up-Current                                     | $V() = 0...VDD - 1V$ , EPU = 1   | -400              | -300                    | -200                 | µA                   |
| B08   | Vpu()       | Pull-Up-Voltage   | $Vpu() = VDD - V()$ , I() = -5 µA, EPU = 1   |                   |                         | 0.4                  | V                    |
| B09   | VTMon       | Test Mode Turn-on Threshold                               | increasing voltage at ERR  |                   |                         | VDD + 2              | V                    |
| B10   | VTMoff      | Test Mode Turn-off Threshold                              | decreasing voltage at ERR  | VDD + 0.5         |                         |                      | V                    |
| B11   | VTMhys      | Test Mode Threshold Hysteresis                            | $VTMhys = VTMon - VTMoff$  | 0.15              | 0.3                     |                      | V                    |
| B12   | fclk()      | Data Output Signal Frequency                              | ENFAST = 0<br>ENFAST = 1   | 120<br>480        | 160<br>640              | 200<br>800           | kHz<br>kHz           |
| B13   | tp(ERR)in   | Process Delay for System Error Message at ERR             | upon power up (VDD > VDDon)  |                   | 10                      |                      | ms                   |
| <b>Reverse Polarity Protection and Supply Switches VDDS, GNDS</b> |             |   |  |                   |                         |                      |                      |
| C01   | Vs()        | Saturation Voltage vs. VDD                                | $Vs(VDDS) = VDD - V(VDDS)$ ;<br>I(VDDS) = -10...0 mA<br>I(VDDS) = -20...-10 mA                                   |                   |                         | 150<br>250           | mV<br>mV             |
| C02   | Vs()        | Saturation Voltage vs. GND                                | $Vs(GNDS) = V(GNDS) - GND$ ;<br>I(GNDS) = 0...10 mA<br>I(GNDS) = 10...20 mA                                      |                   |                         | 150<br>200           | mV<br>mV             |
| C03   | C()         | Backup Capacitor Analog Supply VDDS vs. GNDS              |  | 100               |                         |                      | nF                   |
| <b>Serial Configuration Interface SCL, SDA</b>                    |             |   |  |                   |                         |                      |                      |
| D01   | Vs(lo)      | Saturation Voltage lo                                     | I = 4 mA   |                   |                         | 400                  | mV                   |
| D02   | Isc(lo)     | Short-Circuit Current lo                                  |  | 4                 |                         | 75                   | mA                   |
| D03   | Vt(hi)      | Input Threshold Voltage hi                                |  |                   |                         | 2                    | V                    |
| D04   | Vt(lo)      | Input Threshold Voltage lo                                |  | 0.8               |                         |                      | V                    |
| D05   | Vt(hys)     | Input Hysteresis  | $Vt(hys) = Vt(hi) - Vt(lo)$  | 300               | 500                     |                      | mV                   |
| D06   | Ipu()       | Input Pull-Up Current                                     | $V() = 0...VDDS - 1V$  | -600              | -300                    | -60                  | µA                   |
| D07   | Vpu()       | Pull-Up Voltage   | $Vpu() = VDDS - V()$ , I() = -5 µA   |                   |                         | 0.4                  | V                    |
| D08   | fclk()      | Clock Frequency at SCL                                    | ENFAST = 0<br>ENFAST = 1   | 60<br>240         | 80<br>320               | 100<br>400           | kHz<br>kHz           |
| D09   | tbusy(jcfg) | Duration of Startup Configuration                         | IBN not calibrated, EEPROM access without read failure, time to outputs operational;<br>ENFAST = 0<br>ENFAST = 1 |                   | 36<br>24                | 48<br>34             | ms<br>ms             |
| D10   | tbusy(jerr) | End Of I2C Communication; Time Until I2C Slave Is Enabled | IBN not calibrated;<br>V(SDA) = 0 V<br>V(SCL) = 0 V or arbitration lost<br>no EEPROM<br>CRC ERROR                |                   | 4<br>indef.<br>45<br>95 | 12<br><br>135<br>285 | ms<br>ms<br>ms<br>ms |
| D11   | tp()        | Start Of Master Activity On I2C Protocol Error            | SCL without clock signal: V(SCL) = constant;<br>IBN not calibrated<br>IBN calibrated to 200 µA                   | 25<br>64          | 80<br>80                | 240<br>120           | µs<br>µs             |
| D12   | fclk(ext)   | Permissible External Clock Frequency at SCL               |  |                   |                         | 400                  | kHz                  |
| <b>Temperature Monitoring</b>                                     |             |   |  |                   |                         |                      |                      |
| E01   | VTs         | Temperature Sensor Voltage                                | $VTs() = VDDS - V(PA)$ ,<br>Calibration 3, without Load;<br>Tj = -40 °C<br>Tj = 27 °C<br>Tj = 100 °C             | 740<br>620<br>460 | 770<br>650<br>520       | 790<br>670<br>540    | mV<br>mV<br>mV       |
| E02   | TCs         | Temp. Co. Temperature Sensor Voltage                      |  |                   | -1.8                    |                      | mV/K                 |
| E03   | VTth        | Temperature Warning Activation Threshold                  | $VTth() = VDDS - V(NA)$ , Tj = 27 °C,<br>Calibration 3, without Load;<br>CFGTA(3:0) = 0x0<br>CFGTA(3:0) = 0xF    | 260<br>470        | 310<br>550              | 360<br>630           | mV<br>mV             |

**ELECTRICAL CHARACTERISTICS**

Operating Conditions: VDD = 4.3...5.5 V, Tj = -40 °C...125 °C, IBN calibrated to 200 μA, unless otherwise stated

| Item No. | Symbol | Parameter  | Conditions                           | Min. | Typ.      | Max. | Unit     |
|----------|--------|--|--------------------------------------|------|-----------|------|----------|
|          |        |  |                                      |      |           |      |          |
| E04      | TCth   | Temp. Co. Temperature Warning Activation Threshold |                                      |      | 0.06      |      | %/K      |
| E05      | Tw     | Warning Temperature                                | CFGTA(3:0) = 0x0<br>CFGTA(3:0) = 0xF | 125  | 140<br>65 | 80   | °C<br>°C |
| E06      | Thys   | Warning Temperature Hysteresis                     | 80 °C < Tj < 125 °C                  | 10   | 15        | 25   | °C       |
| E07      | ΔT     | Relative Shutdown Temperature                      | ΔT = Toff – Tw                       | 5    | 15        | 25   | °C       |

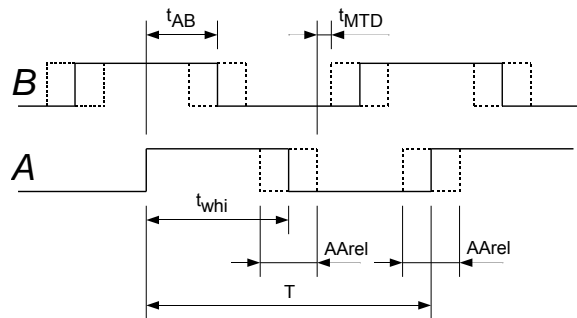


Figure 1: Definition of relative angle error and minimum phase distance

**PROGRAMMING**

|   |  |   |                                       |
|---|--|---|---------------------------------------|
| <b>Configuration Registers, Overview</b> .....                        | Page 13  | <b>Signal Conditioning CH0 (X1, X2)</b> ..... | Page 26                               |
| <b>Serial I<sup>2</sup>C Interface</b> .....                          | Page 15  | GR0:  | Gain Range CH0 (coarse)               |
| ENFAST:   | I <sup>2</sup> C Fast Mode Enable  | GF0:  | Gain Factor CH0 (fine)                |
| ENSL:   | I <sup>2</sup> C Slave Mode Enable                                       | VOS0:   | Offset Reference Source CH0           |
| DEVID:  | Device ID of EEPROM providing the<br>chip configuration data (e.g. 0x50) | OR0:  | Offset Range CH0 (coarse)             |
| CHKSUM:   | CRC of chip configuration data<br>(address range 0x00 to 0x2F)           | OF0:  | Offset Factor CH0 (fine)              |
| CHPREL:   | Chip Release   | <b>Signal Level Controller</b> .....          | Page 27                               |
| END:  | Enable Device  | ADJ:  | Setup of ACO Output Function          |
| <b>Calibration</b> .....  | Page 18  | <b>Sine-To-Digital Conversion</b> .....       | Page 28                               |
| CFGIBN:   | Bias Current   | SELRES:                                       | Resolution                            |
| CFGTA:  | Temperature Monitoring   | SELHYS:                                       | Hysteresis                            |
| <b>Operating Modes</b> .....  | Page 19  | <b>Index Gating</b> .....                     | Page 31                               |
| MODE:   | Operating Mode   | CFGABZ:                                       | Output Logic                          |
| <b>PGA Inputs Configuration<br/>and Signal Path Multiplexer</b> ..... | Page 21  | CFGZPOS:                                      | Zero Signal Positioning               |
| INMODE:   | Diff./Single-Ended Input Mode  | ENZFF:  | Zero Signal Synchronization           |
| RIN12:  | I/V Mode and Input Resistance CH1,<br>CH2                                | <b>Output Drivers</b> .....                   | Page 31                               |
| BIAS12:   | Reference Voltage CH1, CH2   | MTD:  | Minimum Phase Distance                |
| RIN0:   | I/V Mode and Input Resistance CH0  | SIK:  | Driver Short-Circuit Current          |
| BIAS0:  | Reference Voltage CH0  | SSR:  | Driver Slew Rate                      |
| BIASEX:   | Input Reference Selection  | TRIDL:  | Driver Mode                           |
| INVZ:   | Index Signal Inversion   | <b>Monitoring and Error Output</b> .....      | Page 32                               |
| MUXIN:  | Input-To-Channel Assignment:<br>X3...X6 to CH1, CH2                      | EPH:  | I/O Logic Alarm Output ERR            |
| <b>Signal Conditioning CH1, CH2 (X3...X6)</b> ...                     | Page 24  | EMTD:   | Min. Indication Time Alarm Output ERR |
| GR12:   | Gain Range CH1, CH2 (coarse)   | EPU:  | Pull-Up Enable Alarm Output ERR       |
| GF1:  | Gain Factor CH1 (fine)   | EMASKA:                                       | Error Mask Alarm Output ERR           |
| GF2:  | Gain Factor CH2 (fine)   | LINECNT:                                      | Line Count Reference                  |
| VOS12:  | Offset Reference Source CH1, CH2   | EMASKO:                                       | Error Mask Driver Shutdown            |
| VDC1:   | Intermediate Voltage CH1   | PDMODE:                                       | Driver Activation                     |
| VDC2:   | Intermediate Voltage CH2   | EMASKE:                                       | Error Mask EEPROM Savings             |
| OR1:  | Offset Range CH1 (coarse)  | ERR1:   | Error Protocol: First Error           |
| OF1:  | Offset Factor CH1 (fine)   | ERR2:   | Error Protocol: Last Error            |
| OR2:  | Offset Range CH2 (coarse)  | ERR3:   | Error Protocol: History               |
| OF2:  | Offset Factor CH2 (fine)   | <b>Test Mode</b> .....                        | Page 35                               |
| PH12:   | Phase Correction CH1 vs. CH2   | EMODE:  | Test Mode Functions                   |
|   |  | EMODE2:                                       | Test Mode Memory Selection            |

**CONFIGURATION REGISTERS**

| Overview  |               |              |               |           |             |           |             |        |  |
|---|---------------|--------------|---------------|-----------|-------------|-----------|-------------|--------|--|
| Addr  | Bit 7         | Bit 6        | Bit 5         | Bit 4     | Bit 3       | Bit 2     | Bit 1       | Bit 0  |  |
| <b>Serial Configuration Interface</b>                     |               |              |               |           |             |           |             |        |  |
| 0x00  | ENFAST        | DEVID(6:0)   |               |           |             |           |             |        |  |
| <b>Calibration</b>  |               |              |               |           |             |           |             |        |  |
| 0x01  | CFGIBN(3:0)   |              |               |           | CFGTA(3:0)  |           |             |        |  |
| <b>Operating Mode</b>                                     |               |              |               |           |             |           |             |        |  |
| 0x02  | END**         | 1            | 0             | ENZFF     | MODE(3:0)   |           |             |        |  |
| <b>Input Configuration</b>                                |               |              |               |           |             |           |             |        |  |
| 0x03  | 0             | 0            | 0             | 0         | INVZ        | INMODE    | MUXIN(1:0)  |        |  |
| <b>Signal Conditioning CH1, CH2</b>                       |               |              |               |           |             |           |             |        |  |
| 0x04  | GF2(4:0)      |              |               |           | GR12(2:0)   |           |             |        |  |
| 0x05  | GF1(3:0)      |              |               |           | 0           | 0         | 0           | 0      |  |
| 0x06  | VDC1(0)       | 0            | 0             | 0         | 0           | GF1(6:4)  |             |        |  |
| 0x07  | 0             | 0            | 0             | VDC1(5:1) |             |           |             |        |  |
| 0x08  | OR1(0)        | VDC2(5:0)    |               |           |             |           | 0           |        |  |
| 0x09  | OF1(3:0)      |              |               |           | 0           | 0         | 0           | OR1(1) |  |
| 0x0A  | 0             | 0            | OR2(1:0)      |           | OF1(7:4)    |           |             |        |  |
| 0x0B  | OF2(6:0)      |              |               |           |             |           |             | 0      |  |
| 0x0C  | PH12(2:0)     |              |               | 0         | 0           | 0         | 0           | OF2(7) |  |
| 0x0D  | BIASEX(1:0)   |              | 0             | 1         | 1           | PH12(5:3) |             |        |  |
| 0x0E  | 1             | BIAS12       | VOS12(1:0)    |           | RIN12(3:0)  |           |             |        |  |
| <b>Signal Level Controller</b>                            |               |              |               |           |             |           |             |        |  |
| 0x0F  | ADJ(0)        | —            | 0             | TOP2(4)*  | TOP2(3)*    | 0         | 0           | 0      |  |
| 0x10  | ADJ(8:1)      |              |               |           |             |           |             |        |  |
| <b>Signal Conditioning CH0</b>                            |               |              |               |           |             |           |             |        |  |
| 0x11  | GF0(4:0)      |              |               |           | GR0(2:0)    |           |             |        |  |
| 0x12  | OF0(5:0)      |              |               |           |             | OR0(1:0)  |             |        |  |
| 0x13  | 0             | BIAS0        | VOS0(1:0)     |           | RIN0(3:0)   |           |             |        |  |
| <b>Error Monitoring and Alarm Output</b>                  |               |              |               |           |             |           |             |        |  |
| 0x14  | EMASKA(7:0)   |              |               |           |             |           |             |        |  |
| 0x15  | EMODE(1:0)    |              | EMTD(2:0)     |           |             | EPH       | EMASKA(9:8) |        |  |
| 0x16  | EMASKO(7:0)** |              |               |           |             |           |             |        |  |
| 0x17  | EMASKE(3:0)   |              |               |           | ENSL        | EPU       | EMASKO(9:8) |        |  |
| 0x18  | EMODE2        | PDMODE       | EMASKE(9:4)** |           |             |           |             |        |  |
| <b>Zero Signal Output</b>                                 |               |              |               |           |             |           |             |        |  |
| 0x19  | CFGABZ(7:0)   |              |               |           |             |           |             |        |  |
| 0x1A  | CFGZPOS(7:0)  |              |               |           |             |           |             |        |  |
| <b>Sine-To-Digital Conversion, Minimum Phase Distance</b> |               |              |               |           |             |           |             |        |  |
| 0x1B  | SELRES(7:0)   |              |               |           |             |           |             |        |  |
| 0x1C  | —             | SELRES(14:8) |               |           |             |           |             |        |  |
| 0x1D  | MTD(3:0)      |              |               |           | SELHYS(3:0) |           |             |        |  |
| <b>Output Driver Settings</b>                             |               |              |               |           |             |           |             |        |  |
| 0x1E  | —             | —            | SIK(1:0)      |           | SSR(1:0)    |           | TRIHL(1:0)  |        |  |

| Overview              |   |       |               |       |           |       |           |       |
|-----------------------|---|-------|---------------|-------|-----------|-------|-----------|-------|
| Addr                  | Bit 7   | Bit 6 | Bit 5         | Bit 4 | Bit 3     | Bit 2 | Bit 1     | Bit 0 |
| <b>Line Counter</b>   |   |       |               |       |           |       |           |       |
| 0x1F                  | LINECNT(7:0)  |       |               |       |           |       |           |       |
| 0x20                  | 0   | 0     | LINECNT(13:8) |       |           |       |           |       |
| <b>Reserved</b>       |   |       |               |       |           |       |           |       |
| 0x21                  | 0   | 0     | 0             | 0     | 1         | 0     | 0         | 0     |
| 0x22                  | 0x00 (recommended programming)  |       |               |       |           |       |           |       |
| 0x23                  | 0x00 (recommended programming)  |       |               |       |           |       |           |       |
| 0x24                  | free for OEM data   |       |               |       |           |       |           |       |
| 0x25                  | free for OEM data   |       |               |       |           |       |           |       |
| 0x26                  | free for OEM data   |       |               |       |           |       |           |       |
| 0x27                  | free for OEM data   |       |               |       |           |       |           |       |
| 0x28                  | free for OEM data   |       |               |       |           |       |           |       |
| 0x29                  | free for OEM data   |       |               |       |           |       |           |       |
| 0x2A                  | free for OEM data   |       |               |       |           |       |           |       |
| 0x2B                  | free for OEM data   |       |               |       |           |       |           |       |
| 0x2C                  | free for OEM data   |       |               |       |           |       |           |       |
| 0x2D                  | free for OEM data   |       |               |       |           |       |           |       |
| 0x2E                  | free for OEM data   |       |               |       |           |       |           |       |
| <b>Check Sum</b>      |   |       |               |       |           |       |           |       |
| 0x2F                  | CHKSUM(7:0) of EEPROM data [CHPREL(7:0), refer to Table 10]   |       |               |       |           |       |           |       |
| <b>Error Register</b> |   |       |               |       |           |       |           |       |
| 0x30                  | ERR1(7:0)   |       |               |       |           |       |           |       |
| 0x31                  | ERR2(5:0)   |       |               |       |           |       | ERR1(9:8) |       |
| 0x32                  | ERR3(3:0)   |       |               |       | ERR2(9:6) |       |           |       |
| 0x33                  | —   | —     | ERR3(9:4)     |       |           |       |           |       |
| Notes                 | The device RAM initially contains random data following power-on.<br>*) Normal operation requires TOP2(4) = 1, TOP2(3) = 0.<br>**) Mandatory programming of EEPROM: END = 1, EMASKO(7, 6) = 0, EMASKE(8, 7, 6) = 0. |       |               |       |           |       |           |       |

Table 4: Register layout (EEPROM)

## SERIAL I<sup>2</sup>C INTERFACE

The multi-master capable I<sup>2</sup>C interface consists of two bidirectional pins, SCL (for clock) and SDA (for data), and enables iC-MQ to restore its configuration from the external serial EEPROM. For this function, the readout can be accelerated from ENFAST reading onwards if a higher clock frequency is selected as an option.

The I<sup>2</sup>C master of iC-MQ addresses I<sup>2</sup>C devices using an 8-bit register address plus 3 block selection bits as part of the I<sup>2</sup>C device ID.

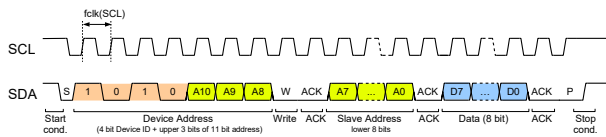


Figure 2: I<sup>2</sup>C slave addressing for writing a single byte to the EEPROM.

Furthermore, the I<sup>2</sup>C interface can be enabled to operate as an I<sup>2</sup>C slave (using ENSL), allowing an external I<sup>2</sup>C master to monitor and edit iC-MQ's configuration data.

| ENFAST |  | Addr. 0x00, bit 7 |
|--------|--|-------------------|
| Code   | Function   |                   |
| 0      | Regular clock rate, f(SCL) approx. 80 kHz  |                   |
| 1      | High clock rate, f(SCL) approx. 320 kHz  |                   |
| Notes  | For in-circuit programming bus lines SCL and SDA require pull-up resistors (e.g. 2.2 kΩ for line capacitances of up to 170 pF and clock rate 320 kHz; the permissible minimum value is 1.5 kΩ). A ground trace between SCL and SDA is recommended to avoid cross talk. |                   |

Table 5: I<sup>2</sup>C Fast Mode

| ENSL |  | Addr. 0x17, bit 3 |
|------|--|-------------------|
| Code | Function   |                   |
| 0    | I <sup>2</sup> C slave mode disabled                 |                   |
| 1    | I <sup>2</sup> C slave mode enabled (Device ID 0x55) |                   |

Table 6: I<sup>2</sup>C Slave Mode

| I <sup>2</sup> C Master Performance |  |
|-------------------------------------|--|
| Protocol                            | Standard I <sup>2</sup> C  |
| Output Clock Rate                   | 100 kHz max. (see Elec.Char. D08), 400 kHz max. using ENFAST = 1         |
| Addressing                          | 11 bit: 8 bit register address plus 3 bit block selection                |
| Access Trials                       | Read: up to 4x at power-on (I <sup>2</sup> C error: acknowledge missing) |
| Multi-Master Capability             | Yes  |
| I <sup>2</sup> C Slave Performance  |  |
| Input Clock Rate                    | 400 kHz max. (see Elec.Char. D12)  |
| Device ID                           | 0x55 ('1010 101' w/o R/W bit)  |

Table 7: I<sup>2</sup>C interface performance

**Note:** The I<sup>2</sup>C bus lines are sensitive. Keeping the traces short and shielding them with ground prevents unwanted actions.

The use of pull-up resistors (e.g. 2.2 kΩ at SCL and SDA) supports the bus signals on logic high and improves the EMI immunity.

**Note:** When programming the EEPROM in-circuit, iC-MQ must be powered up in advance. Note that power must be maintained (e.g. for 10 ms) to allow the EEPROM finishing its write operation.

**Attention:** If a power failure interrupts the EEPROM's write operation, the entire page content may be lost.

**Attention:** If error logging is enabled and periodic errors occur, the maximum permissible write cycles may be exceeded. The recommended precaution is to disable error logging (refer to EMASKE), and to lock the EEPROM by its WP pin after factory calibration.

## EEPROM Device Selection

| EEPROM Device Requirements |  |
|----------------------------|--|
| Supply Voltage             | 3.3 V to 5.5 V   |
| Power-On Threshold         | < 3.3 V (due to Elec.Char. 901)  |
| Addressing                 | 11 bit address max.  |
| Device Address             | 0x50 ('1010 000' w/o R/W bit),<br>0xA0 ('1010 0000' with R/W = 0)  |
| Page Buffer                | Support of <i>Page Write</i> with pages of at least 4 bytes.   |
| Size Minimum               | 512 bit (64x8 bit)<br>(address range used is 0x00 to 0x3F)   |
| Size Maximum               | 8 Kbit (4x 256x8 bit), type 24C08<br>If I <sup>2</sup> C Slave Mode is disabled:<br>16 Kbit (8x 256x8 bit), type 24C16 |

Table 8: EEPROM Device Requirements

If the EEPROM does not feature *Page Write*, error events can not be saved (EMASKE must be configured to 0x00).

The following EEPROMs have been recommended, but may need to be re-tested for the above conditions: Atmel AT24C01, ST M24C01, ST M24C02 (2K), ROHM BR24L01A-W, BR24L02-W.

**Attention:** EEPROMs that ignore the block select or upper address bits in the control byte (such as the Microchip 24AA0x/24LC0xB) should not be used with the iC-MQ.

EEPROMs that use the address pins as additional enable bits should be used instead.

**Attention:** When I<sup>2</sup>C Slave Mode is enabled, iC-MQ responds to device ID 0x55, limiting the maximum EEPROM size to 8 Kbit (0x50 to 0x53 addresses 4x 256 bytes).

## Device Startup

Once the supply has been switched on, i.e. after a power down reset, the iC-MQ outputs are high impedance (tristate) until a valid configuration is read from the EEPROM using device ID 0x50.

If the configuration data is not confirmed by its checksum, the readin process is repeated. If no valid configuration data is available after a fourth attempt, iC-MQ terminates communication with the EEPROM and enables I<sup>2</sup>C slave mode. For timing information, refer to the Electrical Characteristics, items D10 and D11.

For devices loading valid configuration data from the EEPROM, bit ENSL decides whether the I<sup>2</sup>C slave function is enabled or not.

## Configuration Data Checksum

The checksum at address 0x1F is used to initially confirm the configuration data read from the EEPROM.

| CHKSUM             | Addr. 0x1F, bit 7:0   |
|--------------------|---|
| Code               | Function  |
| 0x00...<br>...0xFF | Checksum for address range 0x00 to 0x1E;<br>CRC polynomial 0x11D ( $x^8 + x^4 + x^3 + x^2 + 1$ )<br>Start value: 0x01 |

Table 9: Configuration Data Checksum

## Example of CRC Calculation Routine:

```

unsigned char ucDataStream = 0;
int iCRCPoly = 0x11D;
unsigned char ucCRC=0;
int i = 0;

ucCRC = 1; // start value !!!
for (iReg = 0; iReg<47; iReg ++ )
{
    ucDataStream = ucGetValue(iReg);
    for (i=0; i<=7; i++) {
        if ((ucCRC & 0x80) != (ucDataStream & 0x80))
            ucCRC = (ucCRC << 1) ^ iCRCPoly;
        else
            ucCRC = (ucCRC << 1);
        ucDataStream = ucDataStream << 1;
    }
}
    
```



### I<sup>2</sup>C Slave Mode (ENSL = 1)

In this mode iC-MQ behaves like an I<sup>2</sup>C slave with the device ID 0x55 and the configuration interface permits write and read accesses to iC-MQ's internal registers.

For chip release verification purposes an identification value is stored under ROM address 0x2F; a write access to this address is not permitted.

| CHPREL | Addr 0x2F, bit 7:0 (ROM) |
|--------|--------------------------|
| Code   | Chip Release             |
| 0x00   | Not available            |
| 0x04   | iC-MQ 3                  |
| 0x08   | iC-MQ X                  |
| 0x09   | iC-MQ X1                 |

Table 10: Chip Release

| END   | Addr 0x02, bit 7   |
|-------|--|
| Code  | Function   |
| 0     | Standby: Sin/D converter and line driver disabled (configuration changes allowed, see Table 13)  |
| 1     | Enable Device: Restart of Sin/D conversion, line driver active (configuration data must be valid)  |
| Notes | END is evaluated only during I <sup>2</sup> C slave mode. Write access changes the function. Read access does not return the chip's state.<br><br>Program END = 1 to EEPROM. |

Table 11: Enable Device

The registers 0x0 to 0x2E must be initialized with correct values before enabling iC-MQ. This can be done through the I<sup>2</sup>C slave interface if iC-MQ is used without EEPROM or if the EEPROM content is invalid. Initially, END (bit 7 of address 0x02) must be set to zero, then all registers must be configured. Finally, set END to one without changing other bits of address 0x02 to enable the device.

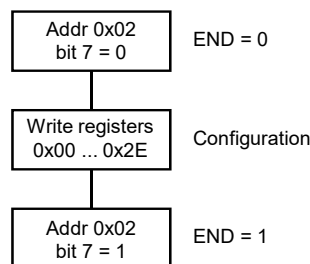


Figure 3: Programming via I<sup>2</sup>C. END is altered by changing only bit 7 of address 0x02 and leaving bits 6:0 unchanged.

### Intermediate error information buffer (Addr. 0x40-0x43)

The intermediate error information buffer is initialized whenever iC-MQ is enabled (END set to 1): ERR1 and ERR3 data is copied from RAM Addr. 0x30-0x33, and ERR2 data is initialized with 0.

The intermediate error information is modified based on EMASKE and occurring errors. (See section *Error Logging* on page 33.)

The data of the intermediate error information buffer is invalid after an EEPROM write access failed. In this case END must be toggled (set to 0, then set to 1) before accessing the intermediate error information buffer.

| Register  | Read access via I <sup>2</sup> C slave mode (ENSL = 1)                         |
|-----------|--|
| RAM Addr  | Content  |
| 0x00-0x21 | Configuration data (see EEPROM addresses 0x00-0x21)                            |
| 0x22-0x2A | Not available*   |
| 0x2B-0x2E | OEM data (4 byte) (see EEPROM addresses 0x2B-0x2E)                             |
| 0x2F      | Chip release CHPREL(7:0)   |
| 0x30-0x33 | Configuration data (see EEPROM addresses 0x30-0x33)                            |
| 0x34-0x3A | Not available  |
| 0x3B-0x3E | OEM data (4 byte) (see EEPROM addresses 0x2B-0x2E)                             |
| 0x3F      | Chip release CHPREL(7:0)   |
| 0x40-0x43 | Intermediate error information buffer  |
| 0x44-0x7F | Not available  |
| Note      | *) The EEPROM addresses 0x22-0x2A (OEM data) are not available in iC-MQ's RAM. |

Table 12: RAM Read Access

| Register  | Write access via I <sup>2</sup> C slave mode (ENSL = 1)  |
|-----------|--|
| RAM Addr  | Access and conditions  |
| 0x00      | Changes permitted during standby (END = 0)   |
| 0x01      | Changes permitted (wrong entries for CFGIBN can limit functions)   |
| 0x02      | Changes to bits 6:0 are permitted only during standby (END = 0, ie. bit 7); Restarting Sin/D conversion by changing END (bit 7) is permitted only with no changes of operating mode (bits 6:0 remain as set) |
| 0x03-0x16 | Changes permitted, no restrictions   |
| 0x17      | Changes to bits 7:4 and 2:0 are permitted during standby (END = 0) (ENSL, bit 3 must be kept 1)  |
| 0x18-0x21 | Changes permitted during standby (END = 0)   |
| 0x2B-0x2E | Changes permitted, no restrictions   |
| 0x2F      | No write access permitted  |
| 0x30-0x33 | Changes permitted during standby (END = 0)   |
| 0x34-0x43 | No write access permitted  |
| 0x44-0x7F | Not available  |

Table 13: RAM Write Access

**BIAS CURRENT SOURCE AND TEMPERATURE SENSOR CALIBRATION**

**Bias Current**

The calibration of the bias current source in operation mode *Calibration 1* (see Table 16) is prerequisite for adherence to the given electrical characteristics and also instrumental in the determination of the chip timing (e.g. clock frequency at SCL). For setup purposes the IBN bias current is measured using a 10 kΩ resistor by pin VDDS connected to pin NB. The setpoint is 200 μA which is equivalent to a voltage drop of 2 V.

**Note:** The measurement delivers a false reading when outputs are tristate (due to a configuration error after cycling power, for instance).

| CFGIBN Addr 0x01, bit 7:4 |                         |        |                         |
|---------------------------|-------------------------|--------|-------------------------|
| Code k                    | IBN ~ $\frac{31}{39-k}$ | Code k | IBN ~ $\frac{31}{39-k}$ |
| 0x0                       | 79 %                    | 0x8    | 100 %                   |
| 0x1                       | 81 %                    | 0x9    | 103 %                   |
| 0x2                       | 84 %                    | 0xA    | 107 %                   |
| 0x3                       | 86 %                    | 0xB    | 111 %                   |
| 0x4                       | 88 %                    | 0xC    | 115 %                   |
| 0x5                       | 91 %                    | 0xD    | 119 %                   |
| 0x6                       | 94 %                    | 0xE    | 124 %                   |
| 0x7                       | 97 %                    | 0xF    | 129 %                   |

Table 14: Calibration of Bias Current

**Temperature Sensor**

The temperature monitoring is calibrated in operating mode *Calibration 3*.

To set the required warning temperature T<sub>2</sub> the temperature sensor voltage VTs at which the warning message is generated is first determined. To this end a voltage ramp from VDDS towards GNDS is applied to pin PA until pin ERR displays the warning message. The following settings are required here: EMASKA = 0x20, EMTD = 0x00 and EPH = 0x00.

The signal at ERR first switches from tristate to low (on reaching the warning threshold VTs) and then from low to tristate (on overshooting the internal hysteresis which

is not relevant to calibration). To avoid confusion a clear change of state (from low to high) must be generated with the help of an external pull-up resistor at pin ERR.

*Example: VTs(T<sub>1</sub>) is ca. 650 mV, measured from VDDS versus PA, with T<sub>1</sub> = 25 °C;*

The necessary reference voltage VTth(T<sub>1</sub>) is then calculated. The required warning temperature T<sub>2</sub>, temperature coefficients TCs and TCth (see Electrical Characteristics, Section E) and measurement value VTs(T<sub>1</sub>) are entered into this calculation:

$$VTth(T_1) = \frac{VTs(T_1) + TCs \cdot (T_2 - T_1)}{1 + TCth \cdot (T_2 - T_1)}$$

*Example: For T<sub>2</sub> = T<sub>1</sub> + 100 K VTth(T<sub>1</sub>) must be programmed to 443 mV.*

Reference voltage VTth(T<sub>1</sub>) is provided for a high impedance measurement (10 MΩ) at output pin NA (measurement versus VDDS) and must be set by programming CFGTA(3:0) to the calculated value.

*Example: Altering VTth(T<sub>1</sub>) from 310 mV (measured with CFGTA(3:0)= 0x0) to 443 mV is equivalent to 143 %, the closest value for CFGTA is 0x9;*

| CFGTA Addr 0x01, bit 3:0 |   |        |                           |
|--------------------------|---|--------|---------------------------|
| Code k                   | VTth ~ $\frac{65+3k}{65}$   | Code k | VTth ~ $\frac{65+3k}{65}$ |
| 0x0                      | 100 %   | 0x8    | 140 %                     |
| 0x1                      | 105 %   | 0x9    | 145 %                     |
| 0x2                      | 110 %   | 0xA    | 150 %                     |
| 0x3                      | 115 %   | 0xB    | 155 %                     |
| 0x4                      | 120 %   | 0xC    | 160 %                     |
| 0x5                      | 125 %   | 0xD    | 165 %                     |
| 0x6                      | 130 %   | 0xE    | 170 %                     |
| 0x7                      | 135 %   | 0xF    | 175 %                     |
| Notes                    | With CFGTA = 0xF Toff is 80 °C typ., with CFGTA = 0x0 Toff is 155 °C typ. |        |                           |

Table 15: Calibration of Temperature Monitoring

**OPERATING MODES**

iC-MQ has various modes of operation, for which the functions of outputs PA, NA, PB, NB, PZ, NZ and ERR are altered.

Two operating modes can be selected for the output of the angle position in normal operation. *Mode 191/193* provides control signals for devices compatible with 74HC191 or 74HC193, whereas in *Mode ABZ* the angle position is output incrementally as an encoder quadra-

ture signal with a zero pulse. Only in these modes are the line drivers and the reverse polarity protection feature active.

In order to condition the input signals and to calibrate and test iC-MQ *Calibration* and *Test* modes are available. Digital and analog test signals are provided; the latter must always be measured at high load impedance.

| MODE(3:0) |  | Addr. 0x02; bit 3:0  |                |                |                |                 |        |             |
|-----------|--|--|----------------|----------------|----------------|-----------------|--------|-------------|
| Code      | Operating Mode   | Pin PA   | Pin NA         | Pin PB         | Pin NB         | Pin PZ          | Pin NZ | Pin ERR     |
| 0x00      | Mode ABZ   | A  | not(A)         | B              | not(B)         | Z               | not(Z) | ERR / Zin** |
| 0x0F      | Mode 191/193   | CPD  | CPU            | CP             | nU/D           | MR              | nPL    | ERR         |
| 0x01      | Calibration 1  | TANAZ(2)   | VREFIZ         | VREFISC        | IBN            | PCH0            | NCH0   | IERR        |
| 0x02      | Calibration 2  | PCH1   | NCH1           | PCH2           | NCH2           | VDC1            | VDC2   |             |
| 0x03      | Test 3*  | VPAH   | VPD            | —              | CGUCK          | IPF             | V05    | IERR        |
| 0x04      | Test 4*  | PS_out   | NS_out         | PC_out         | NC_out         | PZO             | NZO    | IERR        |
| 0x05      | Test 5*  | PSIN   | NSIN           | PCOS           | NCOS           | PZO             | NZO    | IERR        |
| 0x06      | Test 6*  | PCH1i  | NCH1i          | PCH2i          | NCH2i          | VDC1            | VDC2   | res.        |
| 0x07      | Calibration 3  | VTs  | VTth           | —              | —              | VTTFE           | VTTSE  | ERR         |
| 0x08      | Lo-Signal  | All outputs and SCL, SDA, ERR to low level                             |                |                |                |                 |        |             |
| 0x09      | Hi-Signal  | All outputs to high level  |                |                |                |                 |        |             |
| 0x0A      | Test 10*   | TP   | CLK6           | CLK1           | CLK3/8         | Z <sub>In</sub> | CLK4   |             |
| 0x0B      | System Test*   | A <sub>4</sub>   | A <sub>8</sub> | B <sub>4</sub> | B <sub>8</sub> | Z <sub>In</sub> | TP1    | ERR         |
| 0x0C      | Test 12*   | A  | not(A)         | B              | not(B)         | Z               | not(Z) | ERR         |
| 0x0D      | —  | —  | —              | —              | —              | —               | —      | —           |
| 0x0E      | IDDQ Test*   | All PU/PD resistors, oscillator and analog supply voltage deactivated. |                |                |                |                 |        |             |
| Notes     | *) Test function for iC-Haus device test only. **) EMTD = 0x00, EMASKA = 0x10<br>Analog calibration signals are output via approx. 2.5 kΩ source impedance (see Elec. Char. No. 509).<br>For accuracy of calibration the signal frequency should not exceed 4 kHz. |  |                |                |                |                 |        |             |

Table 16: Operating Modes

**Mode ABZ**

In *Mode ABZ* A/B signals are generated and output via PA, NA, PB and NB. A freely configurable zero signal is simultaneously provided at pins PZ and NZ. The differential RS422 line drivers are active; an Nx pin constantly supplies a complementary signal which is the inversion of pin Px.

**Mode 191/193**

In *Mode 191/193* the output pins provide control signals for counter devices compatible with 74HC191 or 74HC193 according to the following table. The driving capability (SIK) and the slew rate (SSR) of the output drivers must be selected so that the clock pulses can be output with a low pulse of typically 110 ns (see Electrical Characteristics 511).

| Mode 191/193 |        |   |
|--------------|--------|---|
| Pin          | Signal | Description   |
| PA           | CPD    | Clock Down Pulse  |
| NA           | CPU    | Clock Up Pulse  |
| PB           | CP     | Clock Pulse   |
| NB           | nU/D   | Count Direction (0: up, 1: down)  |
| PZ           | MR     | Asynch. Master Reset (active high)<br>Signal is '1' if index position is reached, otherwise '0'.                            |
| NZ           | nPL    | Asynch. Parallel Load Input (active low) / Reset (active low)<br>Signal is '0' if index position is reached, otherwise '1'. |

Table 17: Operating mode for counter devices compatible with 74HC191 or 74HC193.

### Calibration 1, 2, 3

These modes are used to condition the input signals and calibrate iC-MQ. In mode *Calibration 1* the user can measure the IBN bias current and the zero channel analog signals are available following signal conditioning (PCH0 and NCH0).

In mode *Calibration 2* the conditioned sine and cosine signals are output (PCH1, NCH1, PCH2 and NCH2). In addition intermediate potential VDC1 is provided for compensating circuit CH1, as is intermediate potential VDC2 for CH2 (for a description of the calibration process, see page 24).

In mode *Calibration 3* the internal temperature monitoring signals are provided. Calibration of the bias current source and temperature monitoring is described on page 18 and calibration of the zero channel on page 26.

### TEST 6

The input voltages at pins X3 to X6 can be checked in mode *Test 6*. The following settings are required here:

- GF1 = 0x0
- GF2 = 0x0
- TOP2(3) = '1'
- TOP2(4) = '0'

### System Test Mode and Digital Calibration

This mode enables the signal conditioning to be adjusted using compared sine and cosine signals. To this end at a resolution of 8 the interpolator generates a switchpoint every 45 degrees. The objective of the calibration procedure is a pulse duty cycle of exactly 50% respectively for A<sub>4</sub>, B<sub>4</sub> und A<sub>8</sub>, B<sub>8</sub>.

| System Test  |                 |  |
|--|-----------------|--|
| Pin  | Signal          | Description  |
| PA   | A <sub>4</sub>  | Offset CH1   |
| NA   | A <sub>8</sub>  | Phase deviation from 90° between CH1 and CH2   |
| PB   | B <sub>4</sub>  | Offset CH2   |
| NB   | B <sub>8</sub>  | Amplitude deviation between CH1 and CH2  |
| PZ   | Z <sub>in</sub> | Digital zero signal, unmasked  |
| NZ   | TP1             | Verification of line count (pulses) between two zero pulses<br>Low signal: verification running (state after power on reset)<br>High signal: verification finished<br>An error messaging at ERR is valid after the second zero signal (enable required). |
| ERR  | ERR             | Error signal   |
| The following settings are required for mode <i>System Test</i> :<br>MODE = 0x0B, SELRES = 0x1B0, SELHYS = 0xF, CFGABZ(7:4) = '0000' |                 |  |

Table 18: Digital Calibration Signals

**INPUT CONFIGURATION**

All input stages are configured as instrumentation amplifiers and thus directly suitable for differential input signals. Referenced input signals can be processed; input X2 can be configured as a reference input. Both current and voltage signals can be processed, selected using RIN12 and RIN0.

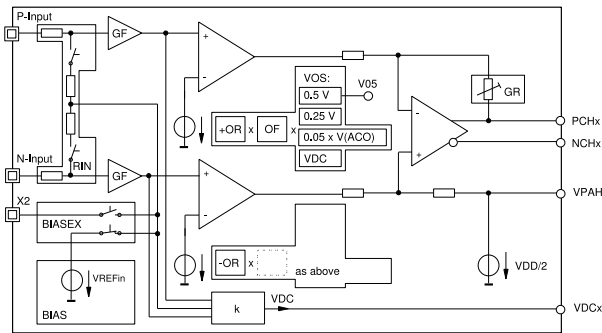


Figure 4: Signal conditioning input circuit.

**Current Signals**

In I Mode an input resistor  $R_{in}()$  becomes active at each input pin, converting the current signal into a voltage signal. Input resistance  $R_{in}()$  consists of a pad wiring resistor and resistor  $R_{ui}()$  which is linked to the adjustable bias voltage source  $V_{REFin}()$ . BIAS<sub>EX</sub> must be set to '00'.

The table besides shows the possible selections, with  $R_{in}()$  giving the typical resulting input resistance (see Electrical Characteristics for tolerances). The input resistor should be set in such a way that intermediate potentials  $V_{DC1}$  and  $V_{DC2}$  lie between 125 mV and 250 mV (verifiable in mode *Calibration 2*).

**NB.** The input circuit is not suitable for back-to-back photodiodes.

**Voltage Signals**

In V mode an optional voltage divider can be selected which reduces unacceptably large input amplitudes to ca. 25%. The circuitry is equivalent to the resistor chain in I mode; the pad wiring resistor is considerably larger here, however.

For sensors whose offset calibration is to be proportional to an external DC voltage source the reference source can be selected using BIAS<sub>EX</sub>; for all other sensors BIAS<sub>EX</sub> should be set to '00'.

| INMODE |   |
|--------|---|
| Code   | Function                                |
| 0      | Differential input signals              |
| 1      | Single-ended input signals*             |
| Note   | * Input X2 is reference for all inputs. |

Table 19: Input Signal Mode

| RIN12 |   |                     |                    |
|-------|---|---------------------|--------------------|
| RIN0  |   |                     |                    |
| Code  | Nominal $R_{in}()$  | Internal $R_{ui}()$ | I/V Mode           |
| -000  | 1.7 k $\Omega$  | 1.6 k $\Omega$      | current input      |
| -010  | 2.5 k $\Omega$  | 2.3 k $\Omega$      | current input      |
| -100  | 3.5 k $\Omega$  | 3.2 k $\Omega$      | current input      |
| -110  | 4.9 k $\Omega$  | 4.6 k $\Omega$      | current input      |
| 1-1   | 20 k $\Omega$   | 5 k $\Omega$        | voltage input 4:1* |
| 0-1   | high impedance  | 1 M $\Omega$        | voltage input 1:1  |
| Notes | For single-ended signals identical settings of RIN0 and RIN12 are required.<br>*) $V_{REFin}$ is the voltage divider's footpoint. Input currents may be positive or negative ( $V_{in} > V_{REFin}$ , or $V_{in} < V_{REFin}$ ) |                     |                    |

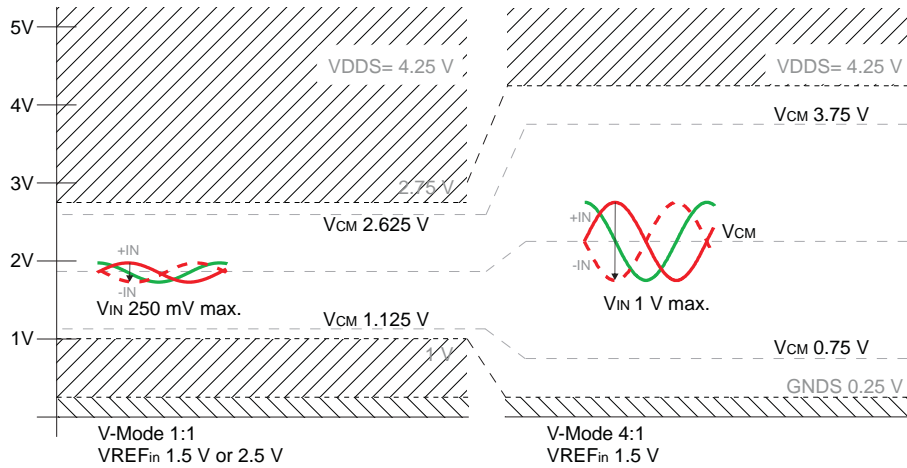
Table 20: I/V Mode and Input Resistance

| BIAS12 |  |
|--------|--|
| BIAS0  |  |
| Code   | Function   |
| 0      | $V_{REFin} = 2.5 V$<br>for low-side current sinks (e.g. photodiodes with common anode at GND <sub>S</sub> )  |
| 1      | $V_{REFin} = 1.5 V$<br>for high-side current-sources (e.g. photodiodes with common cathode at VDD <sub>S</sub> )<br>for voltage sources versus ground (e.g. iC-SM2, Wheatstone sensor bridges)<br>for voltage sources with low-side reference (e.g. iC-LSHB, when using BIAS <sub>EX</sub> = 11) |

Table 21: Reference Voltage

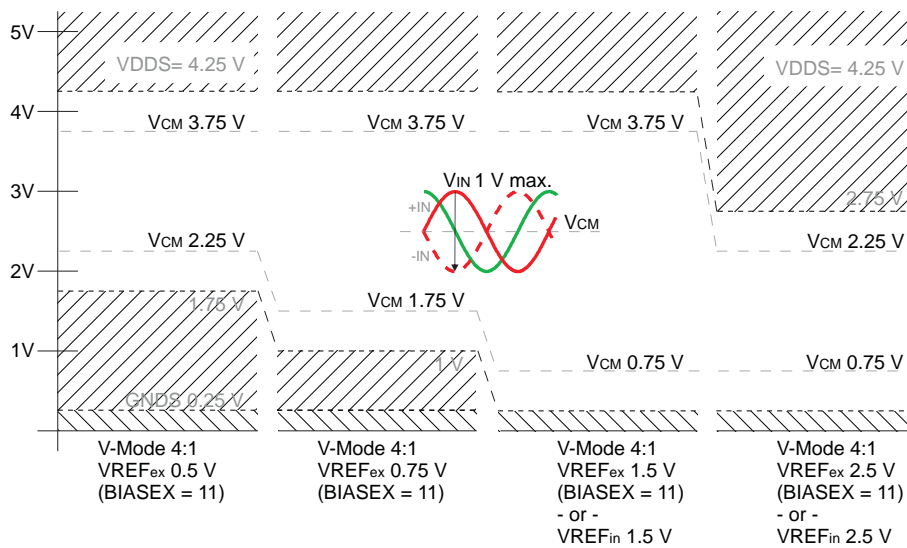
| BIASEX |   |  |
|--------|---|--|
| Code   | $V_{REFin}$   | Pin function of X2   |
| 00*    | internal  | Input Index- (negative zero signal)                          |
| 10     | internal  | Output of $V_{REFin12}$ *                                    |
| 11     | external  | Input for external reference**: $V(X2)$ replaces $V_{REFin}$ |
| Notes  | *) Do not load, buffering recommended<br>**) See Elec. Char. Nos. 122 and 123 |  |

Table 22: Input Reference Selection



NB: VREF<sub>in</sub> is referenced to GNDS.

Figure 5: Permissible common mode range and maximum input signal at lowest gain (GR12 = 0x0, GF1, GF2 = 0x00); left side: voltage input 1:1, right side: voltage input 4:1.



NB: VREF<sub>ex</sub> and VREF<sub>in</sub> are referenced to GNDS.

Figure 6: Permissible common mode range for voltage input 4:1 in dependency to the reference voltage.

**SIGNAL PATH MULTIPLEXING**

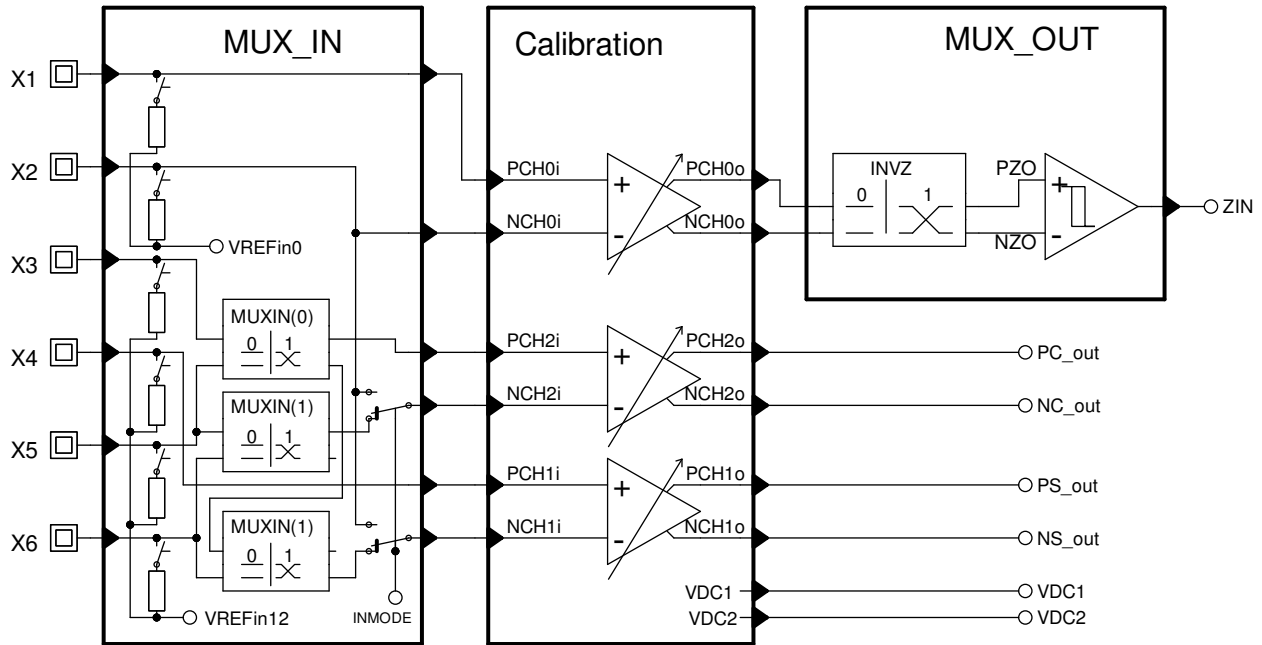


Figure 7: Principle Of Multiplexer Function

The signals for index channel CH0 are connected up to pins X1 and X2. Pins X3 to X6 are allocated to internal channels CH1 and CH2 via MUXIN. INMODE can be activated for referenced input signals; this then selects X2 as the reference signal input. For output purposes INVZ allows the index signal phase to be inverted for channel CH0.

| <b>MUXIN</b> Addr 0x03, bit 1:0 |               |       |       |       |
|---------------------------------|---------------|-------|-------|-------|
| Code                            | PCH1i         | NCH1i | PCH2i | NCH2i |
| 00                              | X4            | X6    | X3    | X5    |
| 01                              | not permitted |       |       |       |
| 10                              | X4            | X5    | X3    | X6    |
| 11                              | X4            | X3    | X5    | X6    |

Table 23: Input Multiplexer for INMODE = 0

| <b>MUXIN</b> Addr 0x03, bit 1:0 |               |       |       |       |
|---------------------------------|---------------|-------|-------|-------|
| Code                            | PCH1i         | NCH1i | PCH2i | NCH2i |
| 00                              | X4            | X2    | X3    | X2    |
| 01                              | not permitted |       |       |       |
| 10                              | not permitted |       |       |       |
| 11                              | X4            | X2    | X5    | X2    |

Table 24: Input Multiplexer for INMODE = 1

| <b>INVZ</b> Addr 0x03, bit 3 |       |       |
|------------------------------|-------|-------|
| Code                         | PZO   | NZO   |
| 0                            | PCH0o | NCH0o |
| 1                            | NCH0o | PCH0o |

Table 25: Index Signal Inversion

**SIGNAL CONDITIONING CH1, CH2**

The analog voltage signals necessary for the calibration of the sine signals can be measured in operation mode *Calibration 2*. Alternatively, characteristic digital test signals are also available for offset, amplitude and phase errors in operating mode *System Test*.

**Gain Settings**

The gain is set in four steps:

1. The sensor supply controller is shut down and the constant current source for the ACO output set to a suitable output current (register ADJ; current value close to the later operating point).
2. The coarse gain is selected so that differential signal amplitudes of ca. 1 Vpp are produced internally (signal Px versus Nx, see Figure).
3. Using fine gain factor GF2 the CH2 signal amplitude is then adjusted to 1 Vpp.
4. The CH1 signal amplitude can then be adjusted to the CH2 signal amplitude via fine gain factor GF1. This results in a total gain of GR12 \* GF1 for differential input signals.

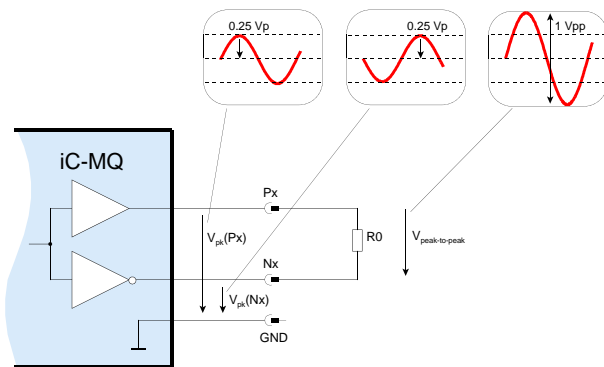


Figure 8: Definition of 1 Vpp signal. Termination R0 must be high-ohmic during all *Test* and *Calibration* modes.

| GR12 Addr 0x04, bit 2:0 |                 |                 |
|-------------------------|-----------------|-----------------|
| Code                    | Range RIN12=0x9 | Range RIN12≠0x9 |
| 0x0                     | 0.5             | 2.0             |
| 0x1                     | 1.0             | 4.1             |
| 0x2                     | 1.3             | 5.3             |
| 0x3                     | 1.7             | 6.7             |
| 0x4                     | 2.2             | 8.7             |
| 0x5                     | 2.6             | 10.5            |
| 0x6                     | 3.3             | 13.2            |
| 0x7                     | 4.0             | 16.0            |

Table 26: Gain Range CH1, CH2

| GF2 Addr 0x04, bit 7:3 |                         |
|------------------------|-------------------------|
| Code                   | Factor                  |
| 0x00                   | 1.00                    |
| 0x01                   | 1.06                    |
| ...                    | $6.25^{\frac{GF2}{31}}$ |
| 0x1F                   | 6.25                    |

Table 27: Fine Gain Factor CH2

| GF1 Addr 0x06, bit 2:0, Addr 0x05, bit 7:4 |                          |
|--|--------------------------|
| Code                                       | Factor                   |
| 0x00                                       | 1.0                      |
| 0x01                                       | 1.015                    |
| ...  | $6.25^{\frac{GF1}{124}}$ |
| 0x7F                                       | 6.53                     |

Table 28: Fine Gain Factor CH1



**Offset Calibration CH1, CH2**

In order to calibrate the offset the reference source must first be selected using VOS12. Two fixed voltages and two dependent sources are available for this purpose. The fixed voltage sources should be selected for external sensors which provide stable, self-regulating signals.

So that photosensors can be operated in optical encoders iC-MQ tracks changes in offset voltages via the signal-dependent source VDC when used in conjunction with the controlled sensor current source for LED supply (pin ACO). The VDC potential automatically tracks higher DC photocurrents. To this end intermediate potentials VDC1 and VDC2 must be adjusted to a minimal AC ripple using the selectable k factor (this calibration must be repeated when the gain setting is altered).

The feedback of pin voltage V(ACO) fulfills the same task as source VDC when MR bridge sensors are supplied by the controlled sensor current source or by supply VDDS.

| <b>VOS12</b> Addr 0x0E, bit 5:4 |   |
|---------------------------------|---|
| Code                            | Type of source  |
| 0x0                             | Feedback of ACO pin voltage: V(ACO)/20 for supply-dependent differential voltage signals for Wheatstone sensor bridges to measure VDDS  |
| 0x1, 0x2                        | Fixed reference: V05 of 500 mV, V025 of 250 mV for single-ended current or voltage signals for single-ended or differential stabilized signals (regulated sensor or waveform generator) |
| 0x3                             | Self-tracking sources VDC1, VDC2 (125...250 mV) for differential current signals for differential voltage signals*  |
| Notes                           | *) Requires BIASEX = 11 and the sensor's reference level connected to input X2 (see Elec. Char. No. 122 for acceptable input voltage).  |

Table 29: Offset Reference Source CH1, CH2

| <b>VDC1</b> Addr 0x07, bit 4:0; Addr 0x06, bit 7 |  |
|--|--|
| <b>VDC2</b> Addr 0x08, bit 6:1                   |  |
| Code   | $VDCi = (1 - k) \cdot VPi + k \cdot VNi$   |
| 0x00   | $k = 1/3$                                  |
| 0x01   | $k = 0.3386$                               |
| ...  | $k = 1/3 + 1/3 \cdot Code/63$              |
| 0x20   | $k = 0.5026$ (center setting)              |
| ...  | ...  |
| 0x3F   | $k = 2/3$                                  |
| Note   | Adjustment is required only if VOS12 = 0x3 |

Table 30: Intermediate Voltages CH1, CH2

The offset calibration range for CH1 and CH2 is dependent on the selected VOS12 source and is set using OR1 and OR2. Both sine and cosine signals are then calibrated using factors OF1 and OF2. The calibration target is reached when the DC fraction of the differential signals PCHi versus NCHi is zero.

| <b>OR1</b> Addr 0x09, bit 0; Addr 0x08, bit 7 |       |
|---|-------|
| <b>OR2</b> Addr 0x0A, bit 5:4                 |       |
| Code  | Range |
| 0x0   | x1    |
| 0x1   | x2    |
| 0x2   | x6    |
| 0x3   | x12   |

Table 31: Offset Range CH1, CH2

| <b>OF1</b> Addr 0xA, bit 3:0; Addr 0x9, bit 7:4 |            | <b>OF2</b> Addr 0xC, bit 0; Addr 0xB, bit 7:1 |                   |
|---|------------|---|-------------------|
| Code  | Factor     | Code  | Factor            |
| 0x00  | 0          | 0x80  | 0                 |
| 0x01  | + 0.0079   | 0x81  | - 0.0079          |
| ...   | + OFx /127 | ...   | - (OFx - 128)/127 |
| 0x7F  | + 1        | 0xFF  | - 1               |

Table 32: Offset Factors CH1, CH2

**Phase Correction CH1 vs. CH2**

The phase shift between CH1 and CH2 can be adjusted using parameter PH12. Following phase calibration other calibration parameters may have to be adjusted again (those as amplitude compensation, intermediate potentials and offset voltages).

| <b>PH12</b> Addr 0xD, bit 2:0; Addr 0xC, bit 7:5 |                   |      |                          |
|--|-------------------|------|--------------------------|
| Code   | Correction angle  | Code | Correction angle         |
| 0x00   | 0°                | 0x20 | 0°                       |
| 0x01   | + 0.65°           | 0x21 | - 0.65°                  |
| ...  | + 20.2° · PH12/31 | ...  | - 20.2° · (PH12 - 32)/31 |
| 0x1F   | + 20.2°           | 0x3F | - 20.2°                  |

Table 33: Phase Correction CH1 vs. CH2

**SIGNAL CONDITIONING CH0**

The voltage signals needed to calibrate the zero channel are available in mode *Calibration 1*. The relative phase position of the ungated zero signal  $Z_{in}$  compared to A and B can be determined in mode *System Test*.

**Gain Settings CH0**

Parallel to the conditioning process for the CH1 and CH2 signals the CH0 gain is also set in the following steps:

1. The sensor supply controller is shut down and the constant current source for the ACO output set to the same output current as in the calibration of CH1 and CH2 (register ADJ; current value close to the later operating point).
2. The coarse gain is selected so that a differential signal amplitude of ca. 1 Vpp is produced internally (signal PCHi versus NCHi).
3. GF0 then permits fine gain adjustment to 1 Vpp. The total gain is accrued from GR0 x GF0.

| GR0 Addr 0x11, bit 2:0 |                  |                  |
|------------------------|------------------|------------------|
| Code                   | Range RIN0 = 0x9 | Range RIN0 ≠ 0x9 |
| 0x0                    | 0.5              | 2.0              |
| 0x1                    | 1.0              | 4.1              |
| 0x2                    | 1.3              | 5.3              |
| 0x3                    | 1.7              | 6.7              |
| 0x4                    | 2.2              | 8.7              |
| 0x5                    | 2.6              | 10.5             |
| 0x6                    | 3.3              | 13.2             |
| 0x7                    | 4.0              | 16.0             |

Table 34: Gain Range CH0

| GF0 Addr 0x11, bit 7:3 |                       |
|------------------------|-----------------------|
| Code                   | Factor                |
| 0x00                   | 1.00                  |
| 0x01                   | 1.06                  |
| ...                    | $6.25 \frac{GF0}{31}$ |
| 0x1F                   | 6.25                  |

Table 35: Fine Gain Factor CH0

**Offset Calibration CH0**

To calibrate the offset the reference source must first be selected using VOS0 (see Offset Calibration CH1 and CH2 for further information). For the CH0 path the dependent source VDC is identical to source VDC1.

| VOS0 Addr 0x13, bit 5:4 |                     |
|-------------------------|---------------------|
| Code                    | Source              |
| 0x0                     | $0.05 \cdot V(ACO)$ |
| 0x1                     | 0.5 V               |
| 0x2                     | 0.25 V              |
| 0x3                     | VDC (i.e. VDC1)     |

Table 36: Offset Reference Source CH0

| OR0 Addr 0x12, bit 1:0 |       |
|------------------------|-------|
| Code                   | Range |
| 0x0                    | x1    |
| 0x1                    | x2    |
| 0x2                    | x6    |
| 0x3                    | x12   |

Table 37: Offset Range CH0

| OF0 Addr 0x12, bit 7:2 |           |      |                  |
|------------------------|-----------|------|------------------|
| Code                   | Factor    | Code | Factor           |
| 0x00                   | 0         | 0x20 | 0                |
| 0x01                   | + 0.0322  | 0x21 | - 0.0322         |
| ...                    | + OF0 /31 | ...  | - (OF0 - 32) /31 |
| 0x1F                   | + 1       | 0x3F | - 1              |

Table 38: Offset Factor CH0

**SIGNAL LEVEL CONTROL and SIGNAL MONITORING**

Via the controlled sensor current source (pin ACO) iC-MQ can keep the input signals for the internal sine-to-digital converter constant regardless of temperature and aging effects by tracking the sensor supply.

Both the controller operating range and input signal amplitude for the controller are monitored and can be enabled for error messaging. A constant current source can be selected for the ACO output when setting the signal conditioning; the current range for the highside current source is adjusted using ADJ(6:5).

| <b>ADJ (6:5)</b> Addr 0x10, bit 5:4 |               |
|-------------------------------------|---------------|
| Code                                | Function      |
| 00                                  | 5 mA - Range  |
| 01                                  | 10 mA - Range |
| 10                                  | 25 mA - Range |
| 11                                  | 50 mA - Range |

Table 39: ACO Output Current Range (applies for control modes and constant current source)

| <b>ADJ (8:7)</b> Addr 0x10, bit 7:6 |                                  |
|-------------------------------------|----------------------------------|
| Code                                | Function                         |
| 00                                  | Sine/cosine square control       |
| 01                                  | Sum control                      |
| 10                                  | Constant current source          |
| 11                                  | Not permitted (device test only) |

Table 40: ACO Output Control Mode

**Note:** Excessive input signals or internal signal clipping can interfere control operation, so that the preset operating point may not be reached (upon power up) or maintained (upon disturbances). Use Control Error 2 and Signal Error 1 for monitoring and configure EMASKA accordingly.

| <b>ADJ (4:0)</b> Addr 0x10, bit 3:0; Addr 0x0F, bit 7 |  |
|---|--|
| Code  | Square control ADJ(8:7) = 00                       |
| 0x00  | Vpp() ca. 300 mV (60 %)                            |
| 0x01  | Vpp() ca. 305 mV (61 %)                            |
| ...   | ... $\approx 300 mV \frac{77}{77 - (1.25 * Code)}$ |
| 0x19  | Vpp() ca. 500 mV (98 %)                            |
| ...   | ...  |
| 0x1F  | Vpp() ca. 600 mV (120 %)                           |

Table 41: Setpoint Square Control (internal sin/cos signal amplitude)

In operation with the active square control mode ADJ(4:0) sets the internal signal amplitudes according to the relation  $(PCH1-NCH1)^2 + (PCH2-NCH2)^2$ ; these should be set to 0.25 Vpk.

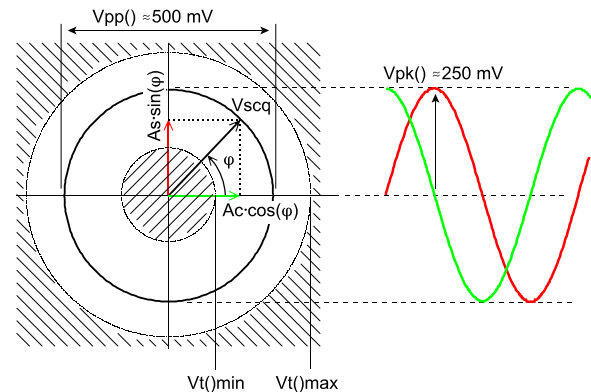


Figure 9: Internal signal monitoring and test signals in *Calibration 2* mode (example for ADJ(8:0) = 0x19).

| Signal monitoring and limits |  |           |                  |
|------------------------------|--|-----------|------------------|
| ADJ (4:0)                    | Vt()min ... max  | ADJ (4:0) | Vt()min ... max  |
| 0x00                         | 120 mV...390 mV  | 0x19      | 200 mV ...650 mV |
| 0x01                         | 122 mV...397 mV  | ...       | ...              |
| ...                          | ...  | 0x1F      | 240 mV...780 mV  |
| Note                         | All values nominal, see also Elec. Char. Nos. 605, 606 |           |                  |

Table 42: Signal Monitoring

The signal monitoring limits are tracked according to ADJ(4:0) and fit for square control mode. When using sum control mode a different operating point can be required for which the monitoring limits may not be suitable. In this case signal monitoring should be disabled via the error mask (see EMASKA etc.).

| <b>ADJ (4:0)</b> Addr 0x10, bit 3:0; Addr 0x0F, bit 7 |  |
|---|--|
| Code  | Sum control ADJ(8:7) = 01                          |
| 0x00  | VDC1 + VDC2 ca. 245 mV                             |
| 0x01  | VDC1 + VDC2 ca. 249 mV                             |
| ...   | ... $\approx 245 mV \frac{77}{77 - (1.25 * Code)}$ |
| 0x1F  | VDC1 + VDC2 ca. 490 mV                             |

Table 43: Setpoint Sum Control (DC value)

| <b>ADJ (4:0)</b> Addr 0x10, bit 3:0; Addr 0x0F, bit 7 |  |
|---|--|
| Code  | Constant current source ADJ(8:7) = 10        |
| 0x00  | I(ACO) ca. 3.125% Isc(ACO)                   |
| 0x01  | I(ACO) ca. 6.25% Isc(ACO)                    |
| ...   | ... $\approx 3.125% * (Code + 1) * Isc(ACO)$ |
| 0x1F  | I(ACO) ca. 100% Isc(ACO)                     |
| Note  | See Elec. Char. No. 602 for Isc(ACO)         |

Table 44: Setpoint Current Source (ACO output current)

**SINE-TO-DIGITAL CONVERSION**

| <b>SELRES</b> Addr 0x1C, bit 6:0; Addr 0x1B, bit 7:0 |  |                                |   |
|--|--|--------------------------------|---|
| Value  | STEP<br>Angle Steps<br>Per Period  | IPF<br>Interpolation<br>Factor | fin()max<br>Permissible Input<br>Frequency<br>(MTD=0x8) |
| 0x00E0   | 4  | 1                              | 500 kHz   |
| 0x01B0   | 8  | 2                              | 500 kHz   |
| 0x02A0   | 12   | 3                              | 200 kHz   |
| 0x0398   | 16   | 4                              | 200 kHz   |
| 0x0414   | 20   | 5                              | 200 kHz   |
| 0x0590   | 24   | 6                              | 166 kHz   |
| 0x078C   | 32   | 8                              | 125 kHz   |
| 0x090A   | 40   | 10                             | 100 kHz   |
| 0x0B88   | 48   | 12                             | 83 kHz  |
| 0x0F86   | 64   | 16                             | 62.5 kHz  |
| 0x1305   | 80   | 20                             | 50 kHz  |
| 0x1784   | 96   | 24                             | 40 kHz  |
| 0x1804   | 100  | 25                             | 40 kHz  |
| 0x1F83   | 128  | 32                             | 30 kHz  |
| 0x2F82   | 192  | 48                             | 20 kHz  |
| 0x3102   | 200  | 50                             | 20 kHz  |
| 0x5F81   | 384  | 96                             | 10 kHz  |
| 0x6301   | 400  | 100                            | 10 kHz  |
| Notes  | <p>The interpolation factor IPF is the frequency factor between input and output pins, for instance<br/> <math>IPF = f_{out}(pin\ PA) / f_{in}(pin\ X4)</math>.</p> <p>The converter's resolution in angle steps (STEP) is visible edge to edge, at output A versus output B (4-fold edge evaluation).</p> |                                |   |

Table 45: Converter Resolution

iC-MQ's converter resolution can be set using SELRES. For a resolution of 4, four angle steps per input signal period are generated so that the switching frequency at the A and B output matches the sine frequency at the input.

The programmable converter hysteresis is determined by SELHYS. It is set in multiples of 0.9° (360°/400) of the input sin/cos cycle and may have a maximum of 11.7° of the input signal period. Two additional values for SELHYS select 1/2 or 1 AB output step (edge).

| <b>SELHYS</b> Addr 0x1D, bit 3:0 |  |
|----------------------------------|--|
| Code                             | Function   |
| 0x0                              | Nearly no hysteresis   |
| 0x1                              | ≈ 0.9°   |
| 0x2                              | ≈ 1.8°   |
| 0x3-0xD                          | ≈ 2.7°-11.7°   |
| 0xE*                             | 1/2 increment of STEP  |
| 0xF**                            | 1 increment of STEP  |
| Notes                            | <p>*) permissible for STEP ≤ 200;<br/>                     **) not permissible for STEP = 4;</p> |

Table 46: Converter Hysteresis

## INDEX GATING

The set interpolation factor IPF determines the number of A/B signal cycles generated internally which are counted via register POS to enable the positioning of the zero pulse. At a sine/cosine phase angle of zero degree the A/B cycle count starts at POS = 0, and the highest cycle count is reached when  $POS_{max} = IPF - 1$ . The internal A/B signal cycle adheres to the following pattern:

|   |   |   |   |   |
|---|---|---|---|---|
| A | 1 | 1 | 0 | 0 |
| B | 1 | 0 | 0 | 1 |

Table 47: Internal A/B Signal Cycle

Inversions and reversals can be selected for the output of the A/B/Z signals and any logic combination for the output of the zero signal. The output logic pairs parameters CFGABZ in accordance with the table below:

| CFGABZ                        | Addr 0x19, bit 7:0   |
|-------------------------------|--|
| Bit                           | Function and Description   |
| 7                             | Output inversion for channel A: PA<>NA<br>PA = P1i xor CFGABZ(7)                 |
| 6                             | Output inversion for channel B: PB<>NB<br>PB = P2i xor CFGABZ(6)                 |
| 5                             | Output inversion for index channel: PZ<>NZ<br>PZ = P0i xor CFGABZ(5)             |
| 4                             | Exchange of A/B signal assignation<br>0: P1i = A, P2i = B<br>1: P1i = B, P2i = A |
| Zero Signal Logic CFGABZ(3:0) |  |
| 3                             | Enable for A = 1, B = 1  |
| 2                             | Enable for A = 1, B = 0  |
| 1                             | Enable for A = 0, B = 0  |
| 0                             | Enable for A = 0, B = 1  |

Table 48: Output Logic

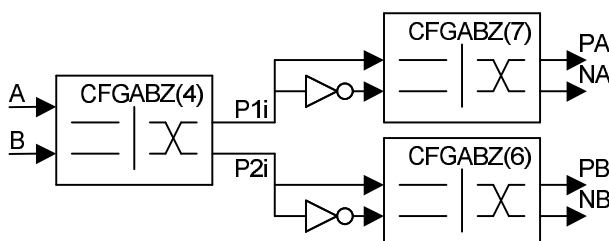


Figure 10: Signal Path from A and B to PA/NA and PB/NB

## Zero Signal Generation

The generation of the zero signal is dependant on the internal enable signal  $Z_{in}$  which is produced by comparing the processed X1 and X2 input signals. The offset calibration of CH0 influences the width of the enable signal so that the correct position of  $Z_{in}$  should be checked before the zero signal logic is configured. In *Mode ABZ* this is possible at the error signal output (pin ERR; required settings are EMASKA = 0x010 and EMTD = 0x0).

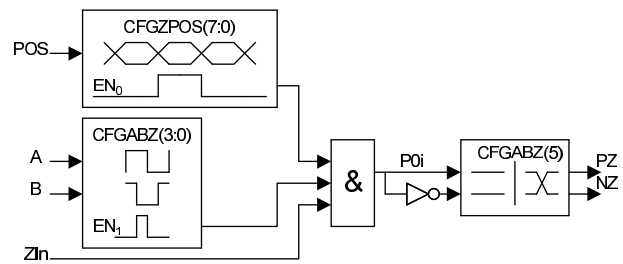


Figure 11: Signal path from  $Z_{in}$  to PZ/NZ

The positioning of the zero signal by CFGZPOS is relative to the internal A/B cycle count POS. A cycle must be selected across which enable signal  $Z_{in}$  is centered as far as is possible. For cycle counts which cannot be achieved due to a smaller interpolation factor no zero signal is generated.

| CFGZPOS | Addr 0x1A, bit 7:0   |
|---------|--|
| Bit     | Description  |
| 7       | 1: Masking active (zero signal output depending on POS)<br>0: Masking not active |
| (6:0)   | POS = A/B cycle count for zero signal output                                     |

Table 49: Zero Signal Positioning

| ENZFF | Addr 0x02, bit 4   |
|-------|--|
| Bit   | Description  |
| 0     | Zero signal output with state change of P0i  |
| 1     | Zero signal output synchronized with A/B signal  |
| Note  | This function requires an index gating window $Z_{in}$ that fully overlaps the selected AB cycle for indexing. |

Table 50: Zero Signal Synchronization

**Description Of CFGABZ Setup**

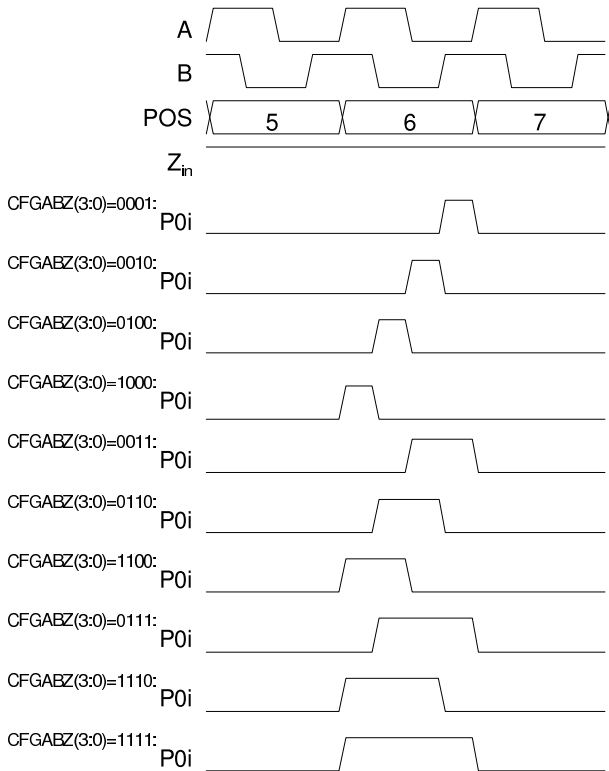


Figure 12: Function of zero signal logic CFGABZ(3:0) (Example for CFGZPOS(7)=1, CFGZPOS(6:0)=0x6)

**Setup Example 1**

Incremental ABZ output with a zero signal of 180° synchronous with the A signal at PA:  
CFGABZ = "0000 1100"

**Setup Example 2**

Incremental ABZ output with a zero signal of 270° which can be synchronized externally with a 90° zero pulse for PA = 1 und PB = 1:  
CFGABZ = "1100 0111"

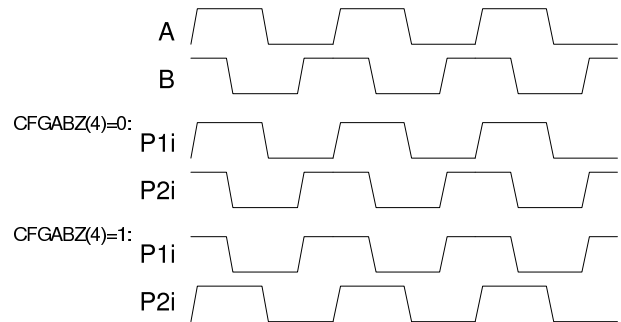


Figure 13: Function of CFGABZ(4)

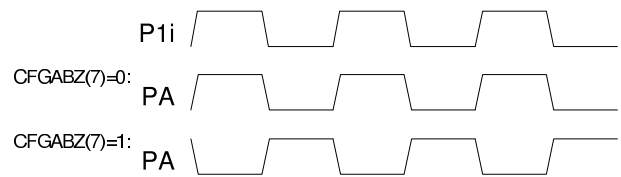


Figure 14: Function of CFGABZ(7)

**OUTPUT DRIVERS**

The output drivers can be used as push-pull, lowside or highside drivers; the mode of operation is determined by TRIHL(1:0).

In order to avoid steep edges when transmitting via short wires the slew rate can be set using SSR to suit the length of the cable. This can result in a limiting of the maximum permissible output frequency if at the same time the RS422 specification is to be adhered to (for example, to 300 kHz at a slew rate of 300 ns; the tolerances in Electrical Characteristics, numbers 506/507, must be observed).

The driver output short-circuit current can be set by SIK and can be minimized when connecting to logic or to an external 24 V line driver. If the outputs are used as RS422-compatible 5 V drivers, it is recommended that SIK = 11 to keep the power dissipation of iC-MQ low.

| <b>TRIHL</b> Addr 0x1E, bit 1:0 |   |
|---------------------------------|---|
| Code                            | Function                                    |
| 00                              | Push-pull operation                         |
| 01                              | Highside driver mode (P channel open drain) |
| 10                              | Lowside driver mode (N channel open drain)  |
| 11                              | Not permitted                               |

Table 51: Output Drive Mode

| <b>SSR</b> Addr 0x1E, bit 3:2 |                              |
|-------------------------------|------------------------------|
| Code                          | Function                     |
| 00                            | Nominal value 12 ns          |
| 01                            | Nominal value 25 ns          |
| 10                            | Nominal value 80 ns          |
| 11                            | Nominal value 220 ns         |
| Note                          | See Elec. Char. Nos. 506/507 |

Table 52: Output Slew Rate

| <b>SIK</b> Addr 0x1E, bit 5:4 |  |
|-------------------------------|--|
| Code                          | Function                               |
| 00                            | typ. 2 mA, linking logic or driver ICs |
| 01                            | typ. 8 mA                              |
| 10                            | typ. 40 mA                             |
| 11                            | typ. 100 mA, recommended for RS422     |
| Note                          | See Elec. Char. Nos. 503/504           |

Table 53: Output Short-Circuit Current

**Minimum Phase Distance**

The minimum phase distance for A/B/Z and CPD/CPU/CP output signals can be preselected using MTD(3:0). This setting limits the maximum possible output frequency for safe transmission to counters which cannot debounce spikes or only permit a low input frequency.

When preselecting the minimum edge distance the configuration of the RS422 output drivers (with regard to the driver current and slew rate) and the length of cable used must be taken into account.

| <b>MTD</b> Addr 0x1D, bit 7:4 |   |                             |
|-------------------------------|---|-----------------------------|
| Code                          | Mode ABZ: $t_{MTD}$   | Mode 191/193: $t_{clk()lo}$ |
| 0x0                           | 220 ns  | 110 ns                      |
| 0x1                           | 410 ns  | 205 ns                      |
| 0x2                           | 600 ns  | 300 ns                      |
| 0x3                           | 800 ns  | 400 ns                      |
| 0x4                           | 1.0 $\mu$ s   | 500 ns                      |
| 0x5                           | 1.2 $\mu$ s   | 600 ns                      |
| 0x6                           | 1.4 $\mu$ s   | 700 ns                      |
| 0x7                           | 1.6 $\mu$ s   | 800 ns                      |
| 0x8                           | 220 ns  | 50 ns                       |
| 0x9                           | 410 ns  | 50 ns                       |
| 0xA                           | 600 ns  | 50 ns                       |
| 0xB                           | 800 ns  | 50 ns                       |
| 0xC                           | 1.0 $\mu$ s   | 50 ns                       |
| 0xD                           | 1.2 $\mu$ s   | 50 ns                       |
| 0xE                           | 1.4 $\mu$ s   | 50 ns                       |
| 0xF                           | 1.6 $\mu$ s   | 50 ns                       |
| Note                          | All timing specifications are nominal values, see Elec. Char. No. 515 for tolerances. |                             |

Table 54: Minimum Phase Distance

**MONITORING AND ERROR OUTPUT**

iC-MQ monitors the input signals, the internal interpolator and the sensor supply controller via which the input signal levels are stabilized. If the sensor supply tracking unit reaches its control limits this can be interpreted as an end-of-life message, for example.

Three separate error masks stipulate whether error events are signaled as an alarm via I/O pin ERR (mask EMASKA), whether they cause the RS422 line drivers to shutdown or not (mask EMASKO) or whether they are stored in the EEPROM (mask EMASKE).

**Alarm Output: I/O-pin ERR**

Pin ERR is operated by a current-limited open-drain output driver and has an internal pull-up which can be disabled. The ERR pin also acts as an input for external system error messaging and for switching iC-MQ to test mode for which a voltage of larger than VTMon must be applied (see page 35). Interpretation of an external system error message and the phase of the message output is configured by EPH, the minimum indication time by EMTD.

| EPH Addr 0x15, bit 2 |  |  |
|----------------------|--|--|
| Code                 | State on error   | State w/o error  |
| 0*                   | active low   | high impedance, with input function for a low-active system error; |
| 1                    | high impedance   | active low   |
| Note                 | *) Pin ERR is disabled during driver shutdown and cannot indicate errors in this case. |  |

Table 55: I/O Logic, Alarm Output ERR

| EMTD Addr 0x15, bit 5:3 |                 |      |                 |
|-------------------------|-----------------|------|-----------------|
| Code                    | Indication Time | Code | Indication Time |
| 0x0                     | 0 ms            | 0x4  | 50 ms           |
| 0x1                     | 12.5 ms         | 0x5  | 62.5 ms         |
| 0x2                     | 25 ms           | 0x6  | 75 ms           |
| 0x3                     | 37.5 ms         | 0x7  | 87.5 ms         |

Table 56: Min. Indication Time, Alarm Output ERR

| EPU Addr 0x17, bit 2 |   |
|----------------------|---|
| Code                 | Function                                      |
| 0                    | No internal pull-up                           |
| 1                    | Internal 300 µA pull-up current source active |

Table 57: Pull-Up Enable, Alarm Output ERR

| EMASKA Addr 0x15, bit 1:0; Addr 0x14, bit 7:0 |  |
|---|--|
| Bit   | Error event  |
| 9   | Line count error (wrong count of sine periods between two zero pulses)   |
| 8   | Temporal tracking error (out-of-sync: position output differs from actual angle, e.g. after cycling power)   |
| 7   | Loss of tracking (excessive input frequency)   |
| 6*  | Configuration error (SDA or SCL pin error, no acknowledge signal from EEPROM or invalid check sum)   |
| 5   | Excessive temperature warning  |
| 4   | Ungated index enable signal $Z_{In}$ (compared X1/X2 inputs for CFGABZ and CFGZPOS adjustment, at EMTD = 0x0)  |
| 3   | Control error 2: range at max. limit   |
| 2   | Control error 1: range at min. limit   |
| 1   | Signal error 2: clipping   |
| 0   | Signal error 1: loss of signal (poor differential amplitude**, wrong s/c phase)  |
| Code  | Function   |
| 1   | Enable: event changes state of pin ERR (if EMASKO does not disable the output function).   |
| 0   | Disable: event does not affect pin ERR.  |
| Notes   | *) Pin ERR can not pull low on configuration error, use high-active error logic instead (EPH = 1);<br>**) Also due to excessive input signals or internal signal clipping. |

Table 58: Error Mask Alarm Output ERR

**Line Count Error**

Line count monitoring is particularly interesting for encoder systems. iC-MQ counts the number of sine cycles between two adjacent zero pulses and compares it to the reference value LINECNT. In case of a deviation the line count error is set. The check is paused if the direction of rotation changes, and is restarted on the next zero pulse. During mode *System Test* signal TP1 indicates when a first line count check has finished.

| LINECNT Addr 0x20, bit 5:0; Addr 0x1F, bit 7:0 |                                      |                  |
|--|--------------------------------------|------------------|
| Code   | Function Value                       | Line Count (CPR) |
| 0x0000   | 0                                    | 1                |
| ...  | ...                                  | Code + 1         |
| 0x3FFF   | 16383                                | 16384            |
| Example  | Code disc of 256 CPR → LINECNT = 255 |                  |

Table 59: Line Count Reference

**Excessive Temperature Warning**

Exceeding the temperature warning threshold  $T_w$  (corresponds to  $T_2$ , refer to Temperature Sensor, page 18) can be signaled at pin ERR or used to shut down the line drivers (via mask EMASKO). The temperature



warning is cleared if the temperature falls below  $T_w - T_{hys}$ .

**Note:** If the temperature shutdown threshold  $T_{off} = T_w + \Delta T$  is exceeded, the line drivers are shut down independently of EMASKO. For  $\Delta T$  refer to Elec. Char. E07.

### Driver Shutdown

Driver shutdown is a precaution to protect iC-MQ. Pin ACO is set to the 5mA range, the line drivers and pin ERR are tristate during driver shutdown.

Driver shutdown due to overheating or due to a configuration error is always enabled. Configuration errors are SDA or SCL pin error, no acknowledge signal from EEPROM or invalid checksum. EMASKO is used program driver shutdown due to other error events.

| PDMODE Addr 0x18, bit 6 |   |
|-------------------------|---|
| Code                    | Function  |
| 0                       | Driver shutdown terminates with the error event |
| 1                       | Permanent driver shutdown until cycling power   |

Table 60: Driver Activation

| EMASKO Addr 0x17, bit 1:0; Addr 0x16, bit 7:0 |  |
|---|--|
| Bit   | Error event  |
| 9   | Line count error (wrong count of sine periods between two zero pulses)   |
| 8   | Temporal tracking error (out-of-sync: position output differs from actual angle, e.g. after cycling power)   |
| 7*  | Loss of tracking (excessive input frequency)   |
| 6**   | —  |
| 5   | Excessive temperature warning  |
| 4   | System error: I/O pin ERR pulled to low by an external error signal (only permitted with EPH=0)  |
| 3   | Control error 2: range at max. limit   |
| 2   | Control error 1: range at min. limit   |
| 1   | Signal error 2: clipping   |
| 0   | Signal error 1: loss of signal (poor differential amplitude***, wrong s/c phase)   |
| Code  | Function   |
| 1   | Enable: event causes a driver shutdown   |
| 0   | Disable: output drivers remain active  |
| Notes   | *) Program EMASKO(7) = 0 to EEPROM.<br>**) Program EMASKO(6) = 0 to EEPROM.<br>This allows to reenble the drivers after a configuration error by toggling bit END (set zero, then one). If set 1, the driver shutdown persists and can not be resolved.<br>***) Also due to excessive input signals or internal signal clipping. |

Table 61: Error Mask Driver Shutdown

### Error Logging

Error information can be stored in the EEPROM. Only errors enabled by EMASKE are logged. The first error in the lifetime of the product is stored in ERR1. The last occurred error is stored in ERR2.

The EEPROM has an additional memory area in which all errors are accumulated (ERR3). Only errors enabled by EMASKE are logged and only the fact that this error has occurred is logged, with no information as to the time and count of appearance of that error given. Error logging can be used to statistically evaluate the causes of system failure, for example.

iC-MQ enters standby and the line drivers are shut down if an I<sup>2</sup>C communication error occurred during a write access to the EEPROM. (iC-MQ can be reenbled with bit END if EMASKO(6) is zero.)

### Clearing ERR1, ERR2 and ERR3

The error information in the EEPROM can be cleared during standby: First, set END to zero, then clear the errors in the EEPROM (Dev-ID 0x50, Addr. 0x30-0x33) *and* in the corresponding registers of iC-MQ (Dev-ID 0x55, Addr. 0x30-0x33). Finally, iC-MQ can be enabled by setting END to one.

| EMASKE Addr 0x18, bit 5:0; Addr 0x17, bit 7:4 |                                   |
|---|-----------------------------------|
| Bit   | Error event                       |
| 9   | Line count error                  |
| 8*  | —                                 |
| 7*  | —                                 |
| 6*  | —                                 |
| 5   | Excessive temperature warning     |
| 4   | System error                      |
| 3   | Control error 2                   |
| 2   | Control error 1                   |
| 1   | Signal error 2                    |
| 0   | Signal error 1                    |
| Code  | Function                          |
| 1   | Enable: event is logged           |
| 0   | Disable: event is not logged      |
| Note  | *) Mandatory programming is zero. |

Table 62: Error Mask EEPROM Savings

| ERR1 Addr 0x31, bit 1:0; Addr 0x30, bit 7:0 |                                |
|---|--------------------------------|
| ERR2 Addr 0x32, bit 3:0; Addr 0x31, bit 7:2 |                                |
| ERR3 Addr 0x33, bit 5:0; Addr 0x32, bit 7:4 |                                |
| Bit   | Error Event                    |
| 9:0   | Assignment according to EMASKE |
| Code  | Function                       |
| 0   | No event                       |
| 1   | Logged error event             |

Table 63: Error Protocol

## REVERSE POLARITY PROTECTION

iC-MQ is protected against a reversal of the supply voltage and has short-circuit-proof, error-tolerant line drivers. A defective device cable or one wrongly connected is tolerated by iC-MQ. All circuitry components which draw the monitored supply voltage from VDDS and GNDS are also protected.

The following pins are also reverse polarity protected: PA, NA, PB, NB, PZ, NZ, ERR, VDD, GND and ACO.

Conditions: This is based on the condition that GNDS only receives load currents from VDDS. The maximum voltage difference between GNDS and another pin should not exceed 6V, the exception here being pin ERR (see *Test Mode* page 35).

## TEST MODE

iC-MQ switches to test mode if a voltage larger than VTMon is applied to pin ERR (precondition: EMODE(0) = 1). In response iC-MQ transmits its configuration settings as current-modulated data using I/O pin ERR either directly from the RAM (for EMODE2 = 1) or after re-reading the EEPROM (for EMODE2 = 0). If the voltage at pin ERR falls below VTMOFF, test mode is terminated and data transmission aborted.

The clock rate for the data output is determined by ENFAST. Two clock rates can be selected: 780 ns for ENFAST = 1 or 3.125 μs for ENFAST = 0 (see Electrical Characteristics, B12, for clock frequency and tolerances).

Data is output in Manchester code via two clock pulses per bit. To this end the lowside current source switches between a Z state (OFF = 0 mA) and an L state (ON = 2 mA).

The bit information lies in the direction of the current source switch:

Zero bit: change of state Z → L (OFF to ON)

One bit: Change of state L → Z (ON to OFF)

Transmission consists of a start bit (a one bit), 8 data bits and a pause interval in Z state (the timing is identical with an EEPROM access via the I<sup>2</sup>C interface).

Example: byte value = 1000 1010

Transmission including the start bit: 1 1000 1010

In Manchester code: LZ LZLL ZLZL LZLL LZLL

Decoding of the data stream:

ZZZZZZ LZ LZ ZL ZL ZL LZ ZL LZ ZL ZZZZZZ  
Pause 1 1 0 0 0 1 0 1 0 Pause

If test mode is quit with EMODE = 0x00, iC-MQ continues operation without any interruption.

If test mode is quit with EMODE > 0x00, then iC-MQ again reads out its configuration from the EEPROM accessible at the device ID filed to DEVID(6:0) of address 0x00.

In EMODE = 0x03 the EEPROM is read completely; in all other cases only the address range 0x00 to 0x31 is read to keep the configuration time for device testing short.

| EMODE |   | Addr 0x15, bit 7:6  |
|-------|---|---|
| Code  | Function during test mode   | Function terminating test mode  |
| 00    | Normal operation  | Normal operation  |
| 01    | <b>EMODE2 = 0:</b><br>Transmission of EEPROM data<br>0x24-0x7F:<br>OEM data and registered errors<br><b>EMODE2 = 1:</b><br>Transmission of RAM data 0x3B-0x43:<br>OEM data (4 bytes) and current errors | Repeated read out of EEPROM<br>(MODE = 0: 0x00-0x7F)<br>(MODE > 0: 0x00-0x31) |
| 10    | Normal operation  | Repeated read out of EEPROM<br>(MODE = 0: 0x00-0x7F)<br>(MODE > 0: 0x00-0x31) |
| 11    | Transmission of EEPROM data (0x00-0x7F)   | Repeated read out of EEPROM (0x00-0x7F)                                       |

Table 64: Test Mode Functions

| EMODE2 |                      | Addr 0x18, bit 7 |
|--------|----------------------|------------------|
| Code   | Memory selection     |                  |
| 0      | EEPROM               |                  |
| 1      | iC-MQ RAM (ENSL = 1) |                  |

Table 65: Test Mode Memory Selection

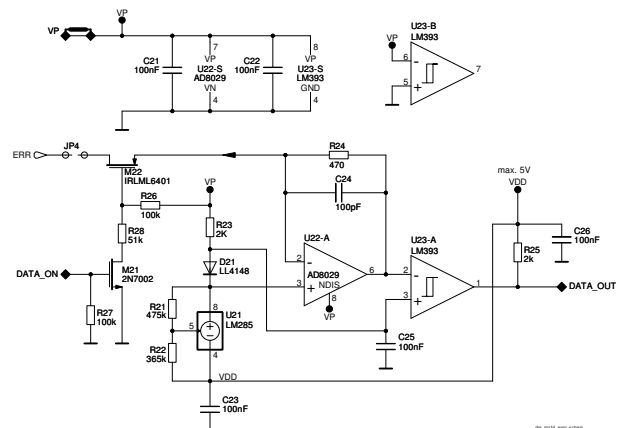


Figure 15: Example circuit for the decoding and conversion of the current-modulated signals to logic levels.

### **Quick Programming In The Single-Master System**

For the purpose of signal conditioning it is possible to reprogram iC-MQ quickly. If test mode is quit and  $EMODE \neq 00$ , iC-MQ reads the configuration data in again. In place of the standard EEPROM (DEVID 0x50) an EEPROM with a different device address can be read in which can be stored under DEVID (address 0x00, bit 6:0).

In operating modes *Mode ABZ*, *System Test* and *Mode 191/193* the content of the EEPROM is read in its entirety. For other modes the address area is limited to 0x0-0x31 so that the configuration time for either calibration or IC testing is shortened.

If the setup is switched to test mode during the readin procedure, readin is aborted and only repeated once test mode has been terminated.

### **Quick Programming In The Multimaster System**

Fast programming of iC-MQ, byte for byte, is possible with a multimaster-competent programming device. To this end the integrated I<sup>2</sup>C slave mode must be enabled by ENSL; iC-MQ then reacts to the device ID 0x55.

If no EEPROM is connected, iC-MQ automatically sets the I<sup>2</sup>C slave mode enable (after a maximum of 150 ms, see Electrical Characteristics, D11) and deactivates the digital section (ENSL = 1 and END = 0 are set). Any number of bytes can be written at any one time; the received data is accepted directly into the RAM register. The conditions given in the following table must be taken into consideration here. After programming END = 1 must be set to restart sine-to-digital conversion in the selected mode of operation.

## GENERAL APPLICATION HINTS

### In-circuit Programming Of The EEPROM

Access to the EEPROM is unhindered when the iC-MQ supply voltage is kept below power down reset threshold  $VDD_{off}$ . In this case an EEPROM which operates at a supply voltage of 2.5 V and above is required. If 3.3 V are necessary to power the EEPROM, iC-MQ's supply voltage can be raised at a maximum to power on threshold  $VDD_{on}$ ; this must occur without overshooting.

The supply voltage provided by pins  $VDDS$  and  $GNDS$  can be used to power the EEPROM; shutdown only occurs with reverse polarity. Here, the load-dependent voltage drop at both switches must be taken into account; see  $V_s(VDDS)$  and  $V_s(GNDS)$  in the Electrical Characteristics, C01 and C02.

### Absolute Angle Accuracy And Edge Jitter

The precise setting of the signal conditioning unit for correction of the analog input signals is crucial to the result of interpolation; the absolute angle error obtained determines the minimum signal jitter. Here, the effect on the transition distance of the A/B output signals is not always the same but instead dependent on the absolute phase angle of the input signals. The following gives an example for an interpolation factor of 100, i.e. 400 edges per sine period.

The offset error in the cosine signal has the strongest effect on the absolute angle error at  $90^\circ$  and  $270^\circ$ ; at  $0^\circ$  and  $180^\circ$  its influence on the transition distance is the most marked. With a range setting of  $OR1 = OR2 = 00$  and  $VOSSC = 01$  the offset error can be compensated for by an increment of 3.9 mV. If the offset has been compensated for incorrectly by one step (1 LSB), the absolute angle error would increase by ca.  $0.45^\circ$  and the transition distance vary by approximately  $\pm 0.8\%$ . Similar conditions apply to the sine signal, with the sole difference that the maxima would be shifted by  $90^\circ$ .

An error in amplitude has the strongest effect on the absolute angle error at  $45^\circ$ ,  $135^\circ$ ,  $225^\circ$  and  $315^\circ$ ; the biggest change in the transition distance can be observed at  $0^\circ$ ,  $90^\circ$ ,  $180^\circ$  and  $270^\circ$ . iC-MQ can compensate for the amplitude ratio in steps of 1.5% so that incorrect compensation by 1 LSB would increase the absolute angle error by ca.  $0.42^\circ$ . The transition distance would then vary by  $\pm 1.5\%$ .

A phase error between the sine and cosine signals (a deviation in phase shift from the ideal  $90^\circ$ ) has the most marked influence on the absolute angle error at  $0^\circ$ ,  $90^\circ$ ,  $180^\circ$  and  $270^\circ$ . The greatest effect on the transition distance is noted at  $45^\circ$ ,  $135^\circ$ ,  $225^\circ$  and  $315^\circ$ . iC-MQ's phase correction feature permits a step size of  $0.64^\circ$  so that incorrect compensation by 1 LSB would increase the absolute angle error by ca.  $0.64^\circ$ . The transition distance would then vary by  $\pm 1.1\%$ .

In a perfect signal conditioning procedure it can be assumed that the residual error constitutes half a compensation step respectively. With this, in theory iC-MQ would achieve an absolute angle accuracy of ca.  $0.5^\circ$ , with the transition distance varying by ca.  $\pm 1.5\%$ . The linearity error of the interpolator must also be taken into consideration; this increases the absolute angle error by ca.  $0.12^\circ$  and the variation in transition distance by 0.4%. With ideal, almost static input signals iC-MQ then obtains an absolute angle accuracy of  $0.62^\circ$  and a variation in transition distance of under 2%.

### Information On The Demo Board

The default delivery status of demo board EVAL MQ1D is such that it expects differential sine/cosine signals at inputs X3 to X6 with an amplitude of 125 mV, i.e.

$$V(X4) = 2.5 V + 0.125 V \sin(\varphi t)$$

$$V(X3) = 2.5 V - 0.125 V \sin(\varphi t)$$

$$V(X5) = 2.5 V + 0.125 V \sin(90^\circ + \varphi t)$$

$$V(X6) = 2.5 V - 0.125 V \sin(90^\circ + \varphi t)$$

Outputs PA, NA, PB and NB generate a differential A/B signal with an angle resolution of 4 (an interpolation factor of 1). When high sine input frequencies are applied or the resolution is increased, the minimum phase distance (MTD), short-circuit current limit (SIK) and driver slew rate (SSR) must be adjusted to meet requirements. For example, a minimum phase distance of  $MTD = 8$  should be selected with a resolution of 200 (an interpolation factor of 50) when input frequencies of up to 20 kHz are to be applied.

## APPLICATIONS NOTES: SIGNAL CONDITIONING

| MODE(3:0) |   | Addr. 0x02; bit 3:0  |                      |                      |                      |                 |             |         |
|-----------|---|----------------------|----------------------|----------------------|----------------------|-----------------|-------------|---------|
| Code      | Operating Mode  | Pin PA               | Pin NA               | Pin PB               | Pin NB               | Pin PZ          | Pin NZ      | Pin ERR |
| 0x00      | Mode ABZ  | A                    | not(A)               | B                    | not(B)               | Z               | not(Z)      | ERR     |
| 0x01      | Calibration 1   | TANAZ(2)             | VREFIZ               | VREFISC              | <b>IBN*</b>          | PCH0            | NCH0        | IERR    |
| 0x02      | Calibration 2**   | <b>PCH1</b>          | <b>NCH1</b>          | <b>PCH2</b>          | <b>NCH2</b>          | <b>VDC1</b>     | <b>VDC2</b> |         |
| 0x0B      | System Test***  | <b>A<sub>4</sub></b> | <b>A<sub>8</sub></b> | <b>B<sub>4</sub></b> | <b>B<sub>8</sub></b> | Z <sub>In</sub> | TP1         | ERR     |
| Notes     | *) Outputs must be active and not tristate; see page 18.<br>**) Analog calibration signals are output via approx. 2.5 kΩ source impedance (see Elec. Char. No. 509). For accuracy of calibration the signal frequency should not exceed 4 kHz.<br>***) Additional parameter settings are required, see page 20, Table 18. |                      |                      |                      |                      |                 |             |         |

Table 66: Used operating modes and test signals.

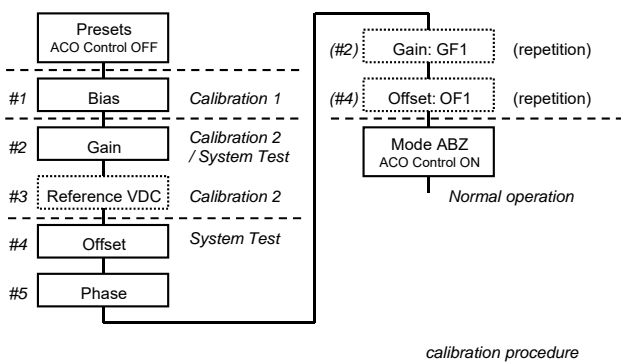


Figure 16: Principle approach (shown for channel CH1 and CH2).

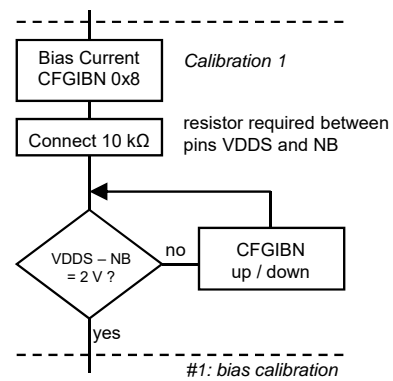


Figure 17: Verification of the bias current is recommended, and if necessary adjustment (see chapter bias current source).

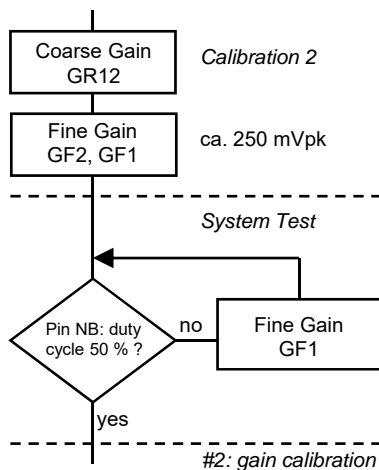


Figure 18: Adjustment of coarse gain GR12 and fine gains GF1 and GF2 to obtain the target amplitude of 250 mVpeak. Amplitude matching is adjusted by fine gain control GF1 of channel CH1.

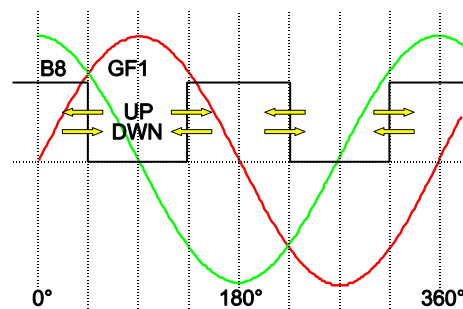


Figure 19: Test signal at pin NB for fine tuning of channel CH1 for identical amplitudes. The adjustment is ideal at a duty ratio of 50%.

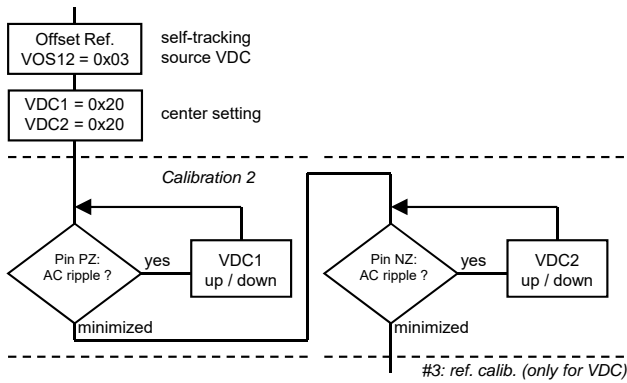


Figure 20: With self-tracking source VDC as offset reference, an adjustment of the center potentials VDC1 and VDC2 for minimal AC ripple is advisable. Other offset references do not require this adjustment.

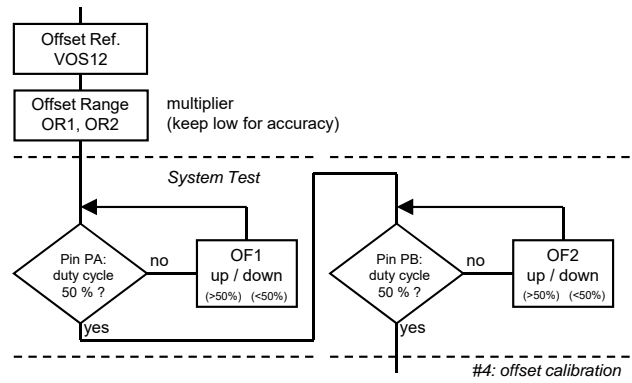


Figure 21: Selection of offset ranges OR1 and OR2 and the subsequent calibration of OF1 and OF2. Selecting OR1 resp. OR2 as small as possible permits a finer adjustment.

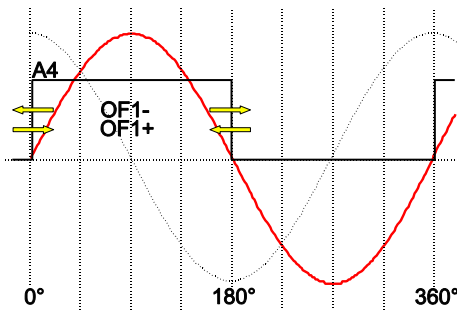


Figure 22: Test signal at pin PA for offset calibration of channel CH1. The adjustment is ideal at a duty ratio of 50%.

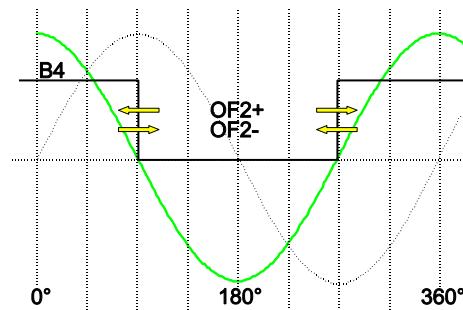


Figure 23: Test signal at pin PB for offset calibration of channel CH2. The adjustment is ideal at a duty ratio of 50%.

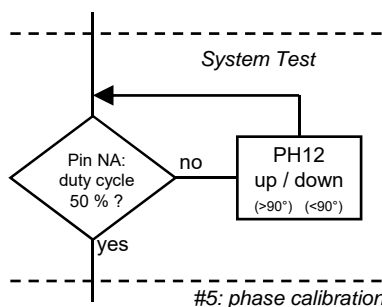


Figure 24: Correction of the sine-to-cosine phase shift by PH12. Repeating the gain and offset calibrations may be reasonable if larger phase correction values are required (refer to chapter signal conditioning for further details).

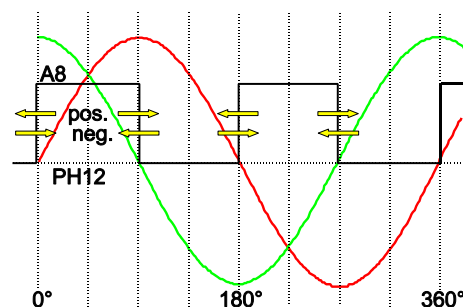


Figure 25: Test signal at pin NA for phase calibration of channel CH1 versus CH2. The adjustment is ideal at a duty ratio of 50%.

**Offset Quick Check**

During normal operation with an interpolation factor of one iC-MQ compares the sine and cosine zero crossing.

Connecting a DC voltmeter to the complementary outputs (P versus N output) indicates directly deviations of the duty cycle. Offset-free signals lead to a duty cycle of 50 % and thus to a measurement value of zero Volts ideally.

This measurement method can also be used when line drivers are connected for 24 V applications; just sensitivity is increased.

To obtain stable readings a minimal signal frequency must be selected, what may depend on the voltmeter model.

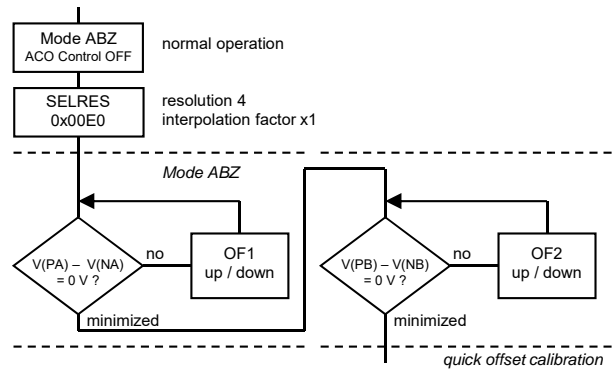


Figure 26: Offset quick check during normal operation with interpolation factor x1.

**Signal Conditioning Example 1:**

**Photodiode array connected to current inputs, LED supply with constant current source**

| Step | Operating Mode       | Calibration and Signal   |
|------|----------------------|--|
| 1.   |                      | Presets<br>VOS12= 0x3, GF1= 0x40, VDC1= 0x20, OF1= 0x0, GF2= 0x10, VDC2= 0x20, OF2= 0x0<br><br>Example: LED current approx. 6.25 mA<br>ADJ(8)= 1 (constant current source), ADJ(6:5)= 11 (range 50 mA), ADJ(4:0)= 0x04 (value 12.5)  |
| 2.   | <i>Calibration 2</i> | Calibration of Channel 1:<br>Parameter GR12: Adjust diff. signal at PA vs. NA to approx. 500 mV amplitude<br>Parameter GF1: Adjust diff. signal at PA vs. NA to exactly 500 mV amplitude<br>Parameter VDC1: Minimization of VDC1 AC fraction at output PZ (ripple < 10 mVpeak)<br>Parameter OR1, OF1: Calibration of DC fraction to zero for diff. signal PA vs. NA (< 5 mVdc) |
| 3.   | <i>Calibration 2</i> | Calibration of Channel 2:<br>Parameter GF2: Adjust diff. signal at PB vs. NB to exactly 500 mV amplitude<br>Parameter VDC2: Minimization of VDC2 AC fraction at output NZ (ripple < 10 mVpeak)<br>Parameter OR2, OF2: Calibration of DC fraction to zero for diff. signal PB vs. NB (< 5 mVdc)   |
| 4.   | <i>System Test</i>   | 1. Iteration, Calibration of Channel 1 vs. Channel 2:<br>Parameter OF1: Adjust duty ratio of A <sub>4</sub> at PA to 50 %<br>Parameter OF2: Adjust duty ratio of B <sub>4</sub> at PB to 50 %<br>Parameter PH12: Adjust duty ratio of A <sub>8</sub> at NA to 50 %<br>Parameter GF1: Adjust duty ratio of B <sub>8</sub> at NB to 50 %   |
| 5.   | <i>Calibration 2</i> | Repeated Adjustment of Intermediate Voltages, VDC1 and VDC2:<br>Parameter VDC1: Minimization of VDC1 AC fraction at output PZ<br>Parameter VDC2: Minimization of VDC2 AC fraction at output NZ   |
| 6.   | <i>System Test</i>   | 2. Iteration, Calibration of Channel 1 vs. Channel 2:<br>Parameter OF1: Adjust duty ratio of A <sub>4</sub> at PA to 50 %<br>Parameter OF2: Adjust duty ratio of B <sub>4</sub> at PB to 50 %<br>Parameter PH12: Adjust duty ratio of A <sub>8</sub> at NA to 50 %<br>Parameter GF1: Adjust duty ratio of B <sub>8</sub> at NB to 50 %   |

Table 67: Conditioning example 1



**Signal Conditioning Example 2:**

**Encoder supplying 100 mVpp to voltage inputs**

| Step | Operating Mode       | Calibration and Signal   |
|------|----------------------|--|
| 1.   |                      | Presets<br>VOS12= 0x1, GF1= 0x40, OF1= 0x0, GF2= 0x10, OF2= 0x0  |
| 2.   | <i>Calibration 2</i> | Calibration of Channel 1:<br>Parameter GR12: Adjust diff. signal at PA vs. NA to approx. 500 mV amplitude<br>Parameter GF1: Adjust diff. signal at PA vs. NA to exactly 500 mV amplitude<br>Parameter OR1, OF1: Calibration of DC fraction to zero for diff. signal PA vs. NA (< 5 mVdc)                                 |
| 3.   | <i>Calibration 2</i> | Calibration of Channel 2:<br>Parameter GF2: Adjust diff. signal at PB vs. NB to exactly 500 mV amplitude<br>Parameter OR2, OF2: Calibration of DC fraction to zero for diff. signal PB vs. NB (< 5 mVdc)   |
| 4.   | <i>System Test</i>   | Calibration of Channel 1 vs. Channel 2:<br>Parameter OF1: Adjust duty ratio of A <sub>4</sub> at PA to 50 %<br>Parameter OF2: Adjust duty ratio of B <sub>4</sub> at PB to 50 %<br>Parameter PH12: Adjust duty ratio of A <sub>8</sub> at NA to 50 %<br>Parameter GF1: Adjust duty ratio of B <sub>8</sub> at NB to 50 % |

Table 68: Conditioning example 2

## APPLICATION NOTES: CIRCUIT EXAMPLES

Figure 27 is a circuit diagram of an optical encoder with an incremental output of quadrature signals as RS422-compatible differential signals which can be terminated by 100 Ω at the controller end. By way of an

alternative the magnetic encoder in Figure 28 uses magneto-resistive sensor bridges. An external overvoltage protection circuit may be realized employing TVS diodes plus a PolyFuse in the VDD line, for instance.

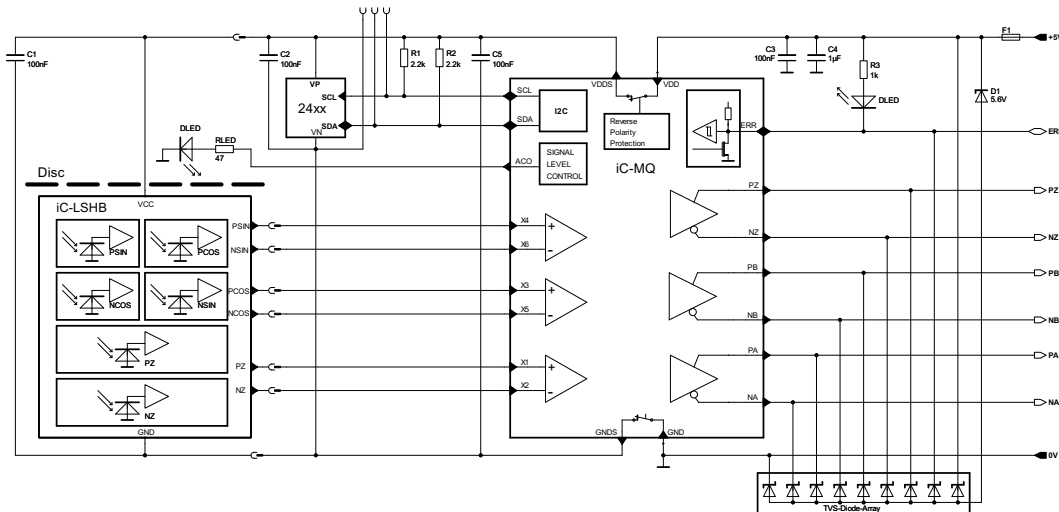


Figure 27: Optical encoder application example.

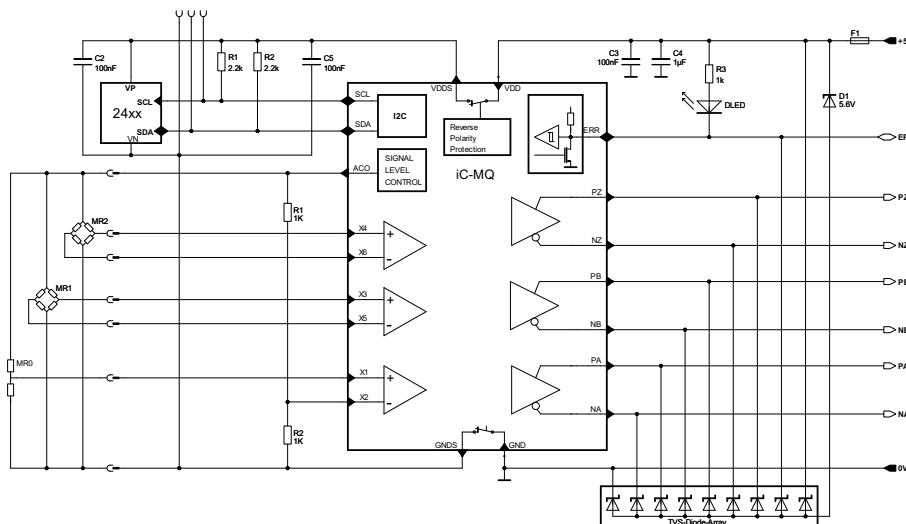


Figure 28: Magnetic encoder application example.

When iC-MQ is used in 24 V systems, with supply voltages of 5 V to 30 V for example, it can be combined with iC-DL which acts as a line driver with an integrated line adaptation feature (Figure 29).

A reduced driving capability of iC-MQ is sufficient (SIK = 00) to operate iC-DL so that the current required is reduced at the 5 V end. If an LDO voltage regulator

is selected, the circuit is suitable for a supply range of 4.5 V to 30 V without any changes having to be made.

The wiring of the iC-DL error message output (pin NER) to the PLC is not necessary if the iC-MQ error mask is set for output shutdown (EMASKO). In the event of error the pull-down current sources ensure that a low signal is produced at the iC-DL inputs on all lines which

the controller recognizes as an error. If there is an overload at the outputs, via its temperature protection unit iC-DL itself makes sure that the driver outputs are shutdown (tristate) - which the controller also classes

as an error. In addition iC-MQ can transmit the overload to the error memory as a system error when information is returned to the bidirectional I/O pin ERR (as shown).

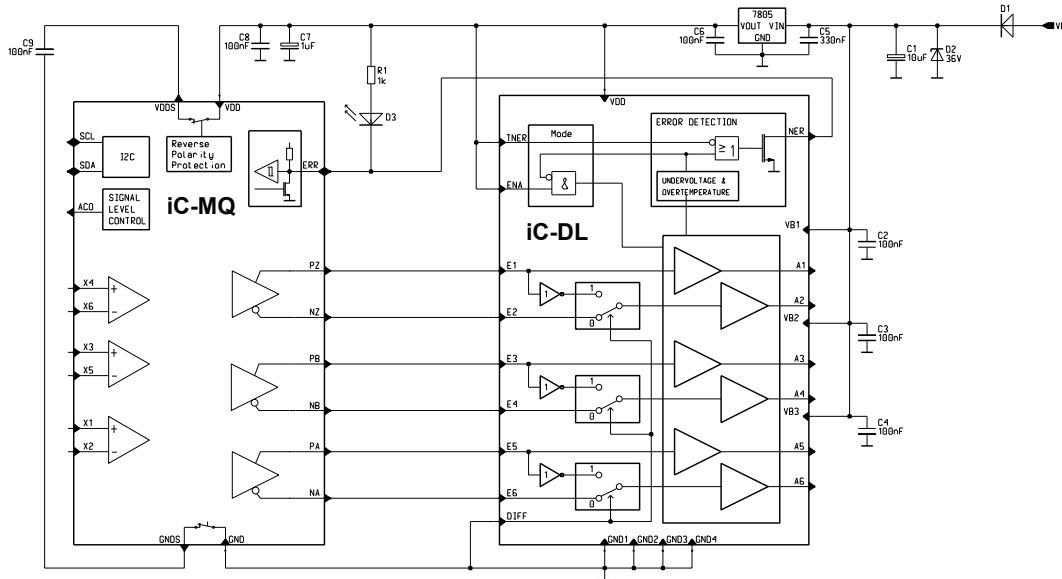


Figure 29: Application example with 24 V line driver.

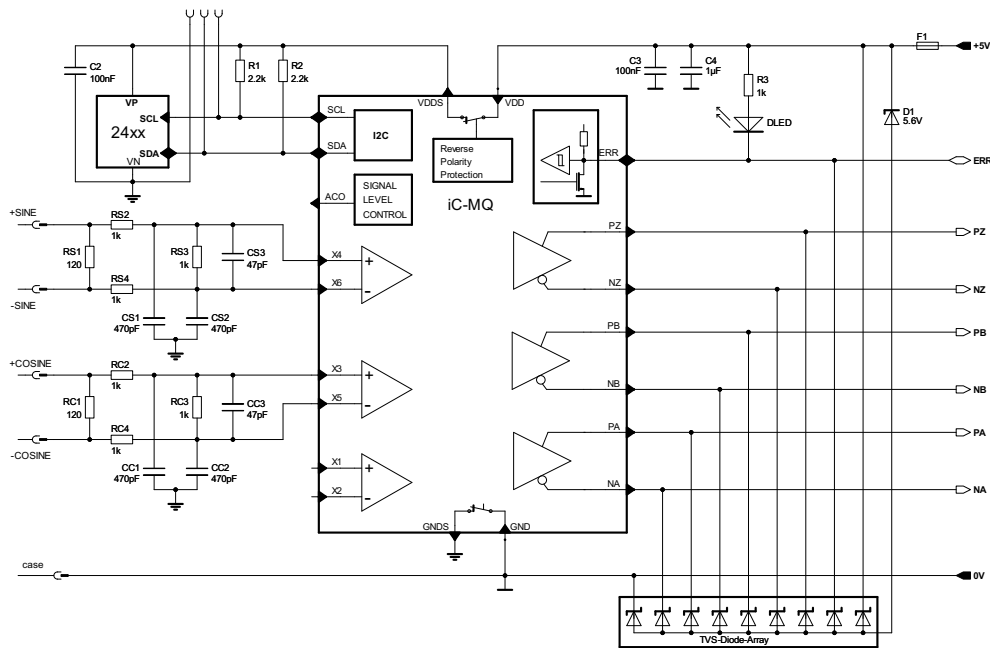


Figure 30: Input circuit for sine encoders (0.8 Vpp to 1.2 Vpp) with 120 Ω termination and low-pass filtering. RS2/RS4, respectively RC2/RC4, serve as protection against ESD and transients, RS3/RC3 reduce the input signal to suit an input gain of 3.

## DESIGN REVIEW: Notes On Chip Functions

| iC-MQ_X1 |                          |   |
|----------|--------------------------|---|
| No.      | Function, Parameter/Code | Description and Application Hints   |
| 1        | END                      | Recommended default programming of EEPROM: END = 1  |
| 2        | ENZFF                    | Recommended default programming of EEPROM: ENZFF = 0.<br>NB: ENZFF = 1 can blank index output if the external gating window is smaller than the selected AB cycle for indexing (adjusted by CFGZPOS). |
| 3        | EMASKO                   | Mandatory programming:<br>EMASKO(6) = 0. Allow driver reactivation by toggling bit END.<br>EMASKO(7) = 0. Do not use driver shutdown for loss of tracking.  |
| 4        | EMASKE                   | Mandatory programming:<br>EMASKE(6) = 0. Do not use error logging for configuration error.<br>EMASKE(7) = 0, EMASKE(8) = 0. Do not use error logging for loss of tracking.                            |

Table 69: Chip release iC-MQ\_X1

## REVISION HISTORY

| Rel. | Rel. Date* | Chapter | Modification | Page |
|------|------------|---------|--------------|------|
| F1   | 2013-08-02 | ...     |              |      |

| Rel. | Rel. Date* | Chapter                           | Modification  | Page   |
|------|------------|-----------------------------------|---|--------|
| F2   | 2014-06-02 | SERIAL CONFIGURATION INTERFACE    | I <sup>2</sup> C Slave Mode: text corrected, new subtitle: Intermediate error information buffer;<br>Table 8, END: description corrected, parameter END represents Enable Device;<br>Table 9 and 10, RAM Read/Write Access: correction of contents;   | 15     |
|      |            | SINE-TO-DIGITAL CONVERSION        | Table 43, SELHYS: description improved  | 26     |
|      |            | ERROR MONITORING AND ALARM OUTPUT | Table 52, EPH: note supplemented<br>Section Driver Shutdown: description supplemented;<br>Table 58, EMASKO: correction of code description and notes;<br>Section Error Protocol replaced by new section: Error Logging and Clearing ERR;<br>Table 59, EMASKE, and Table 60 ERR: correction of contents; | 30, 31 |

| Rel. | Rel. Date* | Chapter                                | Modification   | Page |
|------|------------|--|--|------|
| F3   | 2015-04-17 | ELECTRICAL CHAR.                       | Item 120: allowing 500 kHz at x1 and x2                      | 7    |
|      |            | REGISTER MAP                           | Footnote edited for mandatory programming                    | 12   |
|      |            | SERIAL CONFIG. INTERFACE               | Tab. 8, END: Note edited                                     | 15   |
|      |            | SINE-TO-DIGITAL CONVERSION             | Description of hysteresis updated                            | 26   |
|      |            | OUTPUT SETTINGS AND ZERO SIGNAL        | Tab. 47, ENZFF: Note edited                                  | 27   |
|      |            | ERROR MONITORING AND ALARM OUTPUT      | Tab. 58, EMASKO: Note edited<br>Tab. 59, EMASKE: Note edited | 31   |
|      |            | DESIGN REVIEW: Notes On Chip Functions | Chapter supplemented   | 42   |

| Rel. | Rel. Date* | Chapter                                      | Modification   | Page   |
|------|------------|--|--|--------|
| F4   | 2020-09-16 | BLOCK DIAGRAM                                | Update of block diagram, adaption of section titles  | 1      |
|      |            | DESCRIPTION                                  | Note box added   | 2      |
|      |            | PACKAGING INFORMATION                        | Pin configuration figure and footnote updated (value of bypass cap)<br>Package TSSOP20: dimensions added   | 4      |
|      |            | ELECTRICAL CHARACT.                          | Item D12 added   | 10     |
|      |            | SERIAL CONFIGURATION INTERFACE               | Update of description, Figure 2 added, Table 5: note updated, Table 7 added, note and attention boxes added;<br>Section EEPROM Device Selection: Table 8 max. size corrected, update of description, note boxes added; | 15ff   |
|      |            | OPERATING MODES, APPL. NOTES: SIGNAL CONDIT. | Table 16, 66: Notes added.   | 19, 38 |
|      |            | SINE-TO-DIGITAL CONVERSION                   | Table 45: Note added on IPF and STEP   | 28     |
|      |            | INDEX GATING, OUTP. DRIVERS                  | Former description of Output Settings and Zero Signal separated into 2 sections  | 29, 31 |

\* Release Date format: YYYY-MM-DD

# iC-MQ PROGRAMMABLE 9-BIT Sin/Cos INTERPOLATION IC WITH RS422 DRIVER



Rev F4, Page 45/46

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| Type             | Package                        | Options                               | Order Designation        |
|------------------|--------------------------------|---------------------------------------|--------------------------|
| iC-MQ            | 20-pin TSSOP<br>RoHS compliant |                                       | iC-MQ TSSOP20            |
|                  |                                | Temperature range<br>-40 °C to 100 °C | iC-MQ TSSOP20 ET -40/100 |
| Evaluation Board |                                |                                       | iC-MQ EVAL MQ1D          |

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