iC-MB4
BiSS INTERFACE MASTER

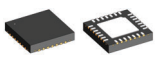
FEATURES

- Bidirectional BiSS communication with up to 8 slaves
- Supports SSI protocol for unidirectional data transmission
- Synchronous sensor data acquisition with cyclic transfer at data rates of up to 10 Mbit/s
- Configurable BiSS/SSI interface:
  two single-ended channels with TTL/CMOS transceivers or one differential channel with RS422/LVDS transceivers
- Slave register operations during cyclic data transfers
- Automatic line delay compensation
- Configurable data lengths of up to 64 bit for each sensor
- CRC verification with up to 16 bits per slave
- Separate memory banks for free controller access during BiSS sensor data transfers
- 64 bytes memory for bidirectional register access
- Parallel or serial (SPI) interface to host e.g. MCU
- Single 3 V to 5 V supply

APPLICATIONS

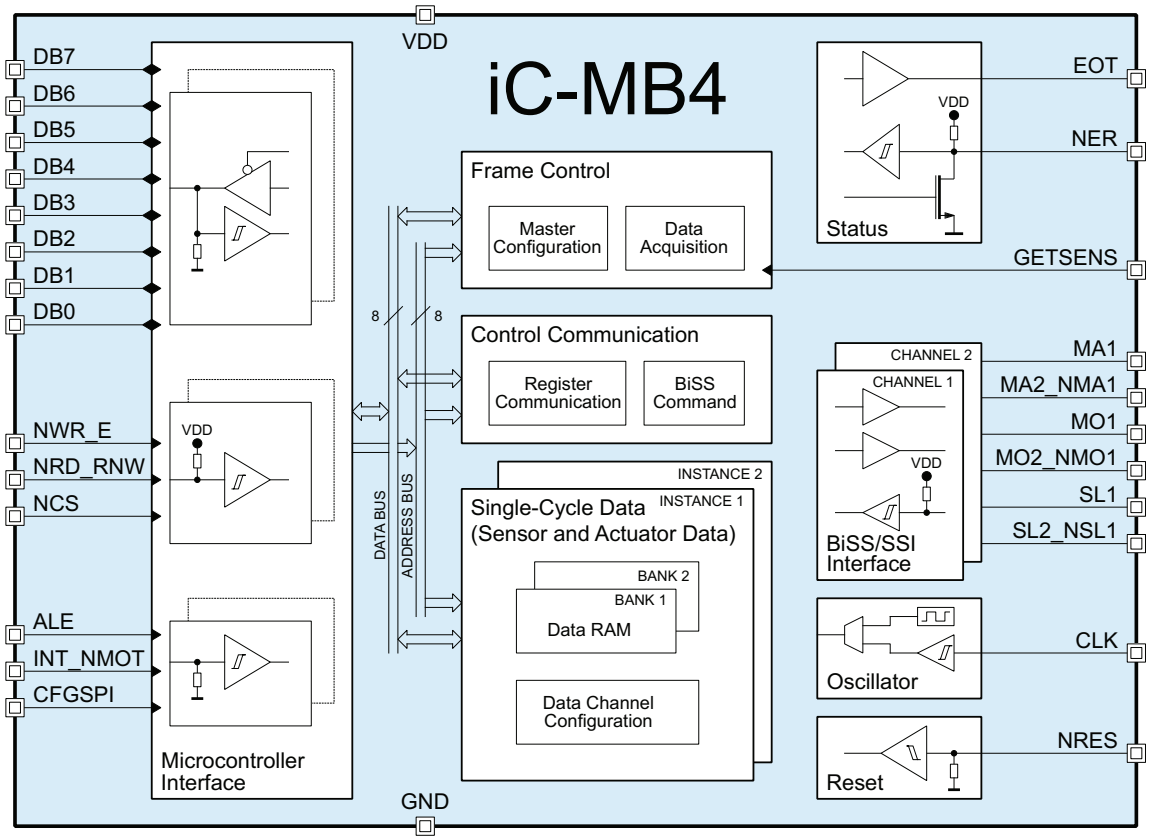
- Bidirectional communication in multi sensor systems
- Linear and rotary encoders
- Motor feedback systems
- PLCs
- Drives
- Robotics

PACKAGES



QFN28
5 mm x 5 mm
RoHS compliant

BLOCK DIAGRAM



DESCRIPTION

iC-MB4 is a single-chip BiSS/SSI interface master controller featuring an 8-bit bus interface to industrial standard microcontroller. Alternatively an SPI interface enables serial communication between iC-MB4 and the connected microcontroller. In point-to-point configuration BiSS devices including one or several sensors are connected to the clock line MA and the data return line SL (Figure 1). In bus configuration BiSS devices including actuators and sensors are additionally connected to the data line MO. It is possible to connect multiple devices (maximum eight slaves) daisy-chained (Figure 2). RS422 transceivers are available on-chip for robust differential communication in industrial environments. Two types of BiSS communication are supported:

1. **Single-Cycle Data (SCD)**:
   Sensor or actuator data with up to 64 bits for each slave (e.g. measurement data, error and warning flag, Sign-of-Life counter, . . .).
2. **Control Communication:**
   E.g. register communication for reading/writing the sensor's/actuators registers (e.g. for reading an Electronic Datasheet or calibrating sensors).

iC-MB4 provides two RAM memory banks for each slave enabling simultaneous access by the microcontroller while new sensor data is being transmitted via BiSS Interface. A 64-byte memory supports register transfers. Sensor data acquisition is started by a microcontroller instruction, via pin GETSENS or automatically by iC-MB4 at a configurable frame repetition rate. The end of the sensor data transmission is indicated at pin EOT. An error during transmission is flagged by pin NER. Error details can be accessed in the status registers even if pin NER is kept low by an external error signal. iC-MB4 generates a clock signal for sensor communication using an internal 20 MHz oscillator. For high-performance applications a precise external oscillator can be applied.

The BiSS C Protocol Description is available at www.biss-interface.com.

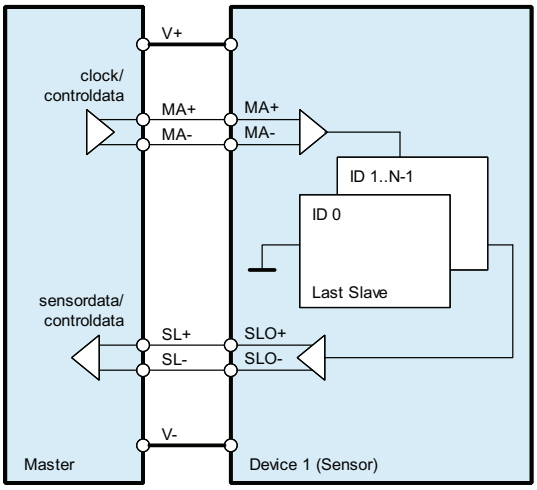


Figure 1: Point-to-point configuration of iC-MB4 to one device with several slaves

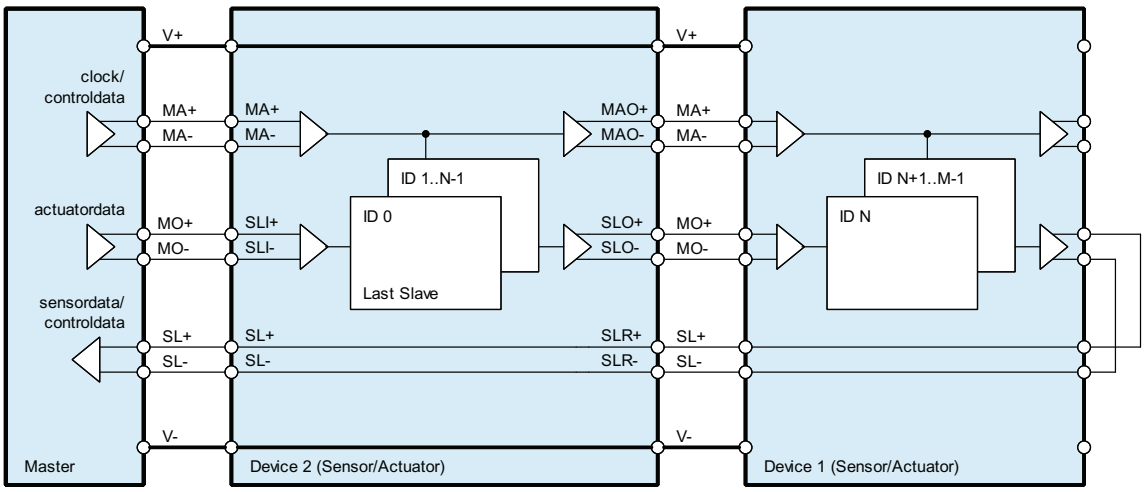
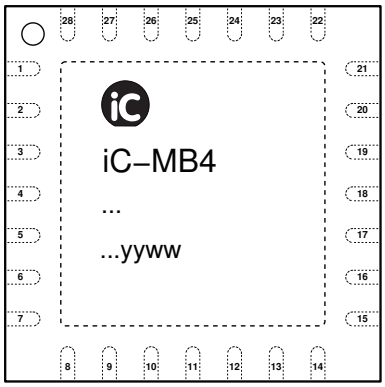


Figure 2: Bus configuration of iC-MB4 and two devices

PACKAGING INFORMATION TO JEDEC

PIN CONFIGURATION QFN28 5 mm x 5 mm
(topview)



PIN FUNCTIONS

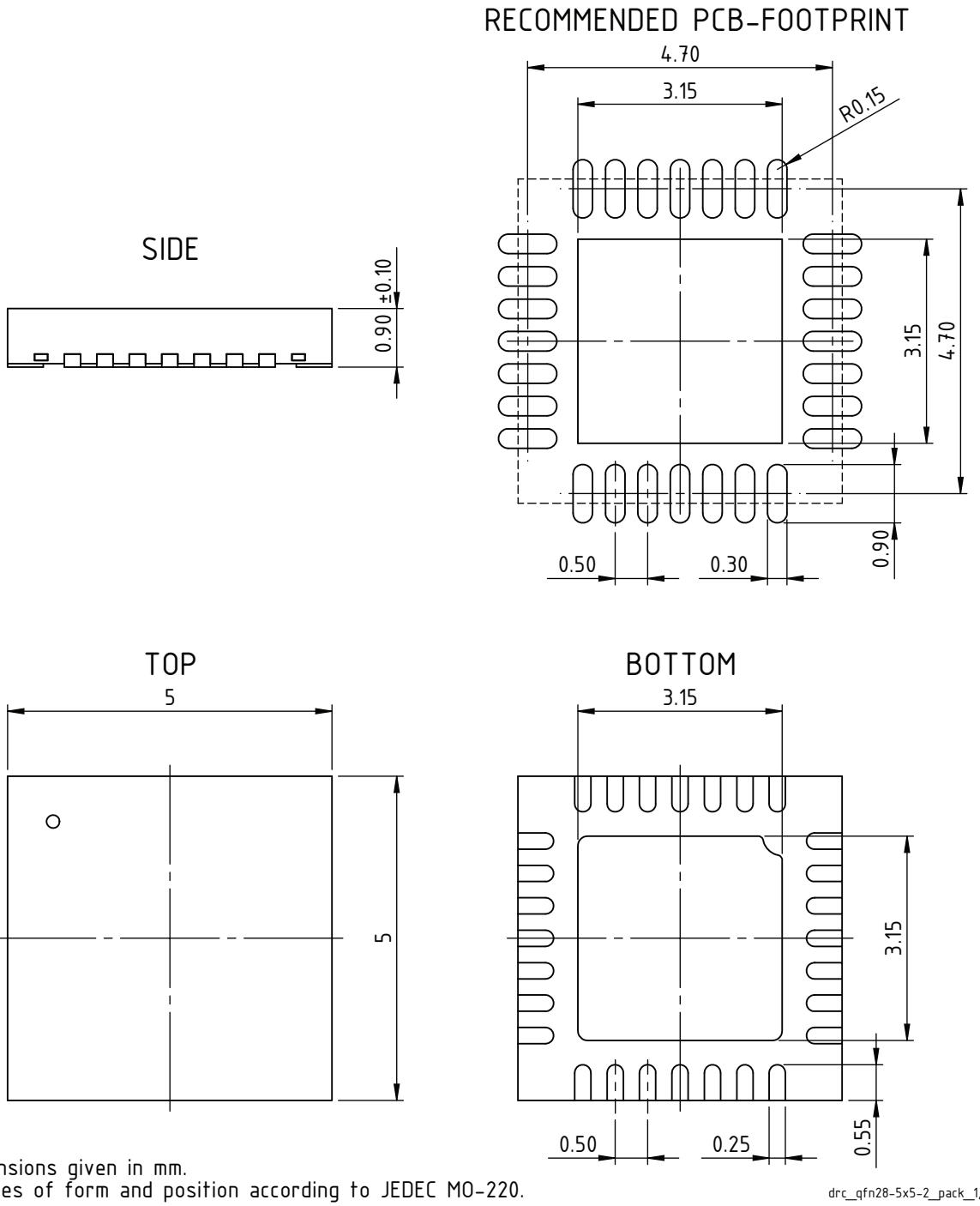
No.	Name	Function
		Serial Microcontroller Interface (SPI) (CFGSPI=1)
27	NCS	SPI Chip Select Input (NCS) (active low)
28	ALE	SPI Clock Input (SCLK)
1	DB0	SPI Serial Data Input (MOSI)
2	DB1	SPI Serial Data Output (MISO)
5	DB4	SPI2 Chip Select Input (NCS) (active low)
6	DB5	SPI2 Clock Input (SCLK)
7	DB6	SPI2 Serial Data Input (MOSI)
8	DB7	SPI2 Serial Data Output (MISO)
		Parallel Microcontroller Interface: Motorola Mode (CFGSPI=0, INT_NMOT=0)
25	NWR_E	Enable Input (active high)
26	NRD_RNW	Read/Not-Write Select Input
27	NCS	Chip Select Input (active low)
28	ALE	Address Latch Enable Input
1...8	DB0...DB7	Data Bus Input/Output
		Parallel Microcontroller Interface: Intel Mode (CFGSPI=0, INT_NMOT=1)
25	NWR_E	Write Input (active low)
26	NRD_RNW	Read Input (active low)
27	NCS	Chip Select Input (active low)
28	ALE	Address Latch Enable Input
1...8	DB0...DB7	Data Bus Input/Output

PIN FUNCTIONS

No.	Name	Function
		Supply Voltage
9	GND	Ground
10	VDD	+3 V . . . +5.5 V Supply Voltage
		Status and Frame Control
11	EOT	End-of-Transmission Output
12	GETSENS	Sensor Data Request Input
13	NER	Error Input/Output (active low)
14	n.c.	not connected
		BiSS/ SSI Interface
15	MA1	BiSS Clock Line Output
16	MA2_NMA1	BiSS Clock Line Output Ch. 2
17	SL1	BiSS Data Line Input
18	SL2_NSL1	BiSS Data Line Input Ch. 2
23	MO1	BiSS Data Line Output
24	MO2_NMO1	BiSS Data Line Output Ch. 2
		Configuration, Reset and Oscillator
19	INT_NMOT	Communication Mode Select Input (Intel=1, Motorola=0)
20	CFGSPI	MCU Interface Select Input (serial (SPI)=1, parallel=0)
21	NRES	Reset Input (active low)
22	CLK	External Oscillator Clock Input
BP		Backside Paddle (GND)

The *Backside Paddle* must be connected to GND.

PACKAGE DIMENSIONS QFN28 5 mm x 5 mm



All dimensions given in mm.
Tolerances of form and position according to JEDEC MO-220.

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ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VDD	Voltage at VDD		-0.3	6	V
G002	I(VDD)	Current in VDD		-20	30	mA
G003	V()	Voltage at all pins excluding VDD and GND	V() $\leq$ VDD + 0.3 V	-0.3	6	V
G004	I()	Current in all pins excluding VDD and GND		-10	10	mA
G005	V_{esd}()	ESD Susceptibility at all pins	HBM, 100 pF discharged through 1.5 Ω		2	kV
G006	Tj	Operating Junction Temperature	VDD = 3.0 V ... 4.5 V VDD = 4.5 V ... 5.5 V	-40 -40	125 140	°C °C
G007	Ts	Storage Temperature Range		-40	150	°C

THERMAL DATA

Operating Conditions: VDD = 3.0 V. . . 5.5 V

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Standard Operating Ambient Temperature Range		-40		85	°C
T02	Ta_{ET}	Extended Operating Ambient Temperature Range	VDD = 4.5 V ... 5.5 V available on request	-40		125	°C
T03	$R_{thjaQFN}$	Thermal Resistance Chip to Ambient	QFN28 package mounted on PCB, *Backside Paddle* at approx. 2 cm² cooling area		40		K/W

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 3.0 V. . . 5.5 V, Tj = -40. . . 125 °C, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VDD	Permissible Supply Voltage		3		5.5	V
002	I(VDD)	Supply Current in VDD	outputs not loaded, f(CLK) = 20 MHz			20	mA
003	Vc()hi	Clamp Voltage hi at all pins exc-luding VDD, GND, MA1, MO1, SL1	Vc()hi = V() - VDD, I() = 1 mA; outputs tristate	0.3		1.75	V
004	Vc()lo	Clamp Voltage lo at all pins exc-luding VDD, GND	I() = -1mA; outputs tristate	-1.6		-0.3	V
Microcontroller Interface: CFGSPI, INT_NMOT, NCS, ALE, NRD_RNW, NWR_E, DB7...0							
A01	Vs()hi	Saturation Voltage hi at DB7...0	Vs()hi = VDD - V(); VDD = 4.5 V, I() = -4 mA VDD = 3 V; I() = -2 mA			 0.4 0.4	 V V
A02	Vs()lo	Saturation Voltage lo at DB7...0	VDD = 4.5 V, I() = 4 mA VDD = 3 V, I() = 2 mA			0.4 0.4	V V
A03	Vt()hi	Threshold Voltage hi at CFGSPI, INT_NMOT, NCS, ALE, NRD_RNW, NWR_E, DB7...0				2	V
A04	Vt()lo	Threshold Voltage lo at CFGSPI, INT_NMOT, NCS, ALE, NRD_RNW, NWR_E, DB7...0		0.8			V
A05	Vt()hys	Threshold Voltage Hysteresis at CFGSPI, INT_NMOT, NCS, ALE, NRD_RNW, NWR_E, DB7...0		150	250		mV
A06	Ipd()	Pull-Down Current at CFGSPI, INT_NMOT, ALE, DB7...0	VDD = 4.5 V, V() = 1 V ... V(VDD) VDD = 3 V, V() = 1 V ... V(VDD)	6 3	30 30	60 60	µA µA
A07	Ipu()	Pull-Up Current at NCS, NRD_RNW, NWR_E	VDD = 4.5 V, V() = 0 V ... V(VDD) - 1 V VDD = 3 V, V() = 0 V ... V(VDD) - 1 V	-60 -60	-30 -30	-6 -3	µA µA
BiSS/SSI Interface							
B01	Rpu()	Pull-up Resistor at SL1, SL2_NSL1			50		kΩ
BiSS/SSI Interface: TTL/CMOS Mode (CFGIF = 00 or 01)							
B02	Vs()hi	Saturation Voltage hi at MA1, MO1, MA2_NMA1, MO2_NMO2	V() = V(VDD) - V(); VDD = 4.5 V, I() = -4 mA VDD = 3 V, I() = -2 mA			 0.4 0.4	 V V
B03	Vs()lo	Saturation Voltage lo at MA1, MO1, MA2_NMA1, MO2_NMO2	VDD = 4.5 V, I() = 4 mA VDD = 3 V, I() = 2 mA			0.4 0.4	V V
BiSS/SSI Interface: TTL Mode (CFGIF = 00)							
B04	Vt()hi	Threshold Voltage hi at SL1, SL2_NSL1				2	V
B05	Vt()lo	Threshold Voltage lo at SL1, SL2_NSL1		0.8			V
B06	Vt()hys	Hysteresis at at SL1, SL2_NSL1		150	300		mV
BiSS/SSI Interface: CMOS Mode (CFGIF = 01)							
B07	Vt()hi	Threshold Voltage hi at SL, SL2_NSL1			62	70	%VDD
B08	Vt()lo	Threshold Voltage lo at SL1, SL2_NSL1		33	39		%VDD
B09	Vt()hys	Hysteresis at at SL1, SL2_NSL1		0.7	1.13		V
BiSS/SSI Interface: RS422 Mode (CFGIF = 10, VDD = 4.5 V ... 5.5 V)							
B10	Vs()hi	Saturation Voltage hi at MA1, MO1, MA2_NMA1, MO2_NMO2	V() = V(VDD) - V(); I() = -50 mA			1.2	V
B11	Vs()lo	Saturation Voltage lo at MA1, MO1, MA2_NMA1, MO2_NMO2	I() = 50 mA			1.2	V

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 3.0 V. . . 5.5 V, Tj = -40. . . 125 °C, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
B12	Vcm()	Common Mode Input Voltage Range at SL1, SL2_NSL1	V()=[V(P) + V(N)]/2	0		3	V
B13	Vtdiff()	Threshold Voltage at SL - SL2_NSL1	V()=V(P) - V(N)	-300		300	mV
B14	Vthys()	Hysteresis Voltage at SL - SL2_NSL1	V()=V(P) - V(N)	75	150		mV
BiSS/SSI Interface: LVDS Mode (CFGIF = 11)							
B15	Vs()hi	Output Voltage hi at MA1, MO1, MA2_NMA1, MO2_NMO2	RL = 100 Ω VDD = 4.5 V ... 5.5 V VDD = 3.0 V ... 3.6 V	 1.25 1.0		 1.6 1.6	 V V
B16	Vs()lo	Output Voltage lo at MA1, MO1, MA2_NMA1, MO2_NMO2	RL = 100 Ω VDD = 4.5 V ... 5.5 V VDD = 3.0 V ... 3.6 V	 0.9 0.7		 1.125 1.125	 V V
B17	Vadiff	Differential Output Voltage at MA1 - MA2_NMA1, MO1 - MO2_NMO2	RL = 100 Ω VDD = 4.5 V ... 5.5 V VDD = 3.0 V ... 3.6 V	 250 220	 350 350	 450 450	 mV mV
B18	Vacm	Common Mode Output Voltage lo at MA1, MO1, MA2_NMA1, MO2_NMO2	RL = 100 Ω VDD = 4.5 V ... 5.5 V VDD = 3.0 V ... 3.6 V	 1.125 0.9	 1.2 1.15	 1.375 1.375	 V V
B19	Vcm()	Input Voltage Range at SL1, SL2_NSL1	V()=[V(P) + V(N)]/2 VDD = 4.5 V ... 5.5 V VDD = 3.0 V ... 3.6 V	 0.8 0.8		 3 1.8	 V V
B20	Vtdiff()	Threshold Voltage at SL1 - SL2_NSL1	V()=V(P) - V(N)	-150		150	mV
B21	Vthys()	Hysteresis Voltage at SL1 - SL2_NSL1	V()=V(P) - V(N) VDD = 4.5 V ... 5.5 V VDD = 3.0 V ... 3.6 V	 25 14	 70 40		 mV mV
Status and Frame Control: EOT, NER, GETSENS							
C01	Vs()hi	Saturation Voltage hi at EOT	Vs()hi = VDD - V(); VDD = 4.5 V, I() = -4 mA VDD = 3 V; I() = -2 mA			 0.4 0.4	 V V
C02	Vs()lo	Saturation Voltage lo at EOT, NER	VDD = 4.5 V, I() = 4 mA VDD = 3 V, I() = 2 mA			0.4 0.4	V V
C03	Vt()hi	Threshold Voltage hi at NER, GETSENS				2	V
C04	Vt()lo	Threshold Voltage lo at NER, GETSENS		0.8			V
C05	Vt()hys	Threshold Voltage Hysteresis at NER, GETSENS		150	250		mV
C06	Ipd()	Pull-Down Current at GETSENS	VDD = 4.5 V, V() = 1 V ... V(VDD) VDD = 3 V, V() = 1 V ... V(VDD)	6 3	30 30	60 60	µA µA
C07	Ipu()	Pull-Up Current at NER	V() = 0 V ... V(VDD) - 1 V	-950	-300	-35	µA
C08	Tw()	Minimum duration of GETSENS pulse		1/f(CLK)			
Oscillator: CLK							
D01	f(CLK)	Permissible external Clock Rate at CLK	Duty cycle 48% . . . 52%		20	25	MHz
D02	Vt(CLK)hi	Threshold Voltage hi				2	V
D03	Vt(CLK)lo	Threshold Voltage lo		0.4			V
D04	Vt(CLK)hys	Threshold Voltage Hysteresis		150	250		mV
D05	f(CLKI)	Internal Oscillator Clock Frequency	VDD = 4.5 V ... 5.5 V VDD = 3.0 V ... 3.6 V	12.5 10	20 15	25 22.5	MHz MHz
D06	Ipd()	Pull-Down Current at CLK	VDD = 4.5 V, V() = 1.5 V ... VDD VDD = 3 V, V() = 1.5 V ... VDD	6 3	30 30	60 60	µA µA

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 3.0 V. . . 5.5 V, Tj = -40. . . 125 °C, unless otherwise stated

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Reset: NRES							
E01	VDDoff	Undervoltage Reset	VDD decreasing	1.4		2.6	V
E02	VDDon	Undervoltage Release	VDD increasing	1.6		2.8	V
E03	VDDhys	Undervoltage Hysteresis	VDDhys = VDDon - VDDoff	200			mV
E04	Vt()hi	Threshold Voltage hi				2	V
E05	Vt()lo	Threshold Voltage lo		0.4			V
E06	Vt()hys	Threshold Voltage Hysteresis		150	250		mV
E07	Ipd()	Pull-Down Current	V() = 1.5 V ... VDD	4	35	70	µA
E08	td()res	Required Reset Pulse Duration	At NRES	250			ns

OPERATING REQUIREMENTS: Parallel Microcontroller Interface (Intel Mode)

Operating conditions: CFGSPI = 0, INT_NMOT = 1, VDD = 3.0 ... 5.5 V, Tj = -40 ... 125 °C
Io input level = 0 ... 0.8 V, hi input level = 2.0 V ... VDD, lo output level = 0 ... 0.4 V, hi output level = 2.4 V ... VDD
Alias: NRD = NRD_RNW, NWR = NWR_E

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
I001	tsCA	Setup Time: NCS lo before ALE hi→lo		10		ns
I002	tsDA	Setup Time: Data stable before ALE hi→lo		15		ns
I003	thDA	Hold Time: Data stable after ALE hi→lo		15		ns
I004	tAh	Signal Duration: ALE at high level		10		ns
I005	tsAR	Setup Time: ALE lo before NRD hi→lo		10		ns
I006	thAR	Hold Time: ALE lo after NRD lo→hi	NCS = lo	10		ns
I007	tRl	Signal Duration: NRD at low level	NCS = lo	10		ns
I008	tpRD1	Propagation Delay: Data stable after NRD hi→lo	NCS = lo, CL = 5 pF, VDD ≥ 4.5 V, Tj = -40 ... 85 °C CL = 5 pF, VDD ≥ 4.5 V CL = 50 pF, VDD ≥ 4.5 V, Tj = -40 ... 85 °C CL = 50 pF, VDD ≥ 4.5 V CL = 5 pF, Tj = -40 ... 85 °C CL = 5 pF CL = 50 pF, Tj = -40 ... 85 °C CL = 50 pF		 23 25 29 33 38 42 49 54	 ns ns ns ns ns ns ns ns
I009	tpRD2	Propagation Delay: Data bus high impedance after NRD lo→hi	NCS = lo, CL = 50 pF		25	ns
I010	thCR	Hold Time: NCS lo after NRD lo→hi		10		ns
I011	tsAW	Setup Time: ALE lo before NWR hi→lo		10		ns
I012	thAW	Hold Time: ALE lo after NWR lo→hi	NCS = lo	10		ns
I013	tWl	Signal Duration: NWR at low level	NCS = lo	10		ns
I014	tsDW	Setup Time: Data stable before NWR lo→hi	NCS = lo	15		ns
I015	thDW	Hold Time: Data stable after NWR lo→hi	NCS = lo	15		ns
I016	thCW	Hold Time: NCS lo after NWR lo→hi		10		ns

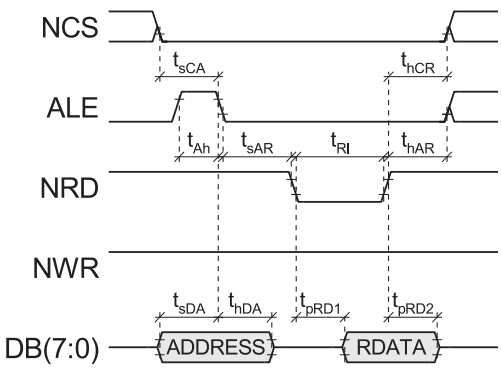


Figure 3: Read cycle (Intel mode)

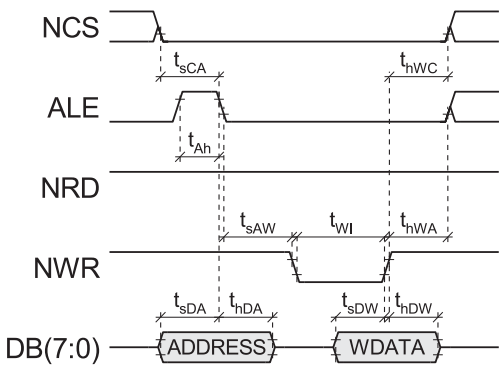


Figure 4: Write cycle (Intel mode)

OPERATING REQUIREMENTS: Parallel Microcontroller Interface (Motorola Mode)

Operating conditions: CFGSPI = 0, INT_NMOT = 0 VDD = 3.0 ... 5.5 V, Tj = -40 ... 125 °C;
lo input level = 0 ... 0.8 V, hi input level = 2.0 V ... VDD, lo output level = 0 ... 0.4 V, hi output level = 2.4 V ... VDD
Alias: RNW = NRD_RNW, E = NWR_E

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
I101	tsCA	Setup Time: NCS lo before ALE hi→lo		10		ns
I102	tsDA	Setup Time: Data stable before ALE hi→lo		15		ns
I103	thDA	Hold Time: Data stable after ALE hi→lo		15		ns
I104	tAh	Signal Duration: ALE at high level		10		ns
I105	tsAE	Setup Time: ALE lo before E lo→hi		10		ns
I106	thAE	Hold Time: ALE lo after E hi→lo	NCS = lo	10		ns
I107	tsRE	Setup Time: RNW stable before E lo→hi	NCS = lo	10		ns
I108	thRE	Hold Time: RNW stable after E hi→lo	NCS = lo	10		ns
I109	tEh	Signal Duration: E at high level	NCS = lo	10		ns
I110	tpED1	Propagation Delay: Data stable after E lo→hi	NCS = lo, CL = 5 pF, VDD ≥ 4.5 V, Tj = -40 ... 85 °C CL = 5 pF, VDD ≥ 4.5 V CL = 50 pF, VDD ≥ 4.5 V, Tj = -40 ... 85 °C CL = 50 pF, VDD ≥ 4.5 V CL = 5 pF, Tj = -40 ... 85 °C CL = 5 pF CL = 50 pF, Tj = -40 ... 85 °C CL = 50 pF		 23 25 29 33 38 42 49 54	 ns ns ns ns ns ns ns ns
I111	tpED2	Propagation Delay: Data bus high impedance after E hi→lo	NCS = lo, CL = 50 pF		25	ns
I112	tsDE	Setup Time: Data stable before E hi→lo	NCS = lo	15		ns
I113	thDE	Hold Time: Data stable after E hi→lo	NCS = lo	15		ns
I114	thCE	Hold Time: NCS lo after E hi→lo		10		ns

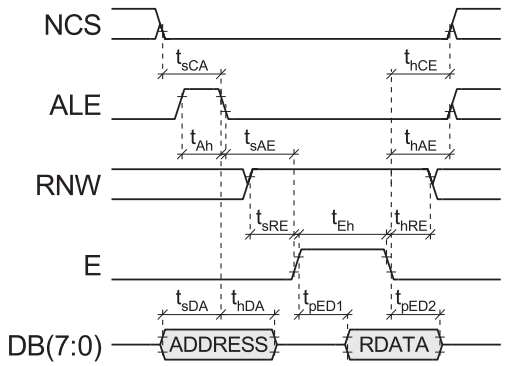


Figure 5: Read cycle (Motorola mode)

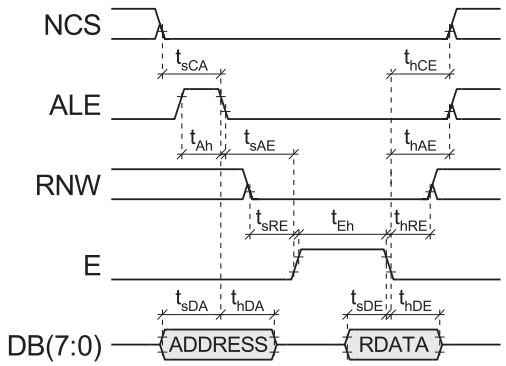


Figure 6: Write cycle (Motorola mode)

OPERATING REQUIREMENTS: Serial Microcontroller Interface (SPI)

Operating conditions: CFGSPI = 1 VDD = 3.0 ... 5.5 V, Tj = -40 ... 125 °C;
lo input level = 0 ... 0.8 V, hi input level = 2.0 V ... VDD, lo output level = 0 ... 0.4 V, hi output level = 2.4 V ... VDD
Alias: NCS = NCS/DB4, SCLK = ALE/DB5, MOSI = DB0/DB6, MISO = DB1/DB7

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
I201	tsCS	Setup Time: NCS lo before SCLK lo→hi		10		ns
I202	thCS	Hold Time: NCS lo after SCLK hi→lo		10		ns
I203	tSl	Signal Duration: SCLK lo		10		ns
I204	tSh	Signal Duration: SCLK hi	 during SPI command 'ReadData' between address and data	10 100		ns ns
I205	tsDS	Setup Time: MOSI stable before SCLK lo→hi		7.5		ns
I206	thDS	Hold Time: MOSI stable after SCLK lo→hi		7.5		ns
I207	tpSD	Propagation Delay: MISO stable after SCLK hi→lo	CL = 5 pF, VDD ≥ 4.5 V, Tj = -40 ... 85 °C CL = 5 pF, VDD ≥ 4.5 V CL = 50 pF, VDD ≥ 4.5 V, Tj = -40 ... 85 °C CL = 50 pF, VDD ≥ 4.5 V CL = 5 pF, Tj = -40 ... 85 °C CL = 5 pF CL = 50 pF, Tj = -40 ... 85 °C CL = 50 pF		23 25 29 33 38 42 49 54	ns ns ns ns ns ns ns ns
I208	tpCD	Propagation Delay: MISO high impedance after NCS lo→hi	CL = 50 pF		25	ns
I209	tCh	Signal Duration: NCS hi		10		ns

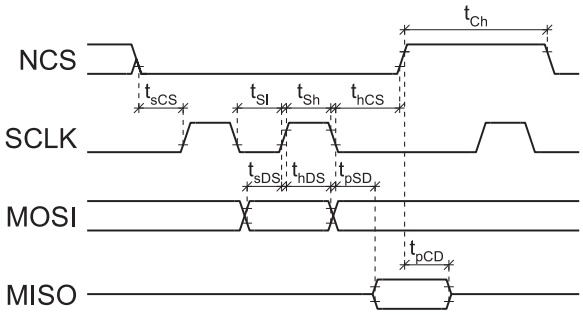


Figure 7: Read/write access (SPI mode)

OPERATING REQUIREMENTS: BiSS Interface - BiSS B/C frame

Operating conditions: register bit SELSSI = 0 VDD = 3.0 . . . 5.5 V, Tj = -40 . . . 125 °C
Alias: MA = MA1/MA2_NMA1, SL = SL1/SL2_NSL1

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
Frame						
I301	TMAS	Clock Period	Single-cycle clock frequency selected with FREQS according to Table 35 on page 30	2	320	1/f(CLK)
I302	tMASl	Clock Signal Lo Level Duration		50	50	% TMAS
I303	tMASh	Clock Signal Hi Level Duration		50	50	% TMAS
I304	tpLine	Permissible Line Delay		0	indefinite	
I305	Δ tpL	Permissible Propagation Delay of Subsequent Clock Cycles vs. 1st Clock Cycle	Δ tpL = max(|tpLine - tpLx|); x= 1 ... n		25	% TMAS
I306	Ttos	Permissible Timeout (Slave)		55		% TMAS

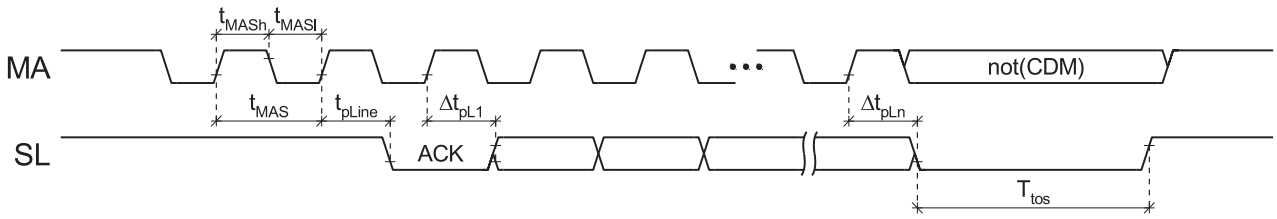


Figure 8: Timing diagram BiSS B/C frame

SLx line sampling
Line delays longer than one clock cycle are permissible in BiSS.
Within one MA clock cycle four equally distributed sampling points are used to evaluate the overall delay from the second rising edge at MAx to the first falling edge at SLx (ACK).
Refer also to the characteristics in BiSS C Protocol Description.

OPERATING REQUIREMENTS: BiSS Interface - BiSS B register data cycle

Operating conditions: register bit SELSSI = 0 VDD = 3.0...5.5 V, Tj = -40...125 °C
Alias: MA = MA1/MA2_NMA1, SL = SL1/SL2_NSL1

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
I401	TMAR	Clock Period	Register communication clock frequency selected with FREQR according to Table 36 on page 30	2	256	TMAS
I402	tMA0h	"Logic 0" Hi Level Duration		25	25	% TMAR
I403	tMA1h	"Logic 1" Hi Level Duration		75	75	% TMAR
I404	tMAth	Clock Signal Hi Level Duration	register data readout	50	50	% TMAR
I405	tsSM	Setup Time: SL stable before MA lo→hi		30		ns
I406	thSM	Hold Time: SL stable after MA lo→hi		0		ns
I407	Ttor	Permissible Timeout (Slave)	For Ttos details see item i306 BiSS Frame	80		% TMAR

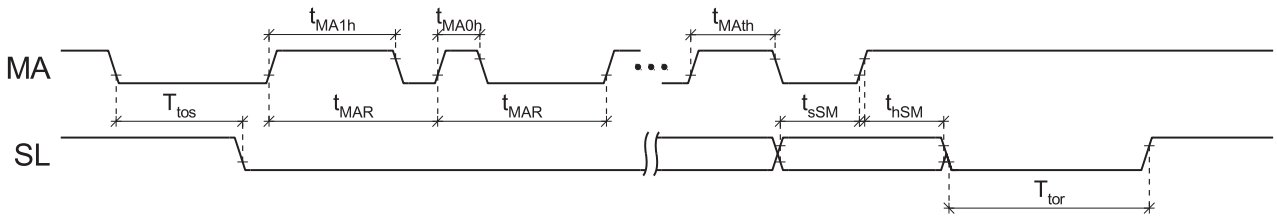


Figure 9: Timing diagram BiSS B register access

OPERATING REQUIREMENTS: BiSS Interface - SSI mode

Operating conditions: register bit SELSSI = 1; VDD = 3. . . 5.5 V, Tj = -40. . . 125 °C
Alias: MA = MA1/MA2_NMA1, SL = SL1/SL2_NSL1

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
I501	TMAS	Clock Period	Single-cycle clock frequency selected with FREQS according to Table 35 on page 30	2	320	1/f(CLK)
I502	tMASh	Clock Signal Hi Level Duration		50	50	% TMAS
I503	tMASl	Clock Signal Lo Level Duration		50	50	% TMAS
I504	tsSM	Setup Time: SLx stable before MAx lo→hi		30		ns
I505	thSM	Hold Time: SLx stable after MAx lo→hi		0		ns
I506	Ttos	Permissible Timeout (Slave)		55		% TMAS

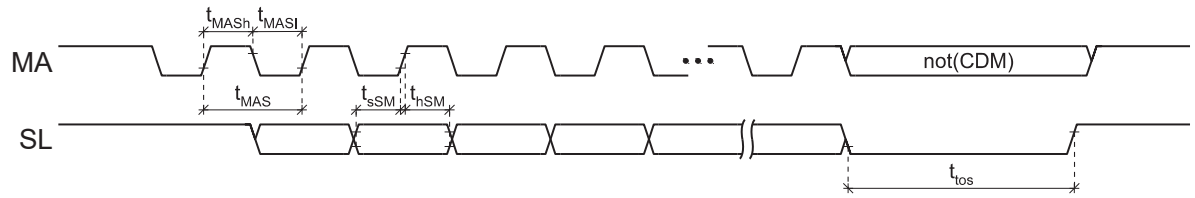


Figure 10: Timing diagram SSI mode

SLx line sampling
In SSI interface mode SLx values are sampled with the rising edge at MAx. An overall delay of the sensor response to the clock at MAx, caused by process times in the sensor or transmission times, is permissible up to the length of one clock cycle minus tsSM.

FUNCTIONAL DESCRIPTION

The open source BiSS Interface Protocol implements a realtime interface for digital, serial and secure communication between drive, sensor and actuator. In the point-to-point configuration BiSS uses one clock line MAx from the master to the sensor and one data line SLx from the sensor to the master (see Figure 1). A device may contain multiple slaves. The data input pin SLI of the last slave is set to digital low. The slaves are daisy-chained (SLO → SLI) and the data output pin SLO of the first slave is directly connected to the master. A data line from the master to the slave is not mandatory.
In the bus configuration the data output line MO is used to transfer actuator data from the master to the slaves (see figure 2). The BiSS protocol describes cyclic data frames and differentiates between process data and control data. Process data are completely transmitted in each frame (SCD) used as actuator or sensor data and control data are transmitted one bit per frame (CD) used for commands and register access.

BiSS C

BiSS C Frame

The BiSS C Frame starts with a digital high on the clock line MAx and is notified by iC-MB4 with a falling edge at the pin EOT. On the first falling edge of MAx all slaves check the SLI pin for a digital low determining the last slave. With the first rising edge at MAx all sensors start calculating their sensor data. The second rising edge of MAx forces all slaves to acknowledge the BiSS C frame with a falling edge at SLO. The master uses the acknowledge to measure the line delay. When the sensor data calculation is finished, the last slave in the chain generates the start bit which will be passed synchronously through all slaves to the master. If the master data output MOx is used, the start bit delay has to be configured to ensure sufficient processing time regarding sensor data for all slaves. Subsequent to the start bit follows one control data bit for all slaves (CDS) which is set according to the rules of the control frame. After the CDS bit, the process data including sensor and actuator data is sent with the most significant bit (MSB) first. At the end, the master sends it's control data bit (CDM) inverted on the clock line MAx to conclude the BiSS C Frame.
During processing the frame all slaves observe the MAx clock line and change into the timeout state, if MAx is stable for a specific time defined within each slave. In the timeout state, only the last slave forces it's SLO pin to digital high. The other slaves in the chain connect SLI and SLO to signal the master that all slaves are in the timeout state. After detecting the slave's timeout with SLO = 1, the master may changes the MAx clock line to digital high or keeps the clock line constant until the next frame begins. This is advantageous if the BiSS C Frame has not been clocked out completely, e.g. for a fast configuration phase and high control data transmission rates. The difference is indicated in Figures 11 and 12.

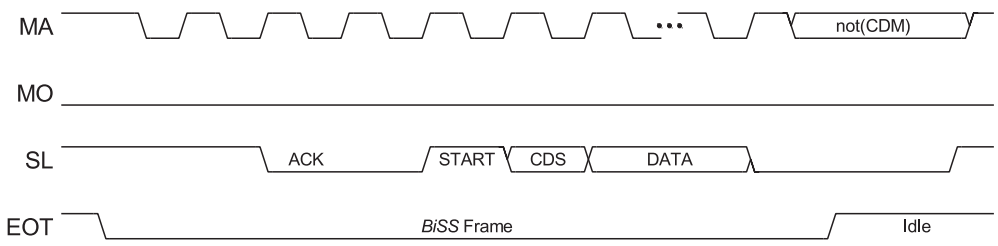


Figure 11: BiSS C frame in point-to-point configuration

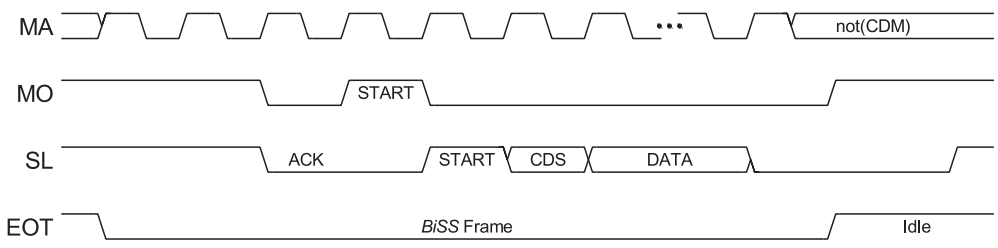


Figure 12: BiSS C frame in bus configuration

BiSS C & Extended SSI Register Communication
The extended SSI operation enables the BiSS C register write access to SSI slaves. The master is able to transmit a BiSS C register write access to the slave without the slave's CDS feedback. The master cannot verify that the BiSS C register write access to the slave did succeed. At the end of the SCD frame the master sends the CDM bit inverted on the MA clock line.

BiSS C Initialization Sequence
An initialization (INIT) sequence is necessary, if the last slave in the point-to-point configuration is not defined and the data line SLx is digital low. In the initialization sequence, two digital low pulses are generated at MAx. The slave(s) should answer with a falling-edge after the second pulse and with a rising-edge at SLx after the BiSS timeout. The time between the second rising-edge at MAx and the falling-edge at SLx is measured as line delay and stored in the single-cycle data RAM, see chapter on page 32.

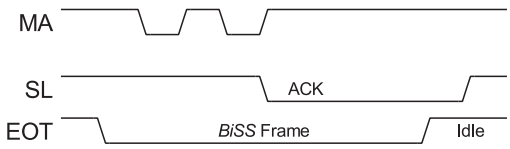


Figure 13: BiSS C initialization sequence

BiSS B

BiSS B Register Communication
For the BiSS B protocol the register communication is started by a timing condition and a handshake at the beginning of the frame (see Figure 14). Alternatively, the register communication can be activated at the beginning of the frame with a connected MO line (slave ID "0" remains unused).

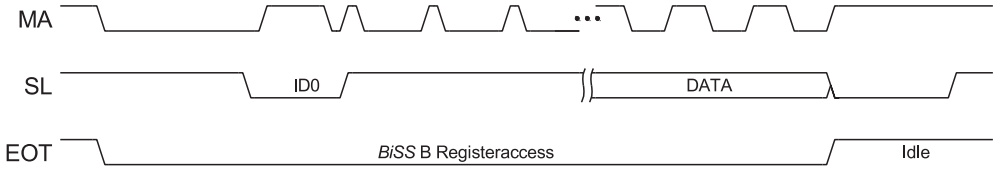


Figure 14: BiSS B register access (EN_MO = 0)

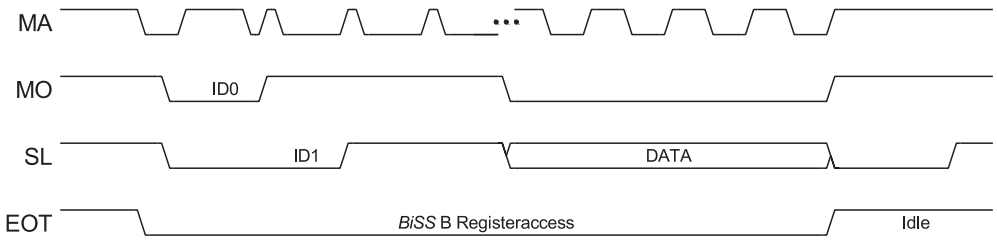


Figure 15: BiSS B register access (EN_MO = 1)

BiSS B Initialization Sequence
In the BiSS B initialization sequence (INIT) only the timing handshake with the first falling edge at MA is executed.

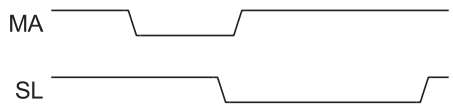


Figure 16: BiSS B initialization sequence

MICROCONTROLLER INTERFACE

The iC-MB4 supports a parallel and a serial microcontroller interface (SPI). The desired interface is selected with input pin CFGSPI. Different interfaces cannot be used at the same time.

CFGSPI	Interface
0	Parallel Microcontroller Interface
1	Serial Microcontroller Interface (SPI)

Table 1: Microcontroller interface

Parallel Microcontroller Interface

With pin CFGSPI = 0 the 8 bit parallel microcontroller interface is selected in which the bidirectional data bus alternately transmits addresses and data in blocks of 8 bits. Pin INT_NMOT selects between two different communication modes. In both cases, a digital low at the pin NCS activates the interface and the pin ALE is used to store the address. The data pins are tristate while deactivated via NCS.

INT_NMOT	Mode
0	Motorola 68HC11
1	Intel 8051

Table 2: Parallel communication modes (CFGSPI = 0)

Motorola Communication Mode 68HC11
If pin INT_NMOT = 0, the motorola communication mode is selected. The pin NRD_RNW (Read-not-Write) chooses between read and write access and the pin NWR_E (active high) executes the access (see Figure 17). Refer to OPERATING REQUIREMENTS on page 10 for timings.

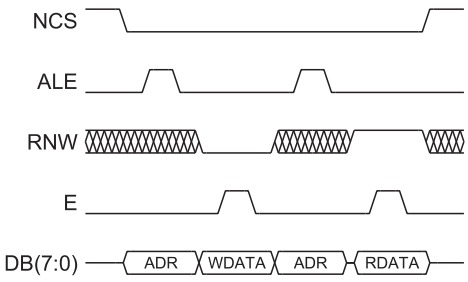


Figure 17: Motorola communication mode

Intel Communication Mode 8051
The Intel 8051 communication mode uses NWR_E (active low) as write enable input and NRD_RNW (active low) as read enable input. It is selected with INT_NMOT = 1 (see Figure 18). Refer to OPERATING REQUIREMENTS on page 9 for timings.

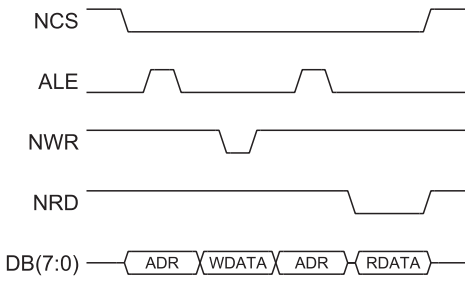


Figure 18: Intel communication mode

Serial Microcontroller Interface (SPI)

If the pin CFGSPI = 1, the SPI serial microcontroller interfaces with polarity = 0 and phase = 0 are selected. When operating in conjunction with an SPI controller, the pin ALE is used as a clock input (SCLK), the pin NCS as an enable input (NCS), the pin DB0 is used as the data input (MOSI) and the pin DB1 is used as the data output (MISO). Data is transmitted serially in successive blocks of 8 bits starting with the command. Depending on the commands, the following blocks contain an address and one or more data bytes (see figure 19). Refer to OPERATING REQUIREMENTS on page 11 for timings.

SPI Commands
Six SPI commands are available:

SPI Commands		
Opcode	Description	Address
0x02	Write Registers	Transmitted
0x03	Read Registers	Transmitted
0x05	Read Status	0xF0
0x07	Write Instruction	0xF4
0x09	Read Registers 0	0x00
0x0B	Write Registers 0	0x00

Table 3: Command Codes for SPI

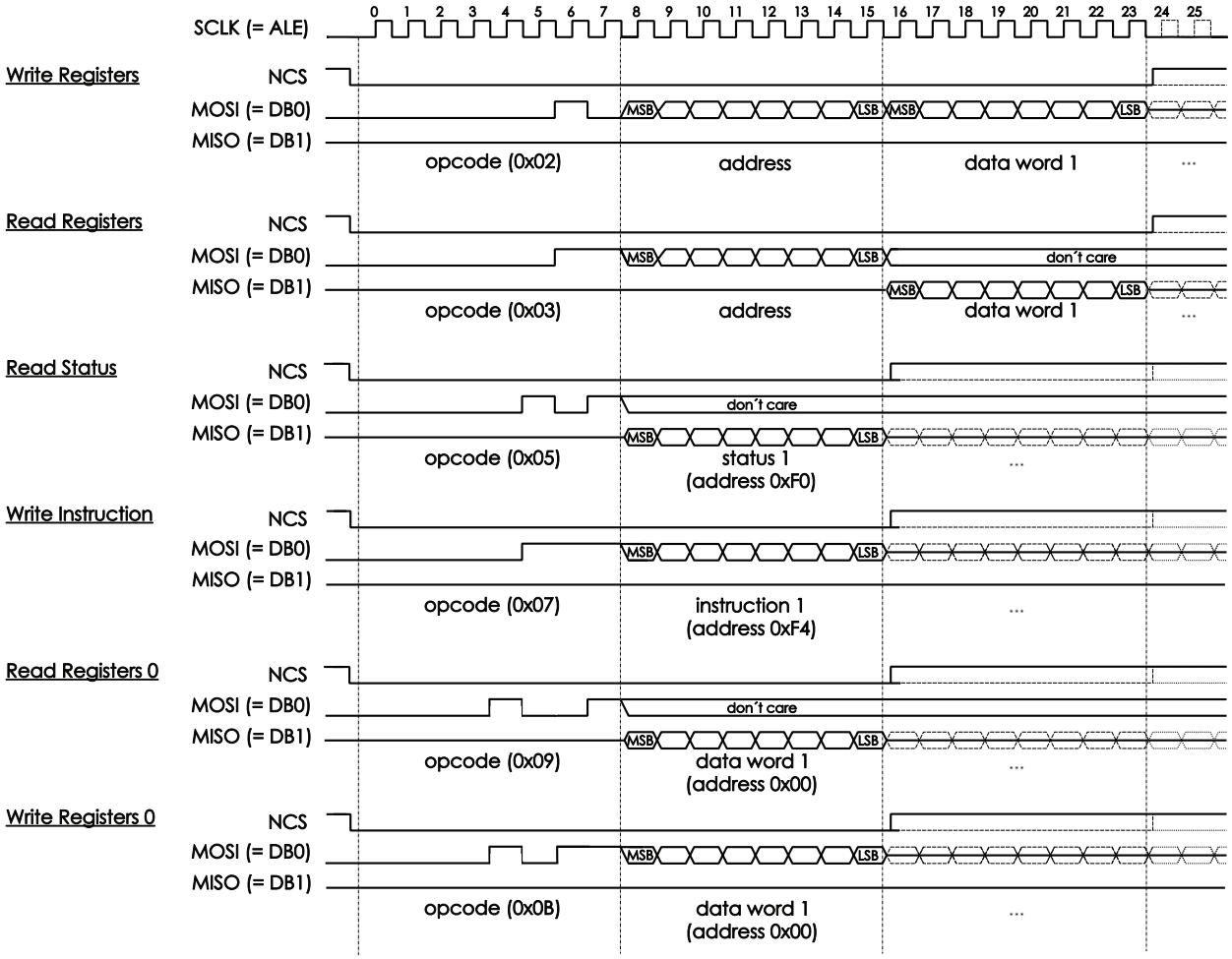


Figure 19: SPI transmission protocol (polarity 0, phase 0)

SPI Command: Write Registers (0x02)
The SPI Command Write Registers can be used to write data to iC-MB4's registers. The microcontroller sends the opcode 0x02 on MOSI that is followed by the register address and the data value. It is possible to transmit several bytes of data consecutively, if the NCS signal remains digital low and ALE/SCLK is clocked continuously. The address is internally increased by 1 for each transmitted byte starting at the transmitted address respectively.

SPI Command: Read Registers (0x03)
The SPI Command Read Registers can be used to read data from iC-MB4's registers. The microcontroller sends the opcode 0x03 on MOSI that is followed by the register address. iC-MB4 responds after the address byte with the registers data value. It is possible to transmit several bytes of data consecutively, if the NCS signal remains digital low and ALE/SCLK is clocked continuously. The address is internally increased by 1 for each transmitted byte starting at the transmitted address respectively. A delay between the address and the first register's data is necessary (refer to I204 on page 11).

SPI Command: Read Status (0x05)
The SPI Command Read Status can be used to read iC-MB4's status registers starting at address 0xF0. It is not necessary to send the address. After the microcontroller sends the opcode 0x05 on MOSI, iC-MB4 responds directly with the register's data value on MISO. It is possible to transmit several bytes of data consecutively, if the NCS signal remains digital low and ALE/SCLK is clocked continuously. The address is internally increased by 1 for each transmitted byte starting at the transmitted address respectively.

SPI Command: Write Instruction (0x07)
The SPI Command Write Instruction can be used to write into iC-MB4's instruction registers starting at address 0xF4. It is not necessary to send the address. The data is transmitted directly after the opcode 0x07 on MOSI. It is possible to transmit several bytes of data consecutively, if the NCS signal remains digital low and ALE/SCLK is clocked continuously. The address is internally increased by 1 for each transmitted byte starting at the transmitted address respectively.

SPI Command: Read Registers 0 (0x09)
The SPI Command Read Registers 0 can be used to read data from iC-MB4's registers starting at address 0x00. It is not necessary to send the address. After the microcontroller sends the opcode 0x09 on MOSI, iC-MB4 responds directly with the register's data value on MISO. It is possible to transmit several bytes of data consecutively, if the NCS signal remains digital low and ALE/SCLK is clocked continuously. The address is internally increased by 1 for each transmitted byte starting at the transmitted address respectively.

SPI Command: Write Registers 0 (0x0B)
The SPI Command Write Registers 0 can be used to write data to iC-MB4's registers starting at address 0x00. The data is transmitted directly after the opcode 0x0B on MOSI. It is possible to transmit several bytes of data consecutively, if the NCS signal remains digital low and ALE/SCLK is clocked continuously. The address is internally increased by 1 for each transmitted byte starting at the transmitted address respectively.

Additional Serial Microcontroller Interface (SPI2)
If the SPI serial microcontroller interface is activated with pin CFGSPI = 1, an additional SPI interface can be enabled with pin NWR_E = 0 for dedicated register access with reduced function set.

NWR_E	Mode
0	Optional SPI2 (polarity = 0, phase = 0), if CFGSPI = 1

Table 4: Additional serial interface (SPI2)

Pin DB5 is used as a clock input (SCLK), the pin DB4 as an enable input (NCS), the pin DB6 is used as the data input (MOSI) and the pin DB7 is used as the data output (MISO).

The additional SPI interface is available for an exclusive read access to the single-cycle data RAM of the slaves 5 to 8 with the commands Read Registers and Read Registers 0. Access to the status, the instruction and the parameter registers is not possible.

SPI2 Commands		
Opcode	Description	Address
0x03	Read Registers	Transmitted
0x09	Read Registers 0	0x20

Table 5: Command Codes for SPI2

Note: This 2nd SPI can only be used to read SCDATAx from 0x20 . . . 0x3F. It is not possible to read the status or to access the configuration RAM via SPI2.

CONFIGURATION PARAMETERS

REGISTER MAP

OVERVIEW								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Single-Cycle Data: Data RAM (Sensor and Actuator Data)								
0x00	SCDATA1(7:0)							
0x01 ...0x07	SCDATA1(63:8)							
0x08 ...0x3F	SCDATA2(63:0) ... SCDATA8(63:0)							
0x40 ...0x7F	– *							
Control Communication: Register Data RAM								
0x80 †	RDATA1(7:0)							
0x80 ‡	IDS(7:0)							
0x81 ...0xBF	RDATA2(7:0) ... RDATA64(7:0)							
Single-Cycle Data: Data Channel Configuration 1								
0xC0	GRAYS1 / LSTOP1	ENSCD1	SCDLEN1(5:0)					
0xC1	SELCRCS1	SCRCLEN1(6:0) / SCRCPOLY1(7:1)						
0xC2	SCRCSTART1(7:0)							
0xC3	SCRCSTART1(16:8)							
0xC4 ...0xDF	Configuration Slave 2(31:0) ... Configuration Slave 8(31:0)							
Control Communication: Configuration								
0xE0	– *							
0xE1	– *							
0xE2	WNR	REGADR(6:0)						
0xE3	– *	REGNUM(5:0)						
0xE4	– *						CHSEL(1:0)	
0xE5 †	CTS	REGVERS	SLAVEID(2:0)			– *	EN_MO	HOLDCDM
0xE5 ‡	CTS	REGVERS	CMD(1:0)		IDA_TEST	– *	EN_MO	HOLDCDM
Frame Control: Master Configuration								
0xE6	FREQR(2:0)			FREQS(4:0)				
0xE7	– *						NOCRC	SINGLEBANK
0xE8	FREQAGS(7:0)							
0xE9	MO_BUSY(7:0)							
0xEA	REVISION(7:0)§							
0xEB	VERSION(7:0)§							

* Reserved or unused register bits highlighted as '–' need to be written with 0 if a byte wide register write access is required.
† Using register communication in control communication (CTS = 1).
‡ Using BiSS commands in control communication (CTS = 0).
§ Register bits with constant '0' or '1' are ROM-based values and can not be changed through writing.

OVERVIEW								
Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BiSS/SSI Interface								
0xEC	'0'	'0'	'0'	SLAVELOC5	'0'	'0'	'0'	'1'
0xED	– *				CFGCH2(1:0)		CFGCH1(1:0)	
0xEE	– *							
Single-Cycle Data: Data Channel Configuration 2								
0xEF	ACTnSENS(8:1)							
Status 1								
0xF0	nERR	nAGSERR	nDELAYERR	nSCDERR	nREGERR	REGEND	'1'	EOT
0xF1	SVALID4	'0'	SVALID3	'0'	SVALID2	'0'	SVALID1	'0'
0xF2	SVALID8	'0'	SVALID7	'0'	SVALID6	'0'	SVALID5	'0'
0xF3	CDMTIME-OUT	CDSSEL	REGBYTES(5:0)					
Frame Control: Data Acquisition								
0xF4	BREAK	HOLDBANK	SWBANK	INIT	INSTR(2:0)			AGS
0xF5	MAVO	MAFO	MAVS	MAFS	CFGIF(1:0)		ENTEST	CLKENI
0xF6	– *	– *	– *	– *	– *	– *	– *	– *
0xF7	– *	– *	– *	– *	– *	– *	– *	– *
Status 2								
0xF8	'0'	'1'	'0'	'1'	CDS2	SL2	CDS1	SL1
0xF9	'0'	'1'	'0'	'1'	'0'	'1'	'0'	'1'
0xFA	– *	– *	– *	– *	– *	– *	– *	– *
0xFB	– *	– *	– *	– *	– *	– *	– *	SWBANKFAIL
Reserved								
0xFC ...0xFF	– *	– *	– *	– *	– *	– *	– *	– *

Table 6: Register layout

iC-MB4 does reset all RAM registers to '0' on a power on reset.

OSCILLATOR

The system clock f_{CLK} (typically 20 MHz) is either generated by the internal oscillator (refer to El.Char. f(CLKI)) or by an external oscillator connected to pin CLK (refer to El.Char. f(CLK)). CLKENI is used to select the oscillator.

Since single-cycle data clock frequency (f_{MA} configured with FREQS) and frame repetition rate (configured with FREQAGS) directly depend on the system clock f_{CLK}, it is recommended to apply a precise external oscillator to pin CLK in high-performance applications.

CLKENI	Addr. 0xF5;	Bit 0	R/W
Code	Function		
0	External oscillator via pin CLK (refer to f(CLK))		
1	Internal oscillator (refer to f(CLKI))		

Table 7: System clock (f_{CLK}) source

BiSS/SSI INTERFACE

iC-MB4 assembled in the QFN28 package provides two options. Option one enables a second physical BiSS/SSI channel and option two enables one BiSS/SSI channel with differential line drivers/receivers (drivers for pins MAx and MOx, receiver for SLx).

The protocol for each physical channel is separately defined with CFGCHx.

CFGCH1	Addr. 0xED;	Bit 1:0	R/W
CFGCH2	Addr. 0xED;	Bit 3:2	R/W
Code	Function		
0x00	BiSS B		
0x01	BiSS C		
0x02	SSI		
0x03	Channel is not used (no device connected)		
Notes	The BiSS C Protocol Description is available at www.biss-interface.com.		

Table 8: Protocol configuration for channel 1 and 2

The interface is configured with CFGIF.

CFGIF	Addr. 0xF5;	Bit 3:2	R/W
Code	Function		
0x00	TTL		
0x01	CMOS		
0x02	RS422 (differential)		
0x03	LVDS (differential)		
Notes	The RS422 interface requires VDD = 4.5 V ... 5.5 V.		

Table 9: Configure physical interface

Up to eight logical single-cycle data channels can be assigned to one physical channel. If two physical BiSS/SSI channels are used, SLAVELOC5 is set to 1. SLAVELOC5 = 1 assigns single-cycle data channels 1 ... 4 to physical channel 1 and single-cycle data channels 5 ... 8 to physical channel 2.

SLAVELOC5	Addr. 0xEC;	Bit 4	R/W
Code	Function		
0	If one physical BiSS/SSI channel is used. Logical single-cycle data channels 5 ... 8 are assigned to physical BiSS/SSI channel 1.		
1	If two physical BiSS/SSI channels are used. Logical single-cycle data channels 5 ... 8 are assigned to physical BiSS/SSI channel 2.		

Table 10: Slave location

SINGLE-CYCLE DATA

DATA CHANNEL CONFIGURATION

For proper sensor and actuator data transmission, it is necessary that the single-cycle data channel configuration of iC-MB4 matches the data channel parameters of the connected BiSS/SSI slave(s). Typically for each slave one single-cycle data channel is configured. The following parameters have to be considered for each data channel:

- ENSCDx configures, if single-cycle data is transmitted.
- SCDLENx configures the single-cycle data length.
- SELCRCSx configures, if a predefined or individual CRC polynomial is used.
- SCRCLENx configures the predefined CRC polynomial.
- SCRCPOLYx configures an individual CRC polynomial.
- SCRCSTARTx configures the CRC start value.
- ACTnSENSx configures, if the slave is a sensor or actuator.
- LSTOPx configures, if a STOP bit is transmitted before actuator data.
- GRAYSx configures, if single-cycle data is binary or GRAY coded for SSI slaves.

ENSCD1	Addr. 0xC0;	Bit 6	R/W
ENSCD2	Addr. 0xC4;	Bit 6	R/W
ENSCD3	Addr. 0xC8;	Bit 6	R/W
ENSCD4	Addr. 0xCC;	Bit 6	R/W
ENSCD5	Addr. 0xD0;	Bit 6	R/W
ENSCD6	Addr. 0xD4;	Bit 6	R/W
ENSCD7	Addr. 0xD8;	Bit 6	R/W
ENSCD8	Addr. 0xDC;	Bit 6	R/W

Code	Function
0	Single-cycle data not available
1	Single-cycle data available

Table 11: Enable single-cycle data for slave x

SCDLEN1	Addr. 0xC0;	Bit 5:0	R/W
SCDLEN2	Addr. 0xC4;	Bit 5:0	R/W
SCDLEN3	Addr. 0xC8;	Bit 5:0	R/W
SCDLEN4	Addr. 0xCC;	Bit 5:0	R/W
SCDLEN5	Addr. 0xD0;	Bit 5:0	R/W
SCDLEN6	Addr. 0xD4;	Bit 5:0	R/W
SCDLEN7	Addr. 0xD8;	Bit 5:0	R/W
SCDLEN8	Addr. 0xDC;	Bit 5:0	R/W

Code	Single-cycle data length
0x00	1
. . .	Code + 1
0x3F	64

Table 12: Single-cycle data length of slave x

SELCRCS1	Addr. 0xC1;	Bit 7	R/W
SELCRCS2	Addr. 0xC5;	Bit 7	R/W
SELCRCS3	Addr. 0xC9;	Bit 7	R/W
SELCRCS4	Addr. 0xCD;	Bit 7	R/W
SELCRCS5	Addr. 0xD1;	Bit 7	R/W
SELCRCS6	Addr. 0xD5;	Bit 7	R/W
SELCRCS7	Addr. 0xD9;	Bit 7	R/W
SELCRCS8	Addr. 0xDD;	Bit 7	R/W

Code	Function
0	Apply CRC polynomial as predefined in SCRCLENx
1	Apply CRC polynomial as individually defined in SCRCPOLYx

Table 13: CRC polynomial selection

BiSS uses CRC polynomials depending on the data length predefined in the EDS and Profile Definitions. The parameter SELCRCSx chooses between predefined polynomials selected according to the CRC length with SCRCLENx and individual CRC polynomials SCRCPOLYx. If SCRCLENx = 0, the CRC verification is deactivated.

SCRCLEN1	Addr. 0xC1;	Bit 6:0	R/W
SCRCLEN2	Addr. 0xC5;	Bit 6:0	R/W
SCRCLEN3	Addr. 0xC9;	Bit 6:0	R/W
SCRCLEN4	Addr. 0xCD;	Bit 6:0	R/W
SCRCLEN5	Addr. 0xD1;	Bit 6:0	R/W
SCRCLEN6	Addr. 0xD5;	Bit 6:0	R/W
SCRCLEN7	Addr. 0xD9;	Bit 6:0	R/W
SCRCLEN8	Addr. 0xDD;	Bit 6:0	R/W

Code	CRC polynomial for single-cycle data
0x00	CRC verification deactivated
0x03	0b1011 = 0xB
0x04	0b1.0011 = 0x13
0x05	0b10.0101 = 0x25
0x06	0b100.0011 = 0x43
0x07	0b1000.1001 = 0x89
0x08	0b1.0010.1111 = 0x12F
0x10	0b1.1001.0000.1101.1001 = 0x190D9
. . .	Other codes are not permitted.

Table 14: CRC length with predefined CRC polynomial

Since the least significant bit of the CRC polynomial is always 1, there is no need to store this information in the CRC polynomial register SCRCPOLYx. Therefore a maximum polynomial length of 8 bit is possible. If the maximum 8 bit polynomial length is not required, the used polynomial (without the LSB bit) is stored right aligned and leading bits are filled with 0.

SCRCPOLY1	Addr. 0xC1;	Bit 6:0	R/W
SCRCPOLY2	Addr. 0xC5;	Bit 6:0	R/W
SCRCPOLY3	Addr. 0xC9;	Bit 6:0	R/W
SCRCPOLY4	Addr. 0xCD;	Bit 6:0	R/W
SCRCPOLY5	Addr. 0xD1;	Bit 6:0	R/W
SCRCPOLY6	Addr. 0xD5;	Bit 6:0	R/W
SCRCPOLY7	Addr. 0xD9;	Bit 6:0	R/W
SCRCPOLY8	Addr. 0xDD;	Bit 6:0	R/W

Code	CRC polynomial for single-cycle data
0x00	CRC verification deactivated
0x01 ...0x7F	Code & '1'
Notes	Example: The CRC polynomial 0x43 = 0b0100.0011 is stored as 0x21 = 0b0010.0001.

Table 15: CRC polynomial

The CRC start values SCRCSTARTx can be used to safely differentiate between single-cycle data words e.g. two position words provided by two different sensors. The same CRC start value that is used in the sensor needs to be applied in the master to validate the received single-cycle data. The CRC start value has a length of 16 bit and is divided into two consecutive 8-bit registers. A typical default slave CRC start value is 0x0000.

SCRCSTART1(7:0)	Addr. 0xC2;	Bit 7:0	R/W
SCRCSTART1(16:8)	Addr. 0xC3;	Bit 7:0	R/W
SCRCSTART2(7:0)	Addr. 0xC6;	Bit 7:0	R/W
SCRCSTART2(16:8)	Addr. 0xC7;	Bit 7:0	R/W
SCRCSTART3(7:0)	Addr. 0xCA;	Bit 7:0	R/W
SCRCSTART3(16:8)	Addr. 0xCB;	Bit 7:0	R/W
SCRCSTART4(7:0)	Addr. 0xCE;	Bit 7:0	R/W
SCRCSTART4(16:8)	Addr. 0xCF;	Bit 7:0	R/W
SCRCSTART5(7:0)	Addr. 0xD2;	Bit 7:0	R/W
SCRCSTART5(16:8)	Addr. 0xD3;	Bit 7:0	R/W
SCRCSTART6(7:0)	Addr. 0xD6;	Bit 7:0	R/W
SCRCSTART6(16:8)	Addr. 0xD7;	Bit 7:0	R/W
SCRCSTART7(7:0)	Addr. 0xDA;	Bit 7:0	R/W
SCRCSTART7(16:8)	Addr. 0xDB;	Bit 7:0	R/W
SCRCSTART8(7:0)	Addr. 0xDE;	Bit 7:0	R/W
SCRCSTART8(16:8)	Addr. 0xDF;	Bit 7:0	R/W

Code	CRC start value for single-cycle data
0x0000 ...0xFFFF	SCRCSTARTx = SCRCSTARTx(16:8) & SCRCSTARTx(7:0)

Table 16: CRC calculation start value

Each data channel can contain actuator data or sensor data. The ACTnSENSx parameter defines the functionality of each BiSS slave on the BiSS bus.

ACTnSENS1	Addr. 0xEF;	Bit 0	R/W
ACTnSENS2	Addr. 0xEF;	Bit 1	R/W
ACTnSENS3	Addr. 0xEF;	Bit 2	R/W
ACTnSENS4	Addr. 0xEF;	Bit 3	R/W
ACTnSENS5	Addr. 0xEF;	Bit 4	R/W
ACTnSENS6	Addr. 0xEF;	Bit 5	R/W
ACTnSENS7	Addr. 0xEF;	Bit 6	R/W
ACTnSENS8	Addr. 0xEF;	Bit 7	R/W

Code	Function
0	Slave is configured as sensor
1	Slave is configured as actuator

Table 17: Slave functionality control

Typically, a BiSS slave expects a leading stop bit before the actuator data which must be enabled with LSTOPx (refer to BiSS C Protocol Description).

LSTOP1	Addr. 0xC0;	Bit 7	R/W
LSTOP2	Addr. 0xC4;	Bit 7	R/W
LSTOP3	Addr. 0xC8;	Bit 7	R/W
LSTOP4	Addr. 0xCC;	Bit 7	R/W
LSTOP5	Addr. 0xD0;	Bit 7	R/W
LSTOP6	Addr. 0xD4;	Bit 7	R/W
LSTOP7	Addr. 0xD8;	Bit 7	R/W
LSTOP8	Addr. 0xDC;	Bit 7	R/W

Code	Function
0	No leading STOP bit on single-cycle actuator data
1	Leading STOP bit on single-cycle actuator data
Notes	LSTOPx is enabled with ACTnSENSx = 1.

Table 18: Actuator stop bit control

The parameter GRAYSx activates a GRAY to binary conversion for SSI encoder.

GRAYS1	Addr. 0xC0;	Bit 7	R/W
GRAYS2	Addr. 0xC4;	Bit 7	R/W
GRAYS3	Addr. 0xC8;	Bit 7	R/W
GRAYS4	Addr. 0xCC;	Bit 7	R/W
GRAYS5	Addr. 0xD0;	Bit 7	R/W
GRAYS6	Addr. 0xD4;	Bit 7	R/W
GRAYS7	Addr. 0xD8;	Bit 7	R/W
GRAYS8	Addr. 0xDC;	Bit 7	R/W

Code	Function
0	SSI single-cycle data binary coded
1	SSI single-cycle data GRAY coded
Notes	GRAYSx is enabled with CFGCHx = 1.

Table 19: SSI format is GRAY code

DATA RAM

For sensor and actuator data a 8x8 byte single-cycle data memory SCDATAx is provided. Eight slaves with up to 64 bit single-cycle data each are supported. The address mapping is shown in Table 20.

SCDATAx	Addr. 0x00 . . . 0x3F; bit 7:0	R/W
Addr.	Content	
0x00	SCDATA1(7:0)	
0x01	SCDATA1(15:8)	
0x02	SCDATA1(23:16)	
0x03	SCDATA1(31:24)	
0x04	SCDATA1(39:32)	
0x05	SCDATA1(47:40)	
0x06	SCDATA1(55:48)	
0x07	SCDATA1(63:56)	
0x08 ...0x0F	SCDATA2(63:0)	
0x10 ...0x17	SCDATA3(63:0)	
0x18 ...0x1F	SCDATA4(63:0)	
0x20 ...0x27	SCDATA5(63:0)	
0x28 ...0x2F	SCDATA6(63:0)	
0x30 ...0x37	SCDATA7(63:0)	
0x38 ...0x3F	SCDATA8(63:0)	

Table 20: Address mapping of single-cycle data

The sensor data is arranged in the memory area with the least significant bit (LSB) at the lowermost address at bit position 0. The memory is written byte by byte and unused bits are set to zero. Unused bytes remain unchanged. In BiSS the CRC bits are inverted before transmission. The received CRC bits are reinverted and then stored at the most significant SCDATAx byte(s) as shown in Table 20 on page 26. This can be disabled with NOCRC = 1.

NOCRC	Addr. 0xE7; Bit 1	R/W
Code	Function	
0	CRC of SCD is stored in SCDATAx	
1	CRC of SCD is not stored in SCDATAx	

Table 21: Storage of received CRC in SCDATAx

Example: BiSS Sensor Bus with 3 Slaves
The following example shows the address mapping of the sensor data and CRC bits generated by three slaves.

Slave 1: 19+2 bits of sensor data, 6 bits of CRC
=> total length of 27 bits

Slave 2: 12+2 bits of sensor data, 5 bits of CRC
=> total length of 19 bits

Slave 3: 24 bits of sensor data, 16 bits of CRC
=> total length of 40 bits

SCDATAx	Addr. 0x00 . . . 0x3F							
Addr.	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x00	Sensor data 1(7:0)							
0x01	Sensor data 1(15:8)							
0x02	0	0	0	Sensor data 1(20:16)				
0x03 ...0x06	not changed							
0x07	0	0	CRC 1(5:0)					
0x08	Sensor data 2(7:0)							
0x09	0	0	Sensor data 2(13:8)					
0x0A ...0x0E	not changed							
0x0F	0	0	0	CRC 2(4:0)				
0x10	Sensor data 3(7:0)							
0x11	Sensor data 3(15:8)							
0x12	Sensor data 3(23:16)							
0x13 ...0x15	not changed							
0x16	CRC 3(7:0)							
0x17	CRC 3(15:8)							
0x18 ...0x3F	not changed							

Table 22: Example address mapping of sensor data

In order to import new sensor data during controller accesses, iC-MB4 has two memory banks for sensor data. While sensor data is being read and written into the first RAM bank during processing of the BiSS Frame, the second RAM bank section containing sensor data of the previous frame can be read by the controller. The relevant sensor data memory banks are swapped at the end of the BiSS Frame. This can be prevented by the controller by setting HOLDBANK (see Table 48). Simultaneously the validity register SVALIDx that corresponds to the RAM bank is also swapped.

CONTROL COMMUNICATION

Control communication enables protected and confirmed reading and writing of the registers of a slave (register communication). It is also used for protected and confirmed sending of BiSS commands to specified slaves or to all slaves. The control data is compounded of 1 bit per single-cycle data frame in each direction. The control data bit sent as part of the single-cycle data frame from master to the slaves is called CDM and the control data bit sent from a slave to the master is called CDS. For more information about the control communication refer to the BiSS C Protocol Description.

If more than one physical BiSS channel is used, the one-hot coded parameter CHSEL selects the channel that is used for control communication. Registers of a BiSS slave can be accessed at one physical channel at a time. BiSS Commands can be sent at both physical channels simultaneously.

CHSEL(1)	Addr. 0xE4;	Bit 0	R/W
Code	Function		
0	Channel 1 not used		
1	Channel 1 used for control communication		
CHSEL(2)	Addr. 0xE4;	Bit 1	R/W
0	Channel 2 not used		
1	Channel 2 used for control communication		
Notes	Channel 1 is selected if CHSEL(1:0) = 00.		

Table 23: Channel mapping for control communication

The type of control communication (register communication or BiSS command) is selected with CTS.

CTS	Addr. 0xE5;	Bit 7	R/W
Code	Function		
0	BiSS Command		
1	Register communication		
Note	Parameter CTS was called MSEL in former MB100 or iC-MB3 data sheets.		

Table 24: Type of control communication

Parameter HOLDCDM determines the clock signal behaviour at pin MA at the end of the frame.
In general operation the BiSS master is configured according to the data channel(s) of the connected BiSS slave(s) as described in on page 24. The data transmission is followed by a timeout which is terminated and signaled to the BiSS master by a rising edge. As soon as the timeout is detected by the BiSS master it can start a new BiSS frame.
If pin SL is not digital low at the end of the frame, e.g. because the BiSS C frame has not been clocked out completely, pin MA can be programmed with HOLDCDM = 1 to be constant until the next frame begins. Thereby it is ensured that the slave can recognize CDM and take part in control communication, even if the master is not configured according to the data channel(s) of the connected BiSS slave(s).

HOLDCDM	Addr. 0xE5;	Bit 0	R/W
Code	Function		
0	MA changes to digital high after detecting the slave's timeout termination at SL.		
1	MA remains constant until the next frame begins		

Table 25: Behavior of pin MA at the end of frame

REGISTER COMMUNICATION

The iC-MB4 supports autonomous register communication with BiSS B and BiSS C. REGVERS is used to select the protocol type. For register write access with extended SSI the BiSS C protocol type needs to be selected.

REGVERS	Addr. 0xE5;	Bit 6	R/W
Code	Function		
0	Register communication BiSS B		
1	Register communication BiSS C		

Table 26: Type of protocol for register communication

The iC-MB4 has an individual 64 byte storage area RDATAx used to store the data of the automatic register communication. In case of a register write access to a BiSS slave, RDATAx must be written with register data by the microcontroller before starting the BiSS communication with INSTR. In case of a register read access to a BiSS slave, the received register data is stored in RDATAx after successful BiSS communication and can then be collected by the microcontroller. In contradiction to SCDATAx there is only one memory bank for RDATAx. Therefore, after performing register communication, RDATAx may only be accessed, if no control communication is currently active (REGEND = 1).

RDATAx	Addr. 0x80 . . . 0xBF;	bit 7:0	R/W
Addr.	Content		
0x80	RDATA1(7:0)		
0x81 ...0xBF	RDATA2(7:0) . . . RDATA64(7:0)		
Notes	Function of register 0x80 depends on CTS. After a register communication via BiSS, RDATAx is accessible, if REGEND = 1.		

Table 27: Address mapping for register communication

The register start address REGADR, register communication direction WNR, number of bytes REGNUM and slave ID SLAVEID are used to configure the BiSS C control communication for register communication. A byte count of 0 entered for REGNUM signals the transmission of a single register value.

REGADR	Addr. 0xE2;	Bit 6:0	R/W
Code	Function		
0x00 ...0x7F	Start address for register communication		

Table 28: Register communication start address

WNR	Addr. 0xE2;	Bit 7	R/W
Code	Function		
0	Read register data		
1	Write register data		

Table 29: Register communication direction

REGNUM	Addr. 0xE3;	Bit 5:0	R/W
Code	Register count		
0x00	1		
0x01 ...0x3E	Code + 1		
0x3F	64		
Notes	If REGNUM>1, a sequential register access is performed (see BiSS C Protocol Description)		

Table 30: Number of consecutive registers to access

SLAVEID	Addr. 0xE5;	Bit 5:3	R/W
Code	Slave ID		
0x00 ...0x07	Code		

Table 31: Slave addressing for register communication (slave to be accessed)

Figure 20 exemplarily shows a control frame including a register read access.

All configuration parameters must be stable during control communication frame.

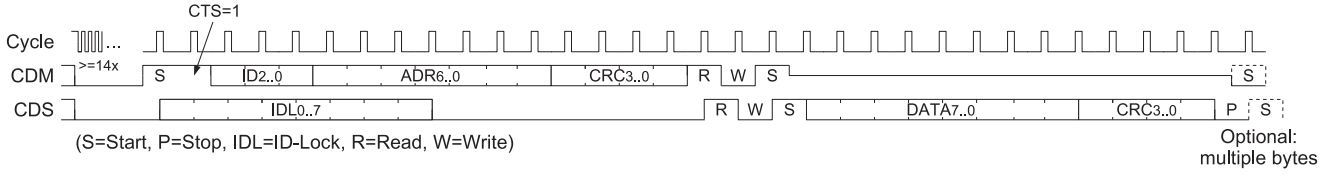


Figure 20: Control frame for register communication (register read access)

BiSS COMMANDS

The BiSS C Protocol Description defines BiSS commands as a subset of the control communication. A BiSS command can address one or several slaves by setting the appropriate bits in IDS. To address all slaves via broadcast commands IDS has to be reset to zero.

IDS(0:7)	Addr. 0x80;	Bit 7:0	R/W
Code	Function		
0x00	All slaves addressed (broadcast)		
IDS7	Addr. 0x80;	Bit 0	R/W
0	Slave with ID 7 is not addressed		
1	Slave with ID 7 is addressed		
IDS6	Addr. 0x80;	Bit 1	R/W
0	Slave with ID 6 is not addressed		
1	Slave with ID 6 is addressed		
IDS4	Addr. 0x80;	Bit 2	R/W
0	Slave with ID 5 is not addressed		
1	Slave with ID 5 is addressed		
IDS4	Addr. 0x80;	Bit 3	R/W
0	Slave with ID 4 is not addressed		
1	Slave with ID 4 is addressed		
IDS3	Addr. 0x80;	Bit 4	R/W
0	Slave with ID 3 is not addressed		
1	Slave with ID 3 is addressed		
IDS2	Addr. 0x80;	Bit 5	R/W
0	Slave with ID 2 is not addressed		
1	Slave with ID 2 is addressed		
IDS1	Addr. 0x80;	Bit 6	R/W
0	Slave with ID 1 is not addressed		
1	Slave with ID 1 is addressed		
IDS0	Addr. 0x80;	Bit 7	R/W
0	Slave with ID 0 is not addressed		
1	Slave with ID 0 is addressed		
Notes	Function of register 0x80 depends on CTS.		

Table 32: Slave addressing for BiSS commands

CMD determines which BiSS command is sent. Some BiSS commands are predefined in the BiSS C Protocol Description, others can be used for device specific functionality of the slave.

CMD(1:0)	Addr. 0xE5;	Bit 5:4	R/W
Code	BiSS Command		
0x00	00		
0x01	01		
0x02	10		
0x03	11		

Table 33: BiSS Command of addressed slave

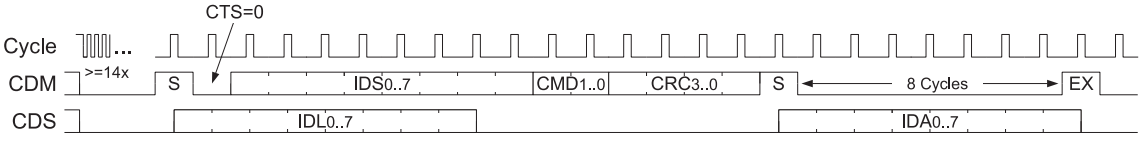
In contrast to broadcast BiSS commands, the reception of an addressed BiSS command is confirmed during IDA (ID acknowledge) by the addressed slave(s). The parameter IDA_TEST defines, if the master triggers the command execution immediately or after checking the IDA bits (see Fig. 21 and 22). The BiSS Command is only executed, if the check is successfull.

IDA_TEST	Addr. 0xE5;	Bit 3	R/W
Code	Function		
0	Immediate execution		
1	The slave's feedback (IDA) is tested before execution. The BiSS Command is not executed, if test fails.		

Table 34: BiSS Command execution control

(S=Start, IDL=ID-Lock, IDS=ID-Select, CMD=Command, EX=Execute)

Figure 21: Control frame for broadcast BiSS command



(S=Start, IDL=ID-Lock, IDS=ID-Select, IDA=ID-Acknowledge, CMD=Command, EX=Execute)

Figure 22: Control frame for addressed BiSS command

FRAME CONTROL

MASTER CONFIGURATION

Master Clock (Pin MA)
The master clock at pin MA is generated for both BiSS and SSI from the system clock f_{CLK} and depends on the frequency division register FREQS. With a typical system clock frequency of 20 MHz, the clock frequency at MA ranges from 10 MHz down to 62.5 kHz.

FREQS	Addr. 0xE6; Bit 4:0	R/W
Code	Single-cycle data clock frequency (f_{MA})	
0x00	f_{CLK} / 2	
0x01 ...0x0F	f_{CLK} / 2 / (Code + 1)	
0x10	"not permitted"	
0x11	f_{CLK} / 40	
0x12 ...0x1F	f_{CLK} / 20 / (Code - 15)	
Notes	f_{CLK} is the system clock (See CLKENI).	

Table 35: Single-cycle data clock frequency at MA (f_{MA})

Both BiSS and SSI slave devices recognize an idle bus at the end of a transmission frame via timeout detection.Thus, the choice of possible clock frequencies is limited as the duration of each logic level may not exceed the shortest timeout of all the connected slaves.

BiSS B devices switch to register mode when recognizing that the bus is idle after a falling-edge on the clock input MA. The master is notified about entering register mode via data line SL, see Ttos (Item I306).

The clock frequency in BiSS B register mode is selected depending on the single-cycle data clock frequency via parameter FREQR and is in the range of 244 Hz to 5 MHz. The selection is also limited since a different timeout detection does now recognize the idle bus at the end of the cycle (see BiSS B Protocol Description).

FREQR	Addr. 0xE6; Bit 7:5	R/W
Code	Register data clock frequency	
0x00	f_{MA} / 2	
0x01 ...0x06	f_{MA} / $2^{(Code+1)}$	
0x07	f_{MA} / 256	
Notes	f_{MA} is the single-cycle data clock frequency configured with FREQS. FREQR = 0x05 must be set, if CFGCHx = 0x01.	

Table 36: BiSS B register data frequency

BiSS B devices typically require a minimum clock frequency (such as 250 kHz) because the MA clock possibly has to be evaluated as a PWM signal for register communication. BiSS C devices generally permit a lower clock frequency. BiSS C devices do not use a MA clock duty cycle (PWM signal) and can be operated down to 80 kHz. SSI devices generally permit a lower clock frequency and with extended SSI, the register access is similar to BiSS C and can be operated down to 80 kHz.

BiSS Frame Repetition Rate
The FREQAGS controls the automatic data transmission (AGS, see Table 44). With FREQAGS the frame repetition rate can be set to a dedicated ratio of the system clock frequency f_{CLK}. With a system clock frequency of 20 MHz frame repetition rates from 1 µs to 4 ms are possible. FREQAGS must be set in a way that the time in between two frames is greater than a complete cycle. One cycle consists of the transmission of a request, an acknowledge signal (including line delay), a start bit (including processing time), a control data bit (BiSS C), the sensor data and CRC bits of each slave and the maximum BiSS timeout of all connected slaves.

FREQAGS	Addr. 0xE8; Bit 7:0	R/W
Code	Frame repetition rate	
0x00	f_{CLK} / 20	
0x00 ...0x7B	f_{CLK} / 20 / (Code +1)	
0x7C	AGSMIN	
0x7D ...0x7F	AGSINFINITE	
0x80 ...0xFF	f_{CLK} / 625 / (Code - 127)	
Notes	FREQAGS is activated with AGS. f_{CLK} is the system clock (See CLKENI).	

Table 37: Frame repetition rate (AGS frequency divider)

AGSMIN
With FREQAGS = AGSMIN the master automatically restarts the next frame after the previous frame is finished. iC-MB4 automatically generates the highest frame rate possible. FREQAGS = AGSMIN requires completed BiSS frames to ensure a low level at SL at the end of each frame. The rate depends on the configured sensor data clock frequency (FREQS, the slave configurations (e.g. SCDLENx), the maximum processing time of the slaves and the total system line delay.

AGSINFINITE
With FREQAGS = AGSINFINITE the master does not automatically restart the next cycle. AGSINFINITE requires a trigger event to start the next frame. The next frame is started by a digital pulse at the GETSENS pin or by setting INSTR.

Data Handling
With SINGLEBANK=0 two RAM banks are used for buffering the SCDATAx. Thus, as described in SINGLE-CYCLE DATA on page 24 it is ensured that one RAM bank can be written with single-cycle data received by iC-MB4 at the BiSS interface while the single-cycle data content of the other RAM bank is read by the microcontroller. A downgrade is possible by setting SINGLEBANK=1.

SINGLEBANK	Addr. 0xE7;	Bit 0	R/W
Code	Function		
0	Two RAM banks are used for SCD		
1	One RAM bank is used for SCD		

Table 38: Use of one/ two RAM bank(s) for SCDATAx

The data output pin MO is used to set the processing time per parameter for all slaves and to send the actuator data. In order to use output MO, it must be enabled with EN_MO=1.

EN_MO	Addr. 0xE5;	Bit 1	R/W
Code	Function		
0	Set and hold MO at low state		
1	Data output at MO enabled		

Table 39: Enable data output at MO

The processing time per parameter is set by the delay of the start bit at MO. The delay is configured with MO_BUSY in periods of MA.

MO_BUSY	Addr. 0xE9;	Bit 7:0	R/W
Code	Start bit delay at MO		
0x00	No start bit delay		
0x01 ...0x0F	Code * 1 / f_{MA}		
Notes	f_{MA} is the single-cycle data clock frequency configured with FREQS.		

Table 40: Processing time per parameter

BiSS Master Device Identification
The BiSS master device is identifiable with parameters VERSION and REVISION. A host software can use these parameters to identify the present device and verify the compatibility of software and device.

VERSION	Addr. 0xEB;	Bit 7:0	R
Code	Version		
0x83	iC-MB3		
0x84	iC-MB4		
. . .			
0xFF			

Table 41: iC-MB version

REVISION	Addr. 0xEA;	Bit 7:0	R
Code	Revision		
0x10	Z(first revision)		
0x11	Z1		
0x20	Y		
. . .			
0xFF			

Table 42: iC-MB4 redesign ID

The device factory test may not be activated, keep ENTEST=0.

ENTEST	Addr. 0xF5;	Bit 1	R/W
Code	Function		
0	Device in normal operation mode		
1	Not permitted		

Table 43: Enable device factory test mode

DATA ACQUISITION

Data transmissions are triggered

- automatically by iC-MB4 (FREQAGS ≠ AGSINFINITE),
- by pin GETSENS (FREQAGS = AGSINFINITE),
- or by selecting a program with INSTR.

Automatic Sensor Data Request

With AGS = 1 and FREQAGS = AGSMIN data transmissions are started automatically as soon as the slave's timeout is detected by iC-MB4. With FREQAGS configured to a constant frame repetition rate data transmissions are started automatically at the configured frame repetition rate.

AGS	Addr. 0xF4;	Bit 0	R/W
Code	FREQAGS	Function	
0		No automatic data transmission	
1	AGSMIN	Start of data transmission after slave's timeout	
1	AGSINFINITE	Start of data transmission triggered by pin GETSENS	
1	Other	Start of data transmission equally spaced at a constant rate	
1	Notes	When using AGS, please refer to Table 69.	

Table 44: Automatic Get Sensor Data (AGS)

Sensor Data Request by Pin GETSENS

Pin GETSENS can be used to start a new BiSS frame, if enabled by AGS = 1 and FREQAGS = AGSINFINITE. Its default pin state is digital low due to the internal pull-down resistor. The GETSENS pin operates statically. Thus, a digital high at GETSENS will start a new BiSS frame. The minimum signal duration at GETSENS is one system clock period f_{CLK}. A digital high that is longer than the SCD cycle will start the next SCD cycle, if HOLDCDM = 0. The delay between trigger event at GETSENS and the falling edge at MA is defined by the system clock f_{CLK} and the single-cycle clock frequency f_{MA} (configured with FREQS):

$$t_{\text{GETSENS to falling edge at MA}} = \frac{2}{f_{CLK}} + \frac{1}{2 * f_{MA}}$$

For high precision capturing it is recommended to use a system clock based GETSENS digital high pulse.

Program Selection with Instructions

INSTR is used to trigger data transmissions by program. With AGS = 0 the master starts the data transmission after finishing writing the instruction register (rising edge of NWR on parallel interface, last rising edge of SCLK on SPI interface) and resets INSTR after executing the frame automatically. An nAGSERR error will be generated if the SLx line is low at the start of the frame. The error can be suppressed by setting FREQAGS = AGSMIN due to waiting for a high state at SLx. A BiSS B register access or a BiSS C control communication (refer to REGVERS, page 28) can be triggered via INSTR as well. It is also possible to enable reduced BiSS frames for control communication with BiSS commands. Within a running control communication the CDM bit is generated automatically. Otherwise the generation of CDM depends on INSTR.

INSTR	Addr. 0xF4;	Bit 3:1	R/W
Code	AGS	Function	
000	0	Reset state. No INSTR performed.	
010	0	Start one frame with CDM = 0. INSTR automatically resets.	
010	1	Upcoming frames with CDM = 0.	
001	0	Start one frame with CDM = 1. INSTR automatically resets.	
001	1	Upcoming frames with CDM = 1.	
011	0	Start one frame with CDM = not(CDSSEL). INSTR autom. resets.	
011	1	Upcoming frames with CDM = not(CDSSEL).	
100	0	Start one frame with control communication. INSTR autom. resets.	
100	1	Upcoming frames with control communication. INSTR will be reset at the end of the control communication.	
111	0	Start one reduced frame with control communication. INSTR autom. resets.	
111	1	Upcoming reduced frames with control communication. INSTR will be reset at the end of the control communication.	

Table 45: SCD Control Instruction

Typically, the BiSS data line SLx is set to digital high by the last slave after timeout. After power-on or after a failure the last slave may not be defined and the SLx line is digital low. An initialisation sequence started by INIT can be used to initialize the slave chain. Additionally an INIT sets the status bits nSCDERR, nREGERR, nDELAYERR and nAGSERR to 1 and resets REGEND to 0.

INIT	Addr. 0xF4;	Bit 4	R/W
Code	REGVERS	Function	
0	-	No operation	
1	0	BiSS B initialize (see Figure 16)	
1	1	BiSS C initialize (see Figure 13)	

Table 46: Start initialisation sequence

With REGVERS = 1 (BiSS C) and an INIT iC-MB4 stores the measured line delay of the physical channel 1 in

SCDATA1(7:0) and the line delay of the physical channel 2 in SCDATA5(7:0).
The unit of these values is 1/4 of the configured single-cycle data clock frequency at MA (f_{MA}) configured with FREQS.

$$t_{\text{Line Delay Channel 1}} = \frac{SCDATA1(7:0)}{4 * f_{MA}}$$

$$t_{\text{Line Delay Channel 2}} = \frac{SCDATA5(7:0)}{4 * f_{MA}}$$

For the INIT sequence the maximum line delay is 255. If this limit is exceeded, the INIT sequence is aborted and nAGSERR is activated (nAGSERR = 0). The INIT sequence does not test the SLx state. A constant SLx = 0 state is ignored and does not set any error state.

All current actions can be aborted using the BREAK command, so that iC-MB4 enters a defined state, if one of the sensors does not respond correctly.

BREAK	Addr. 0xF4;	Bit 7	R/W
Code	Function		
0	No operation		
1	Abort data transmission		
Note	An INIT should be executed after BREAK to ensure resetting status bits		

Table 47: Start BREAK Sequence

When reading more than one Data RAM registers by the controller it is possible that the RAM banks in the master could be switched once a sensor data transmission via BiSS is completed. To avoid unexpected bank switching, the controller can set HOLDBANK before reading Data RAM registers and releases it afterwards.

If bank switching was prevented with HOLDBANK = 1, the bank is switched after resetting HOLDBANK = 0. If a new BiSS frame is scheduled before HOLDBANK is reset (e.g. when using AGS with a high FREQAGS), no bank switching is performed but nAGSERR will be set.

HOLDBANK	Addr. 0xF4;	Bit 6	R/W
Code	Function		
0	Automatic bank switching is permitted		
1	Automatic bank switching is prevented		

Table 48: RAM Bank Control

By inverting SWBANK's value a switch of the RAM banks is forced. This can be used, for instance, to initialize the content of both RAM banks.

SWBANK		Addr. 0xF4; Bit 5	R/W
Previous code	New code	Function	
0	0	No operation	
0	1	RAM banks are switched	
1	0	RAM banks are switched	
1	1	No operation	

Table 49: RAM Bank Switching

The following parameters are used to control the MA clock line which is selected with the parameter CHSEL (see Table 23).

MAFS	Addr. 0xF5;	Bit 4	R/W
Code	Function		
0	Selected MA line is not controlled		
1	Selected MA line is forced with MAVS		
Notes	The MA line is selected with CHSEL		

Table 50: Control of the selected MA line

MAVS	Addr. 0xF5;	Bit 5	R/W
Code	Force value for selected MA		
0	Low		
1	High		

Table 51: Selected MA line force level

The following parameters are used to control the MA clock lines for the remaining channels which are not selected with CHSEL.

MAFO	Addr. 0xF5;	Bit 6	R/W
Code	Function		
0	Not selected MA lines not controlled		
1	Not selected MA lines forced with MAVO		

Table 52: Control of the not selected MA line

MAVO	Addr. 0xF5;	Bit 7	R/W
Code	Force value for not selected MA		
0	Low		
1	High		

Table 53: Not selected MA lines force level

STATUS

The status information is combined in a set of registers. It indicates all device and communication states of the master.

The EOT flag is connected to pin EOT and signals a running frame as described in FUNCTIONAL DESCRIPTION on page 15.

EOT	Addr. 0xF0;	Bit 0	R
Code	Function		
0	Data transmission active		
1	Data transmission not active		

Table 54: End-of-Transmission

An error in the single-cycle data detected by checksum verification (CRC) is shown with nSCDERR. If nSCDERR=0, the faulty sensor can be identified by reading SVALIDx (see Table 61).

nSCDERR	Addr. 0xF0;	Bit 4	R
Code	Function		
0	Error in last single-cycle data transmission		
1	No error in last single-cycle data transmission		

Table 55: SCD transmission error

The control communication including accesses to the slave's registers uses three dedicated flags. REGEND signals a finished control communication. It is also set, if the control communication was not successful. nREGERR signals the status. A missing start bit is shown with nDELAYERR. The REGEND flag is reset after power-on, an INIT and when starting a new control communication.

REGEND	Addr. 0xF0;	Bit 2	R
Code	Function		
0	Control communication running or not started since power-on/INIT		
1	Control communication completed/not running		

Table 56: End of Control Communication

The nREGERR and the nDELAYERR flags are set after power-on and after executing INIT (see Table 46). If a register data error is detected, the number of bytes transmitted correctly before the error occurred is provided by the register message REGBYTES (see Table 63). In case of an error the transmission of data is terminated.

The following issues can cause error indication with nREGERR:

- Read register access: CRC error or inverted R-bit
- Write register access error in repeated CDS data
- BiSS Commands: error in IDA

nREGERR	Addr. 0xF0;	Bit 3	R
Code	Function		
0	Error in last control communication		
1	No error in last control communication		

Table 57: Control communication error

nDELAYERR notifies about a missing start bit in last register communication. The addressed slave register might not be implemented.

nDELAYERR	Addr. 0xF0;	Bit 5	R
Code	Function		
0	Missing start bit in last register data transmission. Register address not implemented or register access processing time too long (> 20 ms, if FREQR = 0x05).		
1	No missing start bit in last register data transmission		
Notes	The Microcontroller can abort register communication after t_{busy_r} (as defined in BiSS C Protocol Description).		

Table 58: Start bit in register communication

When automatic transmission of sensor data is enabled with instruction bit AGS, an AGS watchdog error nAGSERR is indicated, if no new cycle could be initiated. If the last BiSS frame has not been finished in time, the next BiSS frame will be omitted. The following BiSS frame will be executed, if possible. The nAGSERR flag is also indicated, if a write access to instruction register 0xF4 is performed (e.g. by writing BREAK into the instruction register).

nAGSERR	Addr. 0xF0;	Bit 6	R
Code	Function		
0	At least one BiSS frame has been omitted		
1	No missing BiSS frames		

Table 59: AGS error

The nERR flag indicates the state of pin NER. Pin NER is low, if any of the aforementioned errors is indicated. It is possible to input an open-collector error signal (active low) from other components to pin NER.

nERR	Addr. 0xF0;	Bit 7	R
Code	Function		
0	External or internal error occured		
1	No error occurred		

Table 60: State of the pin NER

The CRC verification result of the received single-cycle sensor data of every BiSS frame is written to the validity message register SVALIDx for each slave separately. If the CRC is disabled in the slave configuration the correspondent SVALID flag is set after reading of sensor data has been completed. The validity flags are reset by writing to the SVALIDx register.

After reading sensor data it is recommended to reset the SVALIDx flags in order to recognize updated sensor data.

SVALID1	Addr. 0xF1;	Bit 1	R/W
SVALID2	Addr. 0xF1;	Bit 3	R/W
SVALID3	Addr. 0xF1;	Bit 5	R/W
SVALID4	Addr. 0xF1;	Bit 7	R/W
SVALID5	Addr. 0xF2;	Bit 1	R/W
SVALID6	Addr. 0xF2;	Bit 3	R/W
SVALID7	Addr. 0xF2;	Bit 5	R/W
SVALID8	Addr. 0xF2;	Bit 7	R/W
Code	Function		
0	Single-cycle data invalid		
1	Single-cycle data valid		

Table 61: SCDATAx validity indication

Switching the SCDATAx RAM bank - which is executed at the end of a BiSS frame - also switches the corresponding SVALIDx flags. It fails, if the user disables bank switching via HOLDBANK (see Table 48)

SWBANKFAIL	Addr. 0xFB;	Bit 0	R
Code	Function		
0	Bank switching (SCDATAx) successful		
1	Bank switching (SCDATAx) not successful		

Table 62: Bank switching status

In case of an error in a sequential register communication, the number of faultless transmitted register values are stored in REGBYTES. REGBYTES is reset, if an INIT sequence is transmitted or a new control communication started.

REGBYTES	Addr. 0xF3;	Bit 5:0	R
Code	nREGERR	Number of valid register bytes	
0	1	All	
0x00 ...0x3F	0	Code	

Table 63: Number of valid register bytes

For BiSS C control communication a minimum number of SCD cycles with exclusively CDM = 0 must be sent before starting a new control communication frame. For a manual control communication by the host microcontroller the CDMTIMEOUT bit indicates that ≥ 14 SCD cycles with exclusively CDM = 0 have already been sent.

CDMTIMEOUT	Addr. 0xF3;	Bit 7	R
Code	Function		
0	Timeout of BiSS C control communication not reached		
1	Timeout of BiSS C control communication reached		

Table 64: CDM timeout reached

The value of the control data slave bit (CDS) is sampled for each channel in CDSx. Additionally, the CDS of the physical channel selected with CHSEL is provided by CDSSEL.

CDS1	Addr. 0xF8;	Bit 1	R
CDS2	Addr. 0xF8;	Bit 3	R
Code	CDS value from appropriate channel		
0	CDSx = 0		
1	CDSx = 1		
Notes	Indication of CDSx is only valid, if SINGLEBANK = 0.		

Table 65: CDSx bit of channels

CDSSEL	Addr. 0xF3;	Bit 6	R
Code	CDS value from the selected channel		
0	0		
1	1		
Notes	Indication of CDSSEL is only valid, if SINGLEBANK = 0.		

Table 66: CDS bit from the selected channel (CHSEL)

Note: There are two RAM banks for SVALIDx, CDSSEL and CDSx that switch simultaneously to the SCDATAx RAM banks.

The actual state of the BiSS data input pins SL1 and SL2_NSL1 is available in SLx.

SL1	Addr. 0xF8;	Bit 0	R
SL2	Addr. 0xF8;	Bit 2	R

Code	Function
0	SLx line level low
1	SLx line level high

Table 67: SLx input lines state

DESIGN REVIEW

iC-MB4 Z1		
No.	Function, Parameter/Code	Description and application notes
1	MO_BUSY	Control communication fails, if MO_BUSY ≠ 0 and output MO is not connected to slave input SLI.
2	Actuator data	Transmission of actuator data on both channels with different SCD length fail, if CDM = 0.
3	BiSS C initialize sequence	Line delay measurement fails, if line delay of one channel is bigger than line delay plus timeout of the other channel.
4	CDS1, CDS2, CDSSEL	CDSx and CDSSEL only indicate valid information, if SINGLEBANK = 0.

Table 68: Notes on chip functions regarding iC-MB4 chip revision Z1.

iC-MB4 Y		
No.	Function, Parameter/Code	Description and application notes
1	AGS	When using AGS, the SVALIDx flag must be checked each time after reading single-cycle data by the microcontroller. The following steps should be performed: • Set HOLDBANK. • Read single-cycle data (SCDATAx) with the microcontroller. • Read and reset SVALIDx flag. • Reset HOLDBANK. • If SVALIDx=0 then send BREAK instruction and set AGS subsequently. • Repeat the procedure when the next single-cycle data is read by the microcontroller
2	CDS1, CDS2, CDSSEL	CDSx and CDSSEL only indicate valid information, if SINGLEBANK = 0.

Table 69: Notes on chip functions regarding iC-MB4 chip revision Y.

REVISION HISTORY

Rel.	Rel. Date*	Chapter	Modification	Page
A1	14-06-24		Initial Release.	

Rel.	Rel. Date*	Chapter	Modification	Page
B1	14-11-20	PACKAGING INFORMATION	Function text on pin 25 NWR_E swapped with Function text on pin 26 NRD_RNW: • NWR_E: Read Input, active low (Intel) Read/Not-Write Select Input (Motorola) • NRD_RNW: Write Input, active low (Intel) Enable Input, active high (Motorola)	4
		ELECTRICAL CHARACTERISTICS	Vc()hi Clamp Voltage hi MAX updated from 1.65 V to 1.75 V	8
		ELECTRICAL CHARACTERISTICS	f(CLKI) Oscillator Clock Frequency VDD = 3.0 V ... 3.6 V MAX updated from 20 MHz to 22 MHz	9
		FUNCTIONAL DESCRIPTION	INIT = 1 updated	21
		INSTRUCTION REGISTER	”All configuration parameter must be stable during data transmission” added	28
		CONFIGURATION MASTER	AUTOMATIC REQUEST FOR SENSOR DATA moved into chapter CONFIGURATION MASTER	29
		CONFIGURATION CHANNEL	CFGIF footnote added: RS422 interfaces are only operatable with VDD = 4.5 V ... 5.5 V	31
		CONFIGURATION SLAVE	Slave Configuration CRC Verification: • CRC for single cycle data not present, CRC verification deactivated, SELCRCSx = 0b0 • CRC polynomial(7:1) in SCRCPOLYx SELCRCSx = 0b1 not applicable with CRC polynomial SCRCPOLYx(7:1) = 0x00 • CRC polynomial 0x00 not applicable with SELCRCSx = 0b1 • Other CRC lengths in SCRCLENx are not permitted with SELCRCSx = 0b0	32
		STATUS INFORMATION 1	Bit address of nDELAYERR 0xF0 updated to 5	35
		APPLICATION DESIGN TRANSFER FROM iC-MB3 TSSOP24 TO iC-MB4 TSSOP24	Disabling SCD CRC verification To deactivate the SCD CRC verification select: • SELCRCSx = 0b0 • CRC bit length in SCRCLENx = 0 • Extend the SCDLEN by the length of the present CRC that is subject to be ignored A CRC polynomial SCRCPOLYx = 0x00 is not applicable with SELCRCSx = 0b1.	38
		DESIGN REVIEW	Chapter DESIGN REVIEW added	39
		FUNCTIONAL DESCRIPTION	Measuring the line delay on channel 1 and channel 2, measuring unit added	21

Rel.	Rel. Date*	Chapter	Modification	Page
B2	2015-07-07	DESCRIPTION	BiSS BUA added	2
		FUNCTIONAL DESCRIPTION	Maximum line delay while INIT = 255, overflow abort and AGERR is set	21
		INSTRUCTION REGISTER	All configuration parameter must be stable during SCD data transmission	28

Rel.	Rel. Date*	Chapter	Modification	Page
C1	2018-09-11	All	Minor text details updated	all
		ELECTRICAL CHARACTERISTICS	Bxx section: SSI added	8
		ELECTRICAL CHARACTERISTICS	Item D05 updated	9
		ELECTRICAL CHARACTERISTICS	Item C08 added	9
		ELECTRICAL CHARACTERISTICS	Item I008 updated	13
		ELECTRICAL CHARACTERISTICS	Item I110 updated	13
		ELECTRICAL CHARACTERISTICS	Item I207 updated	13
		ELECTRICAL CHARACTERISTICS	Item I506 Ttos permissible timeout (slave) added	17

		REGISTER LAYOUT, OVERVIEW	Existing or missing ” on bit states replaced by ’	18, 19
		INSTRUCTION REGISTER	Note added: an INIT should be executed after BREAK to ensure resetting status bits, Table 71	38
		APPLICATION DESIGN TRANSFER FROM iC-MB3 TSSOP24 TO iC-MB4 TSSOP24	Chapter removed	39

Rel.	Rel. Date*	Chapter	Modification	Page
D1	2021-11-30	All	Removed "Preliminary" and added colored links. Adjusted chapter order and performed updates for improved understanding.	All
		BLOCK DIAGRAM	Updated block diagram.	1
		DESCRIPTION	Removed BUA disclaimer.	2
		PACKAGING INFORMATION	Removed PACKAGING INFORMATION for TSSOP24 package due to discontinuation.	3
		ABSOLUTE MAXIMUM RATINGS	Updated G003: ”V()VDD + 0.3 V” → ”V()≤ VDD + 0.3 V”	5
		THERMAL DATA	Removed $R_{thjaTSSOP}$ due to discontinuation of TSSOP24 package.	5
		ELECTRICAL CHARACTERISTICS	Updated f(CLKI): - VDD = 4.5 V ... 5.5 V: f_Min = 12.5 MHz (before 15 MHz) - VDD = 3.0 V ... 3.6 V: f_Max = 22.5 MHz (before 22 MHz). Updated name B12 and B19: Vcom() → Vcm(). Updated El.Char. E06: Min. 300 mV → 150 mV and Typ. 500 mV → 250 mV.	7ff
		OPERATING REQUIREMENTS	Updated references in conditions for I301. Updated references in conditions for I401. Updated references in conditions for I501. Added "MA" und "SL" for timing diagram SSI mode Figure 10.	12ff
		MICROCONTROLLER INTERFACE	Updated SPI Command names, description and Figure 19. Corrected address range to read SCDATAx with second SPI channel.	17ff
		OSCILLATOR	Chapter introduced.	23
		BiSS/SSI INTERFACE	Renamed chapter CONFIGURATION CHANNELS to BiSS/SSI INTERFACE. Added note for CFGCH2.	23
		SINGLE-CYCLE DATA	Renamed chapter SLAVE CONFIGURATION to SINGLE-CYCLE DATA. Included chapter SENSOR AND ACTUATOR DATA. Added note for GRAYS and LSTOP. Renamed SCRCSTARTx_H → SCRCSTARTx(16:8). Renamed SCRCSTARTx_L → SCRCSTARTx(7:0). Moved NOCRC in SINGLE-CYCLE DATA chapter. Clarified storage of CRC in SCDATAx.	24ff
		CONTROL COMMUNICATION	Included chapter REGISTER DATA in CONTROL COMMUNICATION. Removed "BiSS A" from REGVERS.	27
		FRAME CONTROL	Renamed chapter MASTER CONFIGURATION to FRAME CONTROL. Renamed chapter INSTRUCTION REGISTER to DATA ACQUISITION and included it. Included GETSENS chapter. Renamed "FSCD" → "f_{MA}" at FREQS. Corrected formula for FREQR. Updated description and corrected address in parameter table SINGLEBANK. Improved description of INSTR and added "Reset State" (=000). Improved description for HOLDBANK.	30ff
		STATUS	Improved parameter description. Renamed SWBANKFAILS → SWBANKFAIL.	34f
		DESIGN REVIEW	Added hint for using AGS.	37
		ORDERING INFORMATION	Added order designation for extended temperature range. Removed order designation for TSSOP24 package due to discontinuation.	41

Rel.	Rel. Date*	Chapter	Modification	Page
D2	2022-01-14	FRAME CONTROL	Added note for FREQR.	30
		STATUS	Added note for nDELAYERR. Added note for CDSx and CDSSEL.	34f
		DESIGN REVIEW	Added note for CDSx and CDSSEL.	37

* Release Date format: *YYYY-MM-DD*

ORDERING INFORMATION

Type	Package	Options	Order Designation
iC-MB4	QFN28-5x5		iC-MB4 QFN28-5x5
		Temperature range -40 °C to 125 °C	iC-MB4 QFN28-5x5 ET -40/125
Evaluation Board			iC-MB4 EVAL MB4_1D

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